JZ4770

Mobile Application Processor

Programming Manual

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

JZ4770 Mobile Application Processor

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Ingenic Semiconductor Co., Ltd.

Room 108, Building A, Information Center, Zhongguancun Software Park
8 Dongbeiwang West Road, Haidian District, Beijing, China,
Tel: 86-10-82826661
Fax: 86-10-82825845
Http: //www.ingenic.cn

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1 Overview

JZ4770 is a mobile application processor targeting for multimedia rich and mobile devices like smartphone, tablet computer, mobile digital TV, and GPS. This SOC introduces innovative dual-core architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices.

The CPU (Central Processing Unit) core, equipped with 16kB instruction and 16kB data level 1 cache, and 256kB level 2 cache, operating at 1000MHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst processor engine. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst processor engine. The SIMD instruction set implemented by XBurst engine, in together with the on chip video accelerating engine and post processing unit, delivers doubled video performance comparing with the single core implementation.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit/8-bit/12-bit/16-bit/24-bit ECC MLC/TLC NAND flash memory for cost sensitive applications.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. TV encoder unit 10-bits DAC provide composite TV signal output in PAL or NTSC format. The LCD controller support up to 1920x1080 output, LVDS as well as plain RGB output which support external HDMI transmitter. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB OTG and USB 1.1 host, Ethernet MAC with MII and RMII interface, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

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1.1 Block Diagram

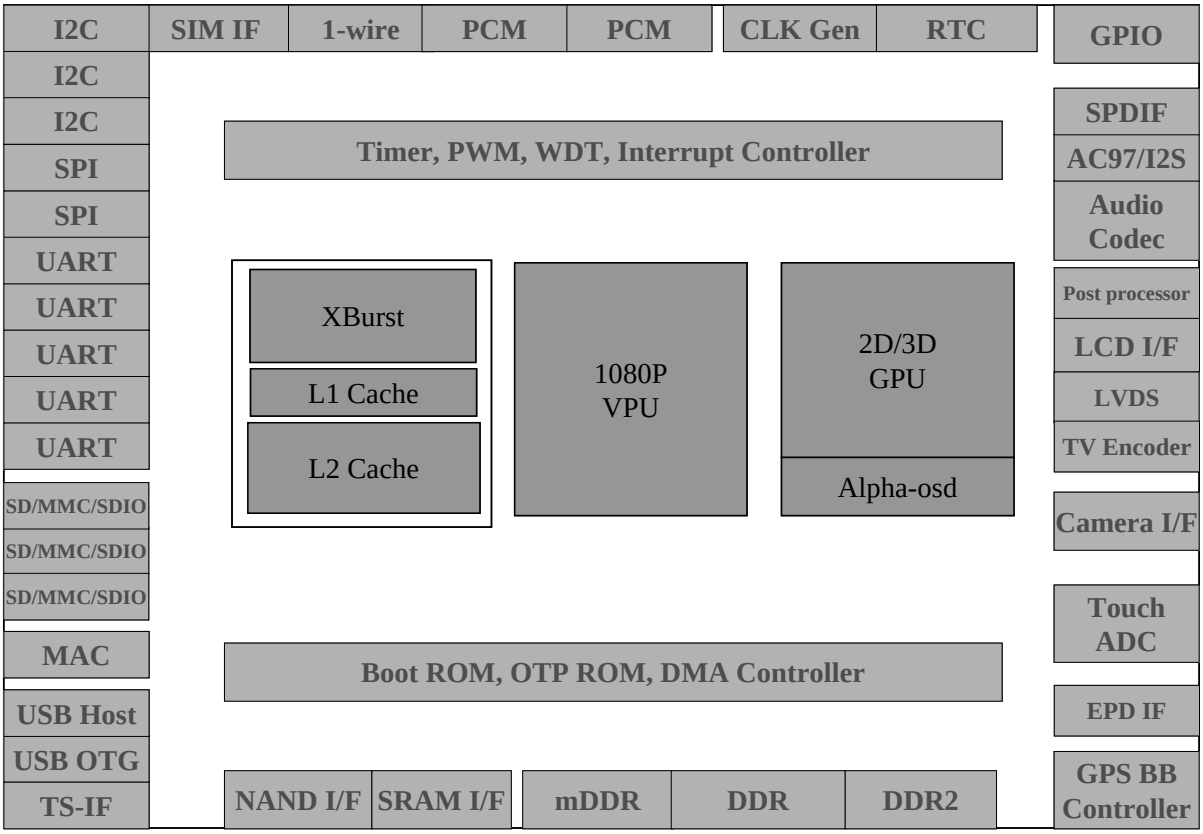


Figure 1-1 JZ4770 Diagram

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1.2 Features

1.2.1 CPU Core

- XBurst CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE745 compatible
  - XBurst® 8-stage pipeline micro-architecture up to 1000MHz
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16kB instruction cache
  - 16kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
  - 256kB unify cache

1.2.2 VPU Core

- XBurst CPU for video processing
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® 8-stage pipeline micro-architecture up to 500MHz
- Video acceleration engine
  - Motion compensation
  - Motion estimation
  - De-block
  - DCT/IDCT for 4x4 block
  - Parser
- 48kB tight coupled memory
- 28kB scratch RAM

1.2.3 GPU Core

- 2D graphic
  - Bit BLT and stretch BLT
  - Line/Rectangle
  - ROP2, ROP3, ROP4/Alpha blending/scaling/Filter
  - Rotation (90/180/270 degree)/Mirror/Transparency/Rendering

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  - Pixel rate up to 200M pix/s
- 3D graphic
  - OpenGL ES2.0 compliance, including extensions
  - OpenGL ES1.1/OpenVG 1.1 compliance
  - DirectFB/GDI/DirectDraw compliance
  - Geometry rate up to 20M tri/s
  - Pixel rate up to 200M pix/s
- Alpha-osd
  - Support ARGB8888, RGB565, RGB555
  - Each layer has an alpha value for all pixels
  - Up to 800*480
  - Software can change overlay orders
  - The level of overlay can be set by software
  - Software must make sure the address of source and destination are 64-word aligned
  - Support 64-burst in AHB bus
  - In RGB656 & RGB555mode, software must make sure each line aligned in word

1.2.4 Memory Sub-systems

- DDR Controller
  - Support DDR2, DDR, mobile DDR (LPDDR) memory
  - Support x16 and x32 external DDR data width
  - Support clock frequency ratio – (BUS clock) : (DDR clock) = 2:1
  - Support clock frequency ratio – (BUS clock) : (DDR clock) = 1:1
  - Support clock-stop mode
  - Support auto-refresh and self-refresh
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width
- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Six chip-select pins for static memory, each can be configured separately
  - Support 8 or 16 bits data width
  - 6 bits address
- NAND flash interface
  - Support 4-bit/8-bit/12-bit/16-bit/24-bit MLC/TLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Support automatic boot up from NAND Flash devices
- BCH Controller
  - Support 4-bit/8-bit/12-bit/16-bit/24-bit ECC encoding and decoding for NAND
- Direct memory access controllers
  - BDMA controller
    - 3 independent DMA channels

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  - Support data transfer between normal memory (NAND, SRAM, etc.) / BCH and system memory (DDR)
- General purpose DMA
  - 12 independent DMA channels
  - Support data transfer between On-chip Peripherals (e.g. I2C, MSC, etc.) and system memory (DDR)
  - APB bus bridge
- Common features
  - Descriptor supported
  - Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte, 32-byte or 64-byte
  - Transfer number of data unit: 1 ~ 224
  - Independent source and target port width: 8-bit, 16-bit, 32-bit

- The XBurst processor system supports little endian only

1.2.5 AHB Bus Arbiter

- Provide a fair chance for each AHB master to possess the AHB bus
- Fulfill the back-to-back feature of AHB protocol
- Automatic privilege for some masters and programmable privilege for others. Round-robin possession for masters in the same privilege

1.2.6 System Devices

- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
  - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, HCLK, HHCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function
  - Support module power-down
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
  - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports

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- Interrupt source and pending registers for software handling
- Unmasked interrupts can wake up the chip in sleep or standby mode

- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset

1.2.7 Audio/Display/UI Interfaces

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 24-bit data bus
  - Support 1,2,4,8 pins STN panel, 16bit, 18bit and 24bit TFT and 8bit I/F TFT
  - Display size up to 1920x1080 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)
  - Support delta RGB
  - One single color background and two foreground OSD
  - Compressed frame supported
  - Support LVDS signal output
- TV encoder
  - Support NTSC or PAL
  - Support CVBS signal
  - 10 bits DAC
- EPD controller
  - Supports Electro-Phoretic Display and compatible devices
  - Supports different size of display panel
  - Supports different width of pixel data

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- Supports internal DMA operation and register operation

- Image post processor
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert
  - Bi-cubic algorithm supported
  - Video enhancement
- Camera interface module
  - Input image size up to 4096×4096 pixels
  - Supports CCIR656 data format
  - YCbCr 4:2:2 and YCbCr 4:4:4 data format
  - Raw data input
  - 64×32 image data receive FIFO with DMA support
- On-chip audio CODEC
  - 24-bit DAC, SNR: 95dB
  - 24-bit ADC, SNR: 90dB
  - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
  - L/R channels line input
  - 2 MICs input, differential or single-ended
  - L/R channels headphone output amplifier support up to 16ohm load
  - Capacitor-coupled
  - Mono differential line out
  - Mono 450mW amplifier for speaker out for 8ohm load
- AC97/I2S/SPDIF controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - Support 2/4/6/8 channels data out for I2S
  - Support compress data format for SPDIF
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the on-chip CODEC
  - Support off-chip CODEC
  - Support off-chip HDMI transmitter audio
- Two PCM interfaces
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM: Short frame sync mode, Long frame sync mode, Multi-slot mode
  - Data is transferred and received with the MSB first
  - Support master mode and slave mode
  - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
  - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK.
  - 8/16 bit sample data sizes supported

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- DMA transfer mode supported
- Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction

- SADC
  - 12-bit, 1Msps/200ksps
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage inputs for internal/external resistor divider respectively
  - 2 generic input channels
  - 5mW@1Msps, 2.2mW@200ksps

1.2.8 On-chip Peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is ???, where ? are dedicated and all others are shared
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up/down on or off
- Three I2C bus interfaces
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- Two Synchronous serial interfaces (SSI0, SSI1)
  - Up to 50MHz speed
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode
- One-wire bus interface
  - Overdrive and regular speed
  - Master only
  - LSB first
  - Bit or byte operate modes
- USB 1.1 host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible
  - Full speed and low speed

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- Embedded USB 1.1 PHY

- USB 2.0 OTG interface
  - Compliant with USB protocol revision 2.0 OTG
  - High speed and full speed supported for device role
  - High speed, full speed and low speed supported for host role
  - Embedded USB OTG PHY
- Ethernet MAC interface
  - Compliant with IEEE802.3
  - 10/100 Mbps data transfer rate with full and half duplex modes
  - MII/RMII interface to talk to an external PHY
- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
  - Support automatic boot up from MSC0, which has 4-bit data bus
  - MSC1 with 4-bit data bus
  - Compliant with "The MultiMediaCard System Specification version 4.2"
  - Compliant with "SD Memory Card Specification version 2.0" and "SDIO Card Specification version 1.0" with 1 command channel and 4 data channels
  - Up to 320 Mbps data rate in MSC0
  - Up to 320 Mbps data rate in MSC1
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- Five UARTs (UART0, UART1, UART2, UART3, UART4)
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 32x8bit FIFO for transmit and 32x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 3.7Mbps baudrate
  - Hardware flow control
- SIM IF
  - Supports normal card and UIM card
  - 8-bit, 16-level receive-/transmit- FIFO
  - Supports asynchronous character (T=0) communication modes
  - Supports asynchronous block (T=1) communication modes
  - Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.)
  - Supports extra guard time waiting
  - Auto-error detection in T=0 receive mode
  - Auto-character repeat in T=0 transmit mode
  - Transforms inverted format to regular format and vice versa
  - Support stop clock function in some power consuming sensitive applications

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- Transport stream slave interface
  - 8-bit or 1-bit data bus selectable
  - Support PID filtering
- OTP Slave Interface
  - Total 256 bits. Lower 128bits are read-able and write-able, Higher 128bits are read only

1.2.9 Bootrom

- 8kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	65nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for mDDR: 1.8V± 0.2V DDR I/O for DDR: 2.5V± 0.2V DDR I/O for DDR2: 1.8V± 0.2V RTC I/O: 3.0V~3.6V EFUSE programming: 2.5V± 10% Analog power suppy 1: 2.5V± 10% Analog power suppy 2: 3.3V± 10% Core: 1.2 -0.1/+0.2 V
Package	BGA379 14mm x 14mm x 1.1mm, 0.65mm pitch
Operating frequency	1000MHz

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2 CPU Core

Enhanced features of CPU core include:

- Enhanced MXU implements XBurst SIMD instruction set release I and release II
- Full implementation of MIPS32 integer instruction release II
- TCSM, tightly coupled shared memory with physical address scope 0x132B0000 ~ 0x132BFFFF
- PMON, processor performance monitor
- FPU, floating point unit implemented to improve floating point number processing ability
- Unified level 2 cache that is transparent for programmer

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2.1 Block Diagram

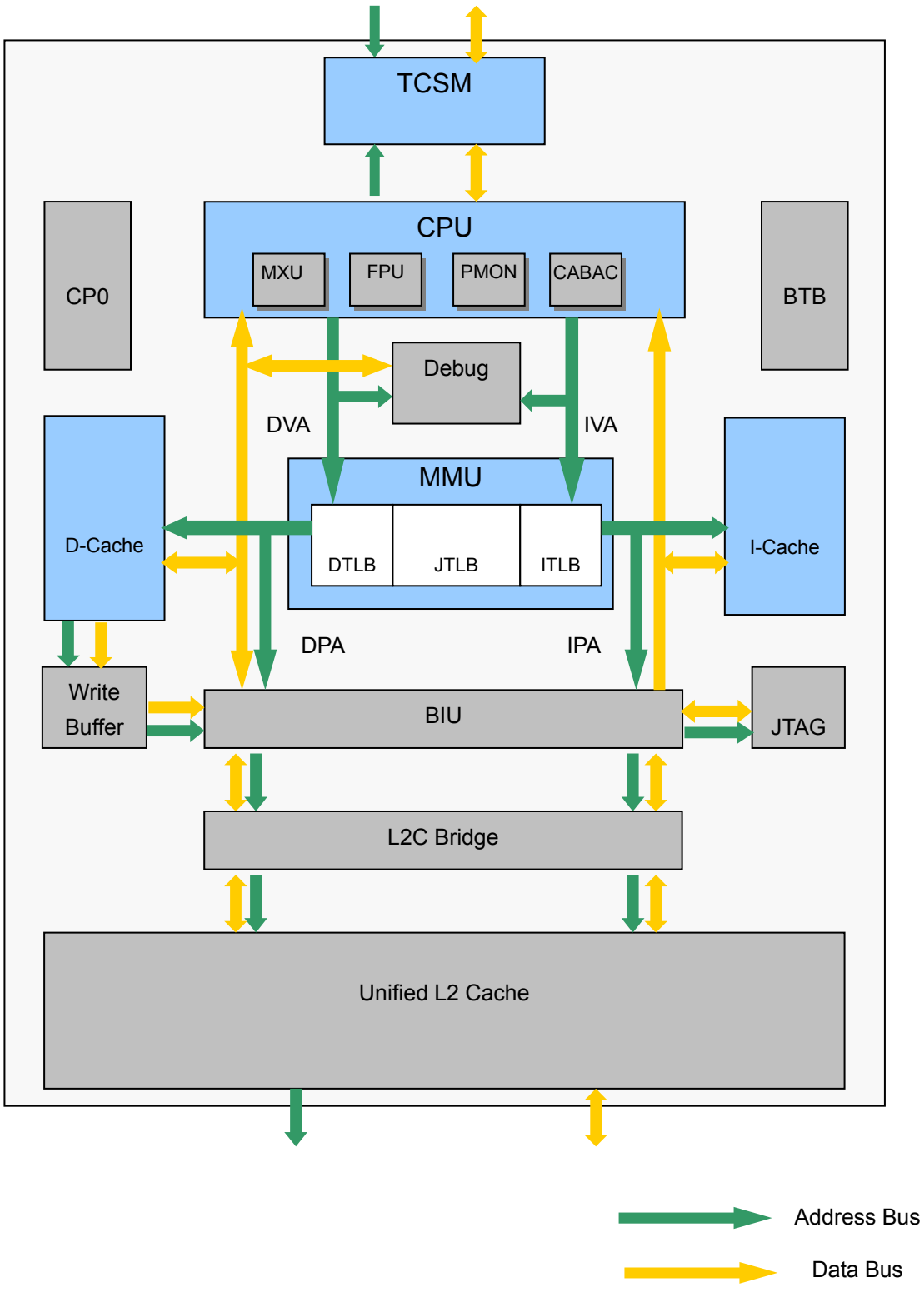


Figure 2-1 Structure of CPU core

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2.2 Extra Features of the CPU core

Item	Features
Media Extension Unit (MXU)	• XBurst SIMD instruction set release I and release II • fully pipelined
Integer Unit with MIPS32 integer instruction release II	• non full pipelined implementation for most of MIP32 integer instruction release II, need 2 ~ 4 interlock cycles
Tightly Coupled Sharing Memory (TCSM)	• Size: 16K bytes • Same clock frequency as L1 cache • AHB slave interface • Four banks support up to four simultaneous accesses
Floating Point Unit (FPU)	• Comply with IEEE754 standard • Support single and double format • not fully pipelined implementation
CABAC interface	• Part of bitstream processing cooperating CABAC in VPU • Dedicated CP0 interface is CP0 register number 21, select0~7
Performance Monitor (PMON)	• Real-time monitor • Dedicated CP0 interface
Unified Level 2 Cache	• Size: 256K bytes • 4 way set association with LRU replacement • Write from Level 1 data cache always write through to memory • Programmer transparent, that is, those CACHE instructions managing L1 cache can manipulate L2 cache automatically
Processor ID	Value read from CP0.PRId is 0x2ed1024f

Please refer to documents XBurst-ISA and XBurst1_PM for ISA and programming relative details.

2.3 Instruction Cycles

Most instructions have one cycle repeat rate, that is, when the pipeline is fully filled, there is one instruction issued per clock cycle. However, some particular instructions require extra cycles. Following table lists cycle consumption of all instructions belonging to XBurst-ISA implemented.

1st Instruction	2nd Instruction	Cycles	Description
WAIT	**Anyone**	variable	WAIT instruction will be repeatedly executed until an interrupt arise.
MTC0 **TLBWI/TLBWR** **TLBP/TLBR**	**Anyone**	4	3 extra interlock cycles.
CACHE	**Anyone**	2	1 extra interlock cycles.
JMP/BC	**Anyone** **(delay slot)**	4/1	0 cycle penalty when BTB predicts taken and the branch is taken or BTB predicts

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			untaken and the branch is untaken or BTB miss and the branch is untaken. Otherwise, extra 3 cycles penalty.
BCL	**Anyone (delay slot)**	5/4/2/1	0 cycle penalty when BTB predicts taken and branch is taken, otherwise: 1 BTB miss, branch is taken, 3 cycles penalty. 2 BTB miss, branch is untaken, 1 cycle penalty. 3 BTB predict taken, branch is untaken, 4 cycles penalty. 4 BTB predict untaken, branch is taken, 3 cycles penalty.
MULT/MULTU MADD/MADDU MSUB/MSUBU	**MULT/MULTU MADD/MADDU MSUB/MSUBU**	4	3 extra interlock cycles due to MDU operating hazard.
	MUL/DIV/DIVU	4	3 extra interlock cycles due to MDU operating hazard.
	MFHI/MFLO MTHI/MTLO	4	3 extra interlock cycles due to MDU operating hazard.
	Any other	1	No data dependency or hazards exist.
MUL	**MULT/MULTU MADD/MADDU MSUB/MSUBU**	4	3 extra interlock cycles due to MDU operating hazard.
	MUL/DIV/DIVU	4	3 extra interlock cycles due to MDU operating hazard.
	MFHI/MFLO MTHI/MTLO	4	3 extra interlock cycles due to MDU operating hazard.
	Any other	4/1	If the second instruction has RAW data dependency, 3 extra interlock cycles, otherwise, 0 cycle penalty.
DIV/DIVU	**MULT/MULTU MADD/MADDU MSUB/MSUBU MUL/DIV/DIVU**	4~35	3~34 extra interlock cycles determined by characteristic value of divider and dividend.
	MFHI/MFLO	2~34	1~33 interlock cycles determined by characteristic value of divider and dividend.
	Any other	1	No data dependency or hazards exist.
MFHI/MFLO/MFC0	**Anyone**	4/1	If the second instruction has RAW data dependency, 3 extra interlock cycles, otherwise, 0 cycle penalty.
LW/LL	**Anyone**	4/1	If the second instruction has RAW data

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LWL/LWR **LB/LBHU** **LH/HU** **LXW** **LXH/LXHU** **LXB/LXBU**			dependency, 3 extra interlock cycles, otherwise, 0 cycle penalty.
D16MUL/D16MULF **D16MAC/D16MACF** **D16MULE/D16MACE**	**SIMD instruction**	3/1	If the second SIMD instruction has RAW data dependency, 2 extra interlock cycles, otherwise, 0 cycle penalty.
	Any other	1	No data dependency or hazards exist.
D32ACC/Q16ACC **Q8SAD** **S32MAX/S32MIN** **D16MAX/D16MIN** **D32ACCM/D32ASUM** **Q16ACCM/D16ASUM**	**SIMD instruction**	2/1	If the second SIMD instruction has RAW data dependency, 1 extra interlock cycle, otherwise, 0 cycle penalty.
	Any other	1	No data dependency or hazards exist.
S32LDD/S32LDDV **S32LDI/S32LDIV** **S32LDDR/S32LDDVR** **S32LDIR/S32LDIVR** **S16LDD/S16DI** **S8LDD/S8LDI**	**SIMD instruction**	2/1	If the second SIMD instruction has RAW data dependency, 1extra interlock cycle, otherwise, 0 cycle penalty.
	Any other	1	No data dependency or hazards exist.
S32I2M	**SIMD instruction**	2/1	If the second SIMD instruction has RAW data dependency, 1extra interlock cycle, otherwise, 0 cycle penalty.
	Any other	1	No data dependency or hazards exist.
S32M2I	**Anyone**	4/1	If the second instruction has RAW data dependency, 3 extra interlock cycles, otherwise, 0 cycle penalty.
S32EXTR **S32EXTRV**	**SIMD instruction**	2/1	If the second SIMD instruction has RAW data dependency, 1extra interlock cycle, otherwise, 0 cycle penalty.
	Any other	1	No data dependency or hazards exist.
Others	**Anyone**	1	

NOTE: JMP denotes J and JR instructions; BC denotes branch conditionally instructions; BCL denotes branch conditionally and likely instructions.

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2.4 TCSM

TCSM (tightly coupled shared memory) is a dedicated on-chip SRAM. It serves as an on-chip scratchpad memory, moreover, it acts as a high-speed SRAM for CPU. Through the TCSM, CPU and VPU's AHB masters such as DBlock can exchange data quickly and efficiently. TCSM in the CPU core has following features:

- 16K bytes
- The same clock frequency as L1 cache
- Physical address scope from 0x132B,0000 to 0x132B,FFFF
- Four banks support up to four simultaneous accesses if no bank conflicts occurs

Moreover, like the **dseg** section separated from K3 section, another **tcsm** section with 16MB capacity range from 0xF400,0000 to 0xF4FF,FFFF is separated too. This virtual address section is uncacheable and unmappable and can only be accessed by CPU core in kernel mode.

Please note the fact that the capacity of TCSM is only 16K bytes, which denotes that available virtual address range is from 0xF400,0000 to 0xF400,3FFF and available physical address range is from 0x132B,0000 to 0x132B,3FFF.

2.4.1 TCSM Occupied Available Physical Address Range

Physical Address range 0x132B,0000 ~ 0x132B,FFFF are reserved for TCSM. Physical address range 0x132B,0000 ~ 0x132B,3FFF are available and others are reserved, and corresponding address partition for the four banks are as following:

bank0: 0xF4000000~0xF4000FFF (virtual); 0x132B,0000~0x132B,0FFF (physical)
bank1: 0xF4001000~0xF4001FFF (virtual); 0x132B,1000~0x132B,1FFF (physical)
bank2: 0xF4002000~0xF4002FFF (virtual); 0x132B,2000~0x132B,2FFF (physical)
bank3: 0xF4003000~0xF4003FFF (virtual); 0x132B,3000~0x132B,3FFF (physical)

Therefore, arranging instructions and data into different banks can achieve best access performance. Similarly, using ping-pong buffers located in the separate banks for efficient data exchange between CPU core and other VPU's AHB masters is a better choice.

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2.5 PMON

PMON is a simple performance monitor. Following performance relative real-time events can be monitored.

- I-cache miss times
- D-cache miss times
- Total issued instructions
- Discarded instructions
- Pipeline freeze cycles
- CPU clock cycles

A dedicated software interface is devised to manipulate PMON in kernel mode, that is, CP0 Config4 ~ Config7 registers are extended for PMON. Refer to chapter of CP0 in the document XBurst1_PM for detail.

2.5.1 Fundamental

When PMON is enabled (set value 1 to config7.bit8), one preset event pair determined by config7.bit15~bit12 will be continuously monitored until PMON is disabled (set value 0 to config7.bit8). Finally, loading values of CP0.config4~CP0.config6 can get monitored result.

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3 VPU Core

Video Processing Unit (VPU) core in this chip is dedicated for video decoding and encoding. VPU embeds an XBurst® CPU core (named AUX in VPU) and application specified hardware accelerators for common video compress/decompress algorithms, which includes Stream Parser, Motion Compensation, Motion Estimation, Quant/Inverse Quant, DCT/Inverse DCT and De-block engines. Further more 3 route general purpose DMA enhances data management and transfer efficiency during video encoding/decoding.

XBurst® core's powerful programming agility combining with specified algorithm accelerators' high hotspot processing ability ensures VPU's multi format supporting and high performance ability. This distinctive structure brings us a nice trade-off of DSP's high power consumption and low processing ability with Hardware IP's complicated large logic size and limited format supporting.

Key standards performance of VPU in the chip:

- RealVideo decoding up to 1080P 30fps
- MPEG-2 decoding up to 1080P 30fps
- MPEG-4 decoding up to 1080P 30fps
- VC-1 decoding up to 1080P 30fps
- H.264 decoding up to 1080P 30fps
- H.264 encoding up to 720P 30fps

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3.1 Block Diagram

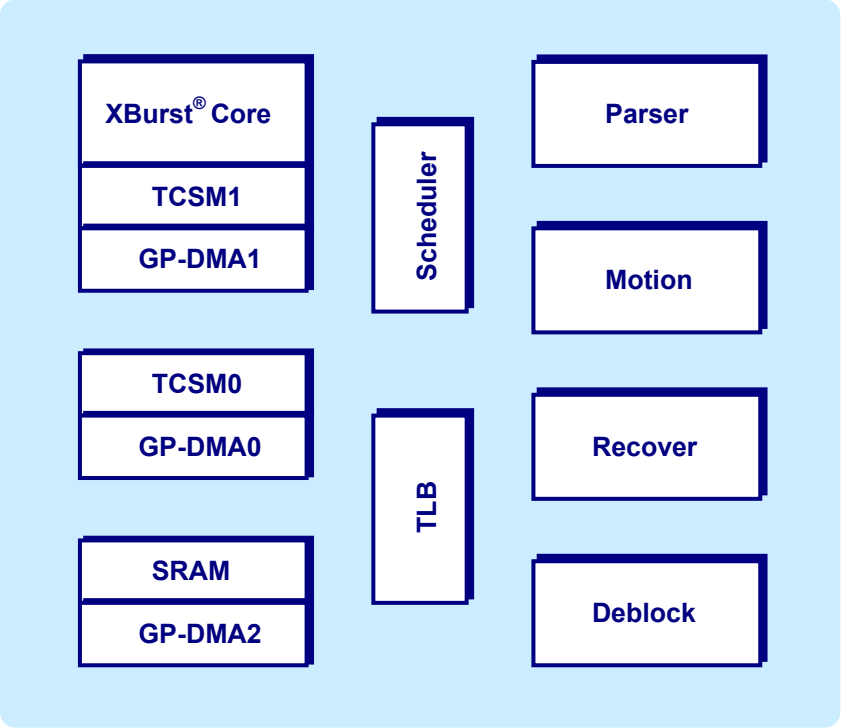


Figure 3-1 VPU Block DiagramFeatures of VPU

Table 3-1 VPU Features

Item	Features
XBurst® core(AUX)	● XBurst-1 CPU – Industry standard RISC instruction set – 32 32-bit general purpose registers, no shadow GPR – Physical address accessing directly ● Media Extension Unit (MXU) – Ingenic SIMD instruction set II – fully pipelined
Tightly Coupled Sharing Memory (TCSM)	● TCSM0 – Size: 16K bytes – AHB slave interface supports external DMA access ● TCSM1 – Size: 48K bytes – AHB slave interface supports external DMA access **NOTE:** TCSM0 is coupled with J1 externally and serves as a memory interface for VPU, while TCSM1 is coupled with VPU XBurst® core

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	internally.
Scratch RAM (SRAM)	● Size: 28K bytes ● AHB slave interface supports external DMA access
Gerenal Purpose DMA(GP_DMA)	● GP_DMA0/GP_DMA1/GP_DMA2 – Descriptor based DMA **NOTE:** GP_DMA0/GP_DMA1 is coupled with TCSM0/TCSM1 and GP_DMA2 is coupled with SRAM as well.
Parser (SDE)	Parser is a stream decode engine (named as SDE) in VPU ● Context adaptive binary arithmetic (CABAC) decoding support ● Context adaptive variable length (CAVLC) decoding support ● Programmable VLC table support for Gerenal Purpose VLC decoding accelerating
Motion (MCE)	Motion serves as a COMBO engine of compensation and estimation (named as MCE) in VPU ● Reference data cache embed ● Descriptor based task fetching ● Programmable processing size from 2x2 to 16x16 (in estimation the size is from 4x4 to 16x16) ● Programmable interplation filter from 2-tap to 8-tap ● Programmable sub-pixel accuracy from 1/2-pixel to 1/8-pixel (in estimation searching accuracy is supported from integer to 1/4-pixel) ● Interlaced mode support ● Intensity compensation support ● Weighted prediction support ● Automatic rotation support for rotated referenced pictures ● Automatic expanding support for outside frame's reference ● Configurable searching strategy in estimation
Recover (VMAU)	Recover is a Matrix Arithmetic Unit in VPU (named as VMAU), it serves for pixel's recovery and reconstruction during vedio decoding and encoding. ● Descriptor based task fetching ● Configurable format intra prediction support ● Configurable format Inverse quant support ● Configurable format IDCT support ● Residual add for pixel's recovery ● Estimation subtract and pixel reconstruction in encoding flow
Deblock (DBLK)	● Descriptor based task fetching ● Dual-channel embeded (named as DBLK1 and DBLK2) ● RealVideo in loop filter support ● H.264 in loop filter support, MBAFF not support
Scheduler (SCH)	Scheduler is a special unit which is used to manage internel functional engines' handshake.

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	• 4 programable channels
Translation look-aside buffer (TLB)	• 8-entry based full associated • Configurable page size

3.2 Internal physical address base definition

Table 3-2 VPU Internal physical address base definition

Module	Physical address base
AUX	0x132A_0000
TCSM0	0x132B_0000
GP_DMA0	0x1321_0000
TCSM1	0x132C_0000
GP_DMA1	0x1322_0000
SRAM	0x132F_0000
GP_DMA2	0x1323_0000
MCE	0x1325_0000
VMAU	0x1328_0000
DBLK1	0x1327_0000
DBLK2	0x132D_0000
SDE	0x1329_0000
SCH/TLB	0x1320_0000

3.3 AUX

3.3.1 Register Definition

3.3.1.1 Control and Status

AUX_CTRL **0x0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLEEP	Reserved																						BTB_INV	Reserved				MIRQ_EN	NMI_DIS	SW_NMI	SW_RST
RST	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31	SLEEP	AUX sleep status. 1: sleep; 0: no sleep.	R
30:9	Reserved	Writing has no effect, read as zero.	R
8	BTB_INV	Writing 1 can invalid BTB. Writing 0 has no effect, read as zero.	W

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7:4	Reserved	Writing has no effect, read as zero.	R
3	MIRQ_EN	1: enable message IRQ. 0: disable.	RW
2	NMI_DIS	1: NMI only wakes up AUX from sleep status 0: NMI wakes up AUX and switch PC to 0xF4000000	RW
1	SW_NMI	Nonmaskable IRQ (NMI). Writing 1 to the field triggers a NMI pulse to AUX. Writing 0 has no effect, read as zero.	W
0	SW_RST	Software reset. 1: let AUX keep at reset status; 0: do not reset.	RW

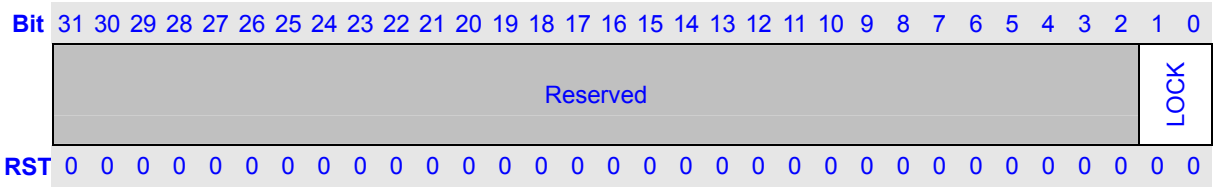
NOTES:

1 When NMI or IRQ or RESET exception occurs, AUX resumes from PC 0xF4000000.

2 When AUX wakes up by an NMI meanwhile NMI_DIS is 1, AUX just resumes from the next PC of the WAIT instruction.

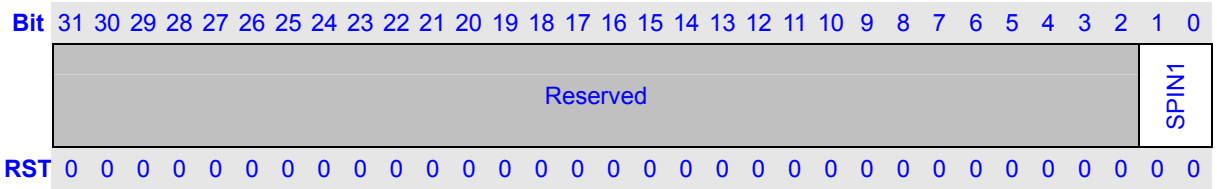
3.3.1.2 SPINLOCK

AUX_SPINLK **0x4**



Bits	Name	Description	R/W
30:2	Reserved	Writing has no effect, read as zero.	R
1:0	LOCK	Lock status.	RW

AUX_SPIN1 **0x8**



Bits	Name	Description	R/W
30:2	Reserved	Writing has no effect, read as zero.	R
1:0	SPIN1	Reading SPIN1 triggers following special hardware operations. First, value of AUX_SPINLK will be checked, if the value equals zero, the value of SPIN1 will overwrite AUX_SPINLK immediately, otherwise, AUX_SPINLK keeps unchanged. Then reading AUX_SPINLK instead of SPIN1 supplies the final read result. Writing SPIN1 is a normal write operation.	RW

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AUX_SPIN2 **0xC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														SPIN2	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
30:2	Reserved	Writing has no effect, read as zero.	R
1:0	SPIN2	The operations for SPIN1 also fit SPIN2 except the role of SPIN1 should be replaced by SPIN2.	RW

AUX_MIRQP **0x10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															MIRQP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	MIRQP	Pending status of MIRQ (message IRQ to CORE) which can only be set to 1 by HW and be reset to 0 by SW. This pending IRQ is routing to main CPU core.	RW

AUX_MSG **0x14**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MESG																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	?	0	0

Bits	Name	Description	R/W
31:0	MESG	If AUX_CTRL.MIRQ_EN is value 1, writing the register raises an IRQ routing to the main CPU core meanwhile the AUX_MIRQP is set to 1 by HW automatically. The IRQ then keeps active until the register AUX_MIRQP is cleared to 0 by SW.	RW

CORE_MIRQP **0x18**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															MIRQP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	MIRQP	Pending status of MIRQ (message IRQ to AUX) which can only be set 1 by HW and be clear to 0 by SW. This pending IRQ is routing to AUX.	RW

CORE_MSG **0x1C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MESG																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MESG	If AUX_CTRL.MIRQ_EN is value 1, writing the register raises an IRQ routing to the AUX. The IRQ then keeps active until the register CORE_MIRQP is cleared to 0 by SW.	RW

3.4 TCSM/SRAM

TCSM0/TCSM1/SRAM serves as the VPU control flow and data flow's communication between XBurst® CPU core with specified algorithm hardware accelerators and different hardware accelerators as well.

3.4.1 TCSM/SRAM space usage

Table 3-3 TCSM space usage

	XBurst® J1	XBurst® AUX	HW accelerator
TCSM0	0xF400_0000 ~ 0xF400_3FFF	0x132B_0000 ~ 0x132B_3FFF	0x132B_0000 ~ 0x132B_3FFF
TCSM1	0x132C_0000 ~ 0x132C_BFFF	0xF400_0000 ~ 0xF400_BFFF	0x132C_0000 ~ 0x132C_BFFF
SRAM	0x132F_0000 ~ 0x132F_6FFF	0x132F_0000 ~ 0x132F_6FFF	0x132F_0000 ~ 0x132F_6FFF

NOTES:

1 TCSM1/SRAM's space list for XBurst® J1 is physical address. In actual using it must be translated to its relative virtual address for XBurst® J1's accessing.

2 XBurst® J1 can not access SRAM with VPU internal masters simultaneously.

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3.5 GP_DMA

3.5.1 Overview

GP_DMA is a 2-D data transfer DMA controller, which is tightly coupled with TCSM0/TCSM1/SRAM. Due to this tightly coupling, the data path for transferring should be limited as the following:

Table 3-4 GP_DMA data transfer path

GP_DMA	Validity of data transfer path
GP_DMA0	From other slavers except SRAM to TCSM0 is valid From TCSM0 to other slavers except SRAM is valid From TCSM0 to TCSM0 is forbiden
GP_DMA1	From other slavers except SRAM to TCSM1 is valid From TCSM1 to other slavers except SRAM is valid From TCSM1 to TCSM1 is forbiden
GP_DMA2	From other slavers to SRAM is valid From SRAM to other slavers is valid From SRAM to SRAM is forbiden

GP_DMA is working under descriptor-based configuration. Its descriptor node is defined as:

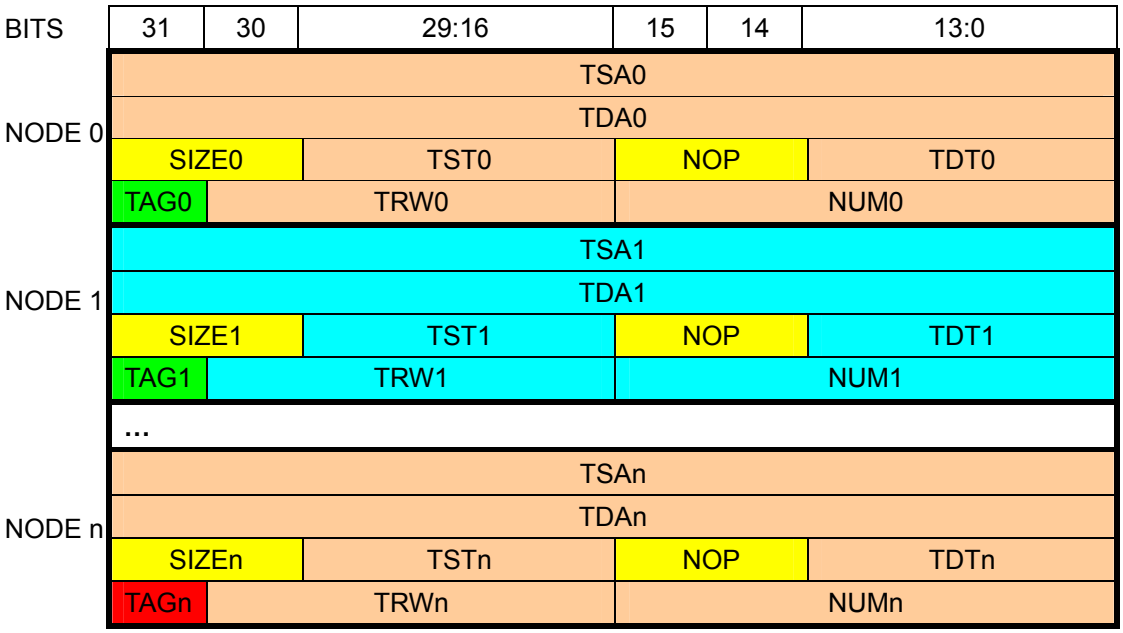


Figure 3-2 GP_DMA descriptor node structure

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Table 3-5 GP_DMA descriptor node description

Item	Meaning
TSA	transfer source ADDRESS.
TDA	transfer destination ADDRESS.
TST	transfer source STRIDE.
TDT	transfer destination STRIDE.
TRW	transfer row WIDTH.
NUM	transfer byte NUMBER.
SIZE	transfer size type. 0: word 1: byte 2: half-word
TAG	Transfer link end tag. (GP_DMA parses each node to do data transfer and then go on parsing next adjacent node until it accomplishes a node with TAG equaling 1)

3.5.2 Register Definition

3.5.2.1 Descriptor Head Address (DHA)

DHA 0x0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DHA																														Reserved	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0

Bits	Name	Description	RW
31:2	DHA	Descriptor Head Address.	RW
1:0	Reserved	Writing has no effect, read as zero.	R

3.5.2.2 DMA Status/Command (DCS)

DCS 0x4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BTN																NDN								Reserved						END	RST	SUP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	BTN	Transfer number byte.	R
15:8	NDN	Transfer node number.	R
15~3	Reserved	Writing has no effect, read as zero.	R
2	END	0: GP_DMA in transferring 1: transmit end, GP_DMA is idle	R
1	RST	GP_DMA SW reset. GP_DMA would be reset when it was written as 1.	RW
0	SUP	GP_DMA startup.	RW

3.6 Video Acceleration Block

Please refer to relative programming manual documents.

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4 GPU Core

4.1 Overview

Today's consumer devices feature rich, graphical user interfaces and run interactive applications like games and mobile web tools. GPU defines a family of high-performance cores that deliver hardware acceleration for 2D and 3D graphics displays on these devices. Addressable screen sizes range from the smallest cell phones to full HD 1080p displays.

GPU provides high performance, high quality graphics, low power consumption, and the smallest silicon footprint in every class. Dynamic power consumption is minimized by extensive use of multi-level hierarchical clock gating. The design also includes a 32-bit AHB interface, a 64-bit AXI interface, and support for virtual memory.

GPU accelerates numerous 2D and 3D graphics applications, including graphical user interfaces (GUI) and menu displays, Flash animation, and gaming, and it is a perfect fit for popular consumer devices like cell phones and smartphones, digital picture frames (DPF), digital signage, portable and in-dash GPS navigation systems, mobile internet devices (MID) and netbooks, handheld gaming consoles, set-top boxes, and HDTV.

An optimized software stack, complete software development tools, and a growing application ecosystem are supported by a robust graphics pipeline designed for industry-standard APIs, and with full support for Android, Linux, and Windows embedded development platforms. GPU supports the following graphics APIs:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1
- DirectFB
- GDI/DirectDraw

4.2 Design Features

GPU includes a 32-bit AHB interface for register accesses and a 64-bit AXI interface for external memory accesses. It also includes virtual memory support. The following table describes the full feature set of GPU.

4.2.1 GPU Architecture Features

FEATURE	GPU Support
Primary API	OpenGL ES 1.1 and 2.0.

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Additional APIs	OpenVG 1.1. DirectFB. GDI. DirectDraw.
Other graphics support	EGL 1.4.
Drivers	OpenGL ES 1.1 and 2.0. OpenVG 1.1. DirectFB. EGL. GDI/DirectDraw.
Operating systems	Windows CE. Linux. Embedded Android.
Z (depth)	Early Z support included.
Stencil	Early stencil support included.
Shader languages	GLSL ES 1.0.
Shader model compatibility	Shader model 3.0.
Shader types and execution units	One (1) programmable Scalable Ultra-threaded Unified Shader. (SIMD4:transcendental,ctl-flow,tx-load) One instruction issue per shader per clock; IEEE 32-bit floating-point pipeline supports long shader instructions.
FSAA anti-aliasing mechanisms	High quality MSAA 4x; MSAA 16x for OpenVG.
Code and data memory location restrictions	Unrestricted; arbitrary memory reads and writes.
Physical address	31 bits.
MMU description	32-bit virtual address; 4 kB pages, error reporting outside of address space.
TLB	4 cache lines per requestor.
Resource locks with CPU	Semaphore lock.
Max memory latency without a performance hit	128 GPU cycles.

4.2.2 GPU Command Processor Features

FEATURE	GPU Support
Command list structure	Linked memory buffer.
Branches	1-cycle; no penalty for dynamic branching.
GPU register access	AHB access to selected GPU registers.
GPU-CPU synchronization	Synchronization occurs via event queues.
Command buffering included in GPU IP	512 bytes; 64 words x 64 bits each.

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Index buffer and vertex cache	512-byte index buffer; 1 kB vertex cache.
Set render state	One 32-bit register per cycle, 1-cycle throughput.
Set render target	One 32-bit register per cycle, 1-cycle throughput.
Set texture	One 32-bit register per cycle, 1-cycle throughput.
Set texture sampler	One 32-bit register per cycle, 1-cycle throughput.
Draw primitive	5-cycle throughput minimum; actual throughput depends on the number of vertices.
Draw indexed primitive	7-cycle throughput minimum; actual throughput depends on the number of vertices.
Counters	Variety of hardware counters for performance profiling.

4.2.3 Power Management Features

FEATURE	GPU Support
Low power CMOS technology compatible	Yes.
Automatic clock gating of flip flops and rams	Yes.
Global clock gating of unused macro blocks	Yes.
Software controlled effective clock frequency without changing the PLL	Yes.

4.2.4 GPU 2D Hardware Features

The features of the dedicated 2D unit are shown in the following table. These features include:

- Bit BLT and stretch BLT
- Rectangle fill and clear
- Line drawing
- High-performance stretch and shrink
- Monochrome expansion for text rendering
- ROP2, ROP3, ROP4
- Alpha blending including Java 2 Porter-Duff compositing blending rules
- 32k x 32k coordinate system
- 90, 180, and 270 degrees rotation
- Transparency by monochrome mask, chroma key, or pattern mask

FEATURE	GPU Support
Programmable Ops	ROP2, ROP3, ROP4 full alpha blending and transparency.
Fixed function	Line draw, Rectangle fill, Clear, Bit blit, Stretch blit, Filter blit.
Blit support	Copy (Bit), Filter, Monochrome Mask, Stretch/Shrink.
Source formats	RGBA4444/ 5551/ 8888, RGBX4444/ 5551/ 8888, RGB565, A8, UYVY(4:2:2), YUY2(4:2:2), YV12(4:2:0), 8-bit color index, NV12(4:2:0), NV16(4:2:2).
Destination formats	RGBA4444/ 5551/ 8888, RGBX4444/ 5551/ 8888, RGB565.

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Alpha blending modes	Java2 Porter-Duff, Chroma Key, Pattern Mask.
Image scaling	Programmable high quality 9-tap, 32-phase filter.
Rotation	90 / 180 / 270 degrees on every 2D primitive.
Text rendering	Monochrome expansion; support for anti-aliased A8 fonts.
Alpha blend, scale, and rotation operations	Blending, scaling, and rotation are supported in one pass for stretch BLT.
Video	Video scaling and format conversion only.
Power for 2D vs. 3D doing 2D operations	Up to 90% less power required for dedicated 2D functions.
Rendering size	32k x 32k raster 2D coordinate system.

4.2.5 GPU 3D Hardware Features

The features of the GPU 3D unit are shown in the following table. These features include:

- OpenGL ES 2.0 compliance, including extensions; OpenGL ES 1.1; OpenVG 1.1
- IEEE 32-bit floating-point pipeline
- Ultra-threaded, unified vertex and fragment shaders
- Low bandwidth at both high and low data rates
- Low CPU loading
- Up to 12 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Depth and stencil compare
- Support for 8 fragment shader simultaneous textures
- Support for 4 vertex shader simultaneous textures
- Point sampling, bi-linear sampling, tri-linear filtering, and cubic textures
- Resolve and fast clear
- 8k x 8k texture size and 8k x 8k rendering target

Unified vertex-fragment shader:

FEATURE	GPU Support
Shader type and execution units	Unified shader, SIMD4, SFP32 Trans.
Swizzle capabilities	Full 32-bit word level swizzle in a 128-bit vector.
GPR's per shader	Up to 512 general purpose registers, 128 bits each.
Uniform registers	Vertex Shader: 160 registers, 128 bits each. Fragment Shader: 64 registers, 128 bits each.
FP denorm and rounding options	Denorms are set to zero. Supports rounding to zero.
Maximum number of data input attributes	Maximum of 12 vertex shader input elements; maximum of 8 fragment shader input elements.
Maximum number of instructions	256 for vertex shaders; 256 for fragment shaders.
Maximum number of vertex streams	1.

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Maximum number of threads in flight	256.
Subroutines	4 levels.
Conditional branch support	GT, LT, EQ, GE, LE, NE.
Shader instruction rate	1-cycle throughput for all shader instructions.
Floating-point instruction precision	Transcendental: 22 bits SIMD4 (vector): 23.5 bits.
Fragment shader video	Supports video texture.

Vertex Processing:

FEATURE	GPU Support
Vx D3D, OGL ES formats supported	BYTE, UBYTE, SHORT, USHORT, INT, UINT, DEC, UDEC, FLOAT, FLOAT16, D3DCOLOR, FIXED16DOT16.
Vertex data size limits	256 bytes.
Pre shader cache	1 Kb.
Post shader cache	8 vertices.

Primitive Processing:

FEATURE	GPU Support
Primitives supported	Triangle strip, fan, and list; line strip and list; point list.
Vertex/primitive geometry input index sizes	8-bit ,16-bit and 20-bit indices.
Setup parameters available to fragment shader	8 vec4 parameters; all available to fragment shader.

Texture Processing:

<table>
<tr><td>FEATURE</td><td>GPU Support</td></tr>
<tr><td>Fixed-point input texture formats</td><td>A8, L8, I8, A8L8, ARGB4, XRGB4, ARGB8, XRGB8, ABGR8, XBGR8, R5G6B5, A1RGB5, X1RGB5, YV12, YUY2, UYVY, D16, D24X8, A8_OES, DXT1, DXT2, DXT3, DXT4, DXT5, ETC1; all fixed-point formats are filtered.
<table>
<tr><td>Bits</td><td>Format</td><td>R</td><td>G</td><td>B</td><td>Alpha</td></tr>
<tr><td>16</td><td>ARGB4444</td><td>4</td><td>4</td><td>4</td><td>4</td></tr>
<tr><td>16</td><td>XRGB4444</td><td>4</td><td>4</td><td>4</td><td>4 don’t care</td></tr>
<tr><td>16</td><td>ARGB1555</td><td>4</td><td>4</td><td>4</td><td>1</td></tr>
<tr><td>16</td><td>XRGB1555</td><td>4</td><td>4</td><td>4</td><td>1 don’t care</td></tr>
<tr><td>16</td><td>RGB565</td><td>5</td><td>6</td><td>5</td><td>0</td></tr>
<tr><td>32</td><td>ARGB8888</td><td>8</td><td>8</td><td>8</td><td>8</td></tr>
<tr><td>32</td><td>XRGB8888</td><td>8</td><td>8</td><td>8</td><td>8 don’t care</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><td></td><td>
<table>
<tr><td>32</td><td>ABGR8888</td><td>8</td><td>8</td><td>8</td><td>8</td></tr>
<tr><td>32</td><td>XBGR8888</td><td>8</td><td>8</td><td>8</td><td>8 don’t care</td></tr>
</table>
<table>
<tr><th>Planes</th><th>Format</th><th>Mode</th><th>Y</th><th>U</th><th>V</th><th>UV</th><th>YUYV</th><th>UYVY</th></tr>
<tr><td>3</td><td>YV12</td><td>4:2:0</td><td>1</td><td>1</td><td>1</td><td></td><td></td><td></td></tr>
<tr><td>2</td><td>NV12</td><td>4:2:0</td><td>1</td><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>1</td><td>YUY2</td><td>4:2:2:</td><td></td><td></td><td></td><td></td><td>1</td><td></td></tr>
<tr><td>1</td><td>UYVY</td><td>4:2:2</td><td></td><td></td><td></td><td></td><td></td><td>1</td></tr>
</table>
</td></tr>
<tr><td>Texture compression</td><td>4 bits and 8 bits per texel.</td></tr>
<tr><td>Compressed texture formats</td><td>DXT1, DXT2, DXT3, DXT4, DXT5, ETC1.
All compressed formats are filtered.</td></tr>
<tr><td>Texture size maximum</td><td>8k x 8k.</td></tr>
<tr><td>Addressing modes</td><td>wrap, mirror, clamp.</td></tr>
<tr><td>Mipmap support</td><td>14 mipmap levels; programmable LOD biasing & replacement.</td></tr>
<tr><td>Shadow texture</td><td>Depth texture PCF filtering.</td></tr>
<tr><td>Texture cache organization</td><td>Tiled, 4x4 texels.</td></tr>
<tr><td>Texture cache size</td><td>32 cache lines, with 64 bytes per cache line;
total of 2 kB texture cache.</td></tr>
<tr><td>Texture coordinate fraction bits</td><td>5 bits.</td></tr>
<tr><td>Texture sampler units</td><td>12 samplers, indexable.</td></tr>
<tr><td>Textures per fragment maximum</td><td>8 texture samplers.</td></tr>
<tr><td>Dependent texture operation</td><td>High performance; unlimited dependent texture reads.</td></tr>
<tr><td>Dependent tx per fragment max, relative sampling</td><td>No limit.</td></tr>
<tr><td>Texture repeat max</td><td>256.</td></tr>
<tr><td>Texture types</td><td>2D, cube map, 1D, projected, depth, bump map, displacement map.</td></tr>
<tr><td>Texture filters</td><td>Point sample, bi-linear, tri-linear.</td></tr>
<tr><td>Texture component mapping: D3D, OGL ES options</td><td>Supports both D3D and OES options.</td></tr>
<tr><td>Texture size types</td><td>Power-of-2, Non-square texture support.</td></tr>
</table>

Rasterization:

FEATURE	GPU Support
Interpolant attributes	8.
Render target size	8k x 8k.
Clipping window	Clipping rectangle supported.
Early Z	Yes.

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Fragment Processing:

FEATURE	GPU Support
FSAA anti-aliasing mechanisms	High quality MSAA 4x; MSAA 16x for OpenVG.
Fragment color, alpha, Z, stencil precision	RGBA4444, RGBA5551, RGB565, RGBA8888, D16, D24, D24S8.
Fragment storage	16-bit color and Z, 32-bit color and Z for each fragment. Lossless compression, no storage reduction.
Alpha support	Individual fragment alpha masking.
Fragment cache	16 cache lines for color. 16 cache lines for Z. 64 bytes per cache line.

Dest/Alpha Blending:

FEATURE	GPU Support
Destination color formats	RGBA4444, RGBA5551, RGB565, RGBA8888.
Blend modes	Porter-Duff blending modes.
Dithering	Render target dithering support.

Z/Stencil Buffer:

FEATURE	GPU Support
Z/stencil formats	16-bit Z; 24-bit Z plus 8-bit stencil, with lossless compression support.
Z/stencil cache	16 cache lines; 64 bytes per line.
Stencil support	Both stencil and two-sided stencil.

Render Target:

FEATURE	GPU Support
Formats	16-bit and 32-bit, with lossless compression support.
RT buffer cache	16 cache lines; 64 bytes per line; RT caches are fully set associative.

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5 DDR Controller

5.1 Overview

DDRC (DDR Controller) is a general IP which provide an interface to DDR2, DDR, mobile DDR memory. The DDRC IP is designed for SOC usage and is configurable, scalable to meet the requirement of various SOC.

Features:

- Support DDR2, DDR, mobile DDR (LPDDR) memory
- Support x16 and x32 external DDR data width
- Support clock frequency ratio – (BUS clock) : (DDR clock) = 2:1
- Support clock frequency ratio – (BUS clock) : (DDR clock) = 1:1
- Support clock-stop mode
- Support auto-refresh and self-refresh
- Support power-down mode and deep-power-down mode
- Programmable DDR timing parameters
- Programmable DDR row and column address width

5.1.1 Supported DDR SDRAM Types

In the following table, the DDR memory types in green are supported by DDRC.
Row address width 15-bit or more & Column width 11 or more are not supported.

64Mb			
Configuration	16Mb x 4	8Mb x 8	4Mb x 16
Number of Banks	4	4	4
Row address width	12	12	12
Column address width	10	9	8
128Mb			
Configuration	32Mb x 4	16Mb x 8	8Mb x 16
Number of Banks	4	4	4
Row address width	12	12	12
Column address width	11	10	9
256Mb			
Configuration	64Mb x 4	32Mb x 8	16Mb x 16
Number of Banks	4	4	4
Row address width	13	13	13
Column address width	11	10	9

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512Mb			
Configuration	128Mb x 4	64Mb x 8	32Mb x 16
Number of Banks	4	4	4
Row address width	13	13	13
Column address width	12	11	10
1Gb			
Configuration	256Mb x 4	128Mb x 8	64Mb x 16
Number of Banks	4	4	4
Row address width	14	14	14
Column address width	12	11	10

5.1.2 Supported DDR2 SDRAM Types

In the following table, the DDR2 memory types in green are supported by DDRC.
All x4 (memory data width is 4-bit) devices are not supported.
Row address width 15-bit or more & Column width 11 or more are not supported.

256Mb			
Configuration	64Mb x 4	32Mb x 8	16Mb x 16
Number of Banks	4	4	4
Row address width	13	13	13
Column address width	11	10	9
512Mb			
Configuration	128Mb x 4	64Mb x 8	32Mb x 16
Number of Banks	4	4	4
Row address width	14	14	13
Column address width	11	10	10
1Gb			
Configuration	256Mb x 4	128Mb x 8	64Mb x 16
Number of Banks	8	8	8
Row address width	14	14	13
Column address width	11	10	10
2Gb			
Configuration	512Mb x 4	256Mb x 8	128Mb x 16
Number of Banks	8	8	8
Row address width	15	15	14
Column address width	11	10	10

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5.1.3 Supported LPDDR SDRAM Types

In the following table, the LPDDR memory types in green are supported by DDRC.
Row address width 15-bit or more & Column width 11 or more are not supported.

128Mb			
Configuration		8Mb x 16	4Mb x 32
Number of Banks		4	-
Row address width		12	-
Column address width		9	-
256Mb			
Configuration		16Mb x 16	8Mb x 32
Number of Banks		4	4
Row address width		13	12
Column address width		9	9
512Mb			
Configuration		32Mb x 16	16Mb x 32
Number of Banks		4	4
Row address width		13	13
Column address width		10	9
1Gb			
Configuration		128Mb x 16	64Mb x 32
Number of Banks		8	8
Row address width		14	13
Column address width		10	10

5.1.4 Block Diagram

Following figure shows the functional block diagram of DDRC.

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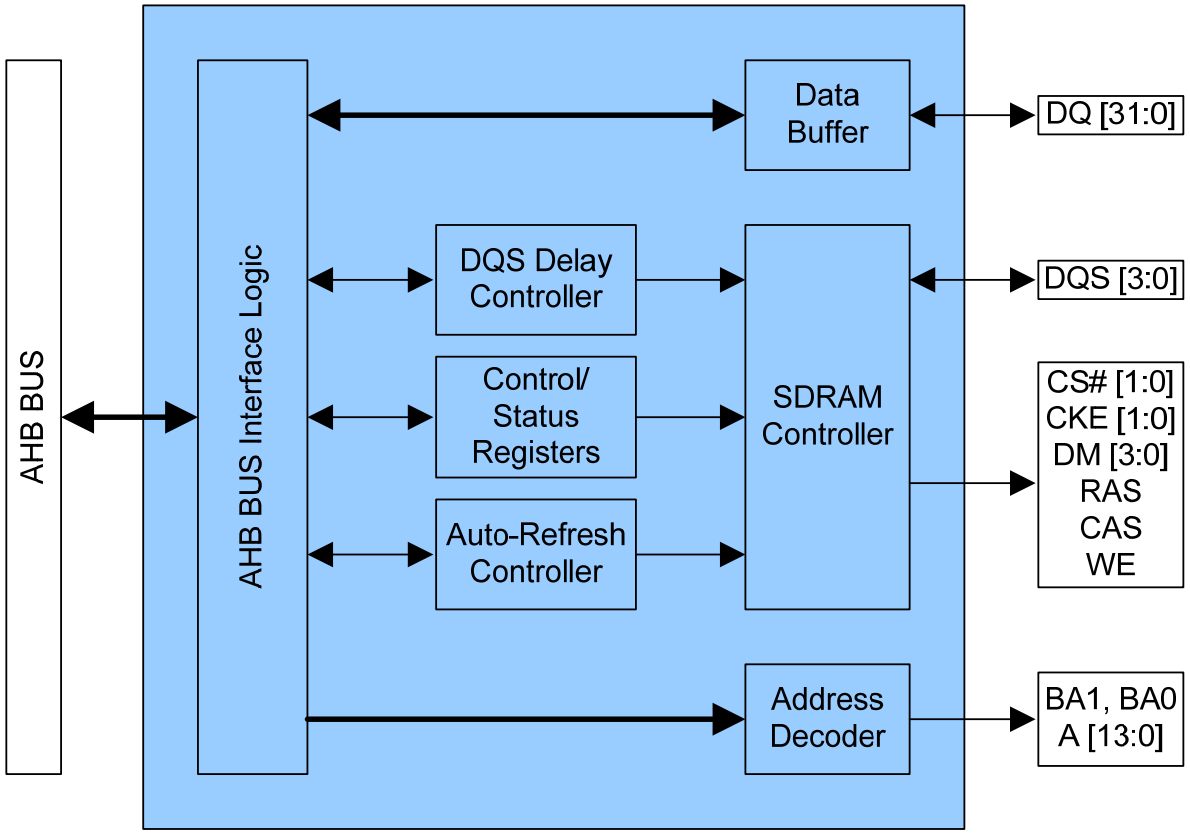


Figure 5-1 DDRC block diagram

5.2 Register Description

Table 5-1 DDRC Register lists the registers of DDR Controller. All of these registers are 32bit, and each bit of the register represents or controls one interrupt source that list in Table 5-1 DDRC Register.

All DDRC register 32bit access address is physical address.
The physical address base for the address-mapped registers of DDRC is 0x13020000.

Table 5-1 DDRC Register

Name	Address offset	Width	Access	Description
DSTATUS	0x00	32	RW	Status Register
DCFG	0x04	32	RW	DDR Configure Register
DCTRL	0x08	32	RW	DDR Control Register

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DLMR	0x0C	32	RW	DDR Load-Mode-Register
DTIMING1	0x10	32	RW	DDR Timing Configure Register 1
DTIMING2	0x14	32	RW	DDR Timing Configure Register 2
DREFCNT	0x18	32	RW	Auto-Refresh Counter
DDQS	0x1C	32	RW	DDR DQS Delay Control Register
DDQSADJ	0x20	32	RW	DDR DQS Delay Adjust Register
DMMAP0	0x24	32	RW	DDR Memory CS0 Map Configure Register
DMMAP1	0x28	32	RW	DDR Memory CS1 Map Configure Register
DDELAYCTRL1	0x2C	32	RW	DDR Memory Delay Control Register1
DDELAYCTRL2	0x30	32	RW	DDR Memory Delay Control Register2
DSTRB	0x34	32	RW	Multi-media stride register
PMEMBS0	0x50	32	RW	IO pad control register
PMEMBS1	0x54	32	RW	IO pad control register
PMEMOSEL	0x58	32	RW	IO pad control register
PMEMOEN	0x5C	32	RW	IO pad control register

5.2.1 DSTATUS

DSTATUS **0x1302000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								ENDIAN	MISS	DPDN	PDN	AREF	SREF	Reserved	CKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31~8: Reserved. Writing has no effect, read as zero.

ENDIAN: Read-only, indicate the data endian status.

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Bit [7]	Description	Remark
0	Little data Endian.	(reset value)
1	Big data Endian.	

MISS: Indicate the bus memory-operation address out of DDRC memory mapping area. (this bit can be written)

Bit [6]	Description	Remark
0	No operation miss DDRC memory mapping.	(reset value)
1	At last one operation miss DDRC memory mapping.	

DPDN: Indicate the deep-power-down status of DDR memory.

Bit [5]	Description	Remark
0	DDR memory is NOT in deep-power-down state.	(reset value)
1	DDR memory is in deep-power-down state.	

PDN: Indicate the power-down status of DDR memory.

Bit [4]	Description	Remark
0	DDR memory is NOT in power-down state.	(reset value)
1	DDR memory is in power-down state.	

AREF: Indicate the auto-refresh status of DDR memory.

Bit [3]	Description	Remark
0	DDR memory is NOT in auto-refresh state.	(reset value)
1	DDR memory is in auto-refresh state.	

SREF: Indicate the self-refresh status of DDR memory.

Bit [2]	Description	Remark
0	DDR memory is NOT in self-refresh state.	(reset value)
1	DDR memory is in self-refresh state.	

CKE1: not support in this version.

Bit [1]	Description	Remark
0	CKE1 Pin is low.	(reset value)
1	CKE1 Pin is high.	

CKE0: Indicate the CKE0 Pin status of DDR memory.

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Bit [0]	Description	Remark
0	CKE0 Pin is low.	(reset value)
1	CKE0 Pin is high.	

5.2.2 DCFG

Configure the external memory, once set; this register can NOT be changed on-the-fly.

DCFG 0x13020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			ROW1		COL1		BA1	IMBA	DQSMD	BTRUN	Reserved					MISPE	TYPE			ROW0		COL0		CS1EN	CS0EN	CL				BA0	DW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31~29, 20~16: Reserved. Writing has no effect, read as zero.

MISPE: Miss CS protect. Set 1 to enable.

If software read (or write) a memory space which is not select by any CS, this function will return random data to a read operation (or mask write operation) to avoid system bus be locked. A CS missing flag will set in DSTATUS.

DQSMD: Dqs pin mode. (only for inner test)

1: DQS pin with pull down resist

0: DQS pin without pull down resist

BTRUN: burst terminate enable. (only for mddr /ddr1)

1: enable

0: disable

IMBA:

0: CS0, CS1 connected 2 memory chips which has same ROW, COL, BA configuration.
In this mode, ROW,COL, BA configure both two chips. ROW1,COL1,BA1 are don't care

1: CS0, CS1 connected 2 memory chips which has different ROW, COL, BA configuration.
ROW, COL, BA refer to CS0; ROW1, COL1, BA1 refer to CS1

MEM_TYPE: Select external memory device type.

This field is not supported by current DDRC design.

Bit [14:12]	Description	Remark
000	Normal SDR (Single-Data-Rate) SDRAM(Not support).	(reset value)
001	Mobile SDR(Not support).	
010	Normal DDR1 (Double-Data-Rate) SDRAM.	
011	Mobile DDR.	
100	Normal DDR2.	
101	Mobile DDR2 (Not support).	
110	Normal DDR3 (Not support).	

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111	Mobile DDR3 (Not support).	

ROW0/1: Row Address width. Specify the row address width of external DDR.

Bit [11:10]	Description	Remark
00	12-bit row address is used.	(reset value)
01	13-bit row address is used.	
10	14-bit row address is used.	
11	Reserved.	

COL0/1: Column Address width. Specify the Column address width of external DDR.

Bit [9:8]	Description	Remark
00	8-bit Column address is used.	(reset value)
01	9-bit Column address is used.	
10	10-bit Column address is used.	
11	11-bit Column address is used.	

CS1EN: DDR Chip-Select-1 Enable.

If there're ddr memory connected to ddr pin cs1, set CS1EN=1.

Bit [7]	Description	Remark
0	DDR Pin CS1 un-used.	(reset value)
1	There're DDR memory connected to CS1.	

CS0EN: DDR Chip-Select-0 Enable.

If there're ddr memory connected to ddr pin cs0, set CS0EN=1.

Bit [6]	Description	Remark
0	DDR Pin CS0 un-used.	(reset value)
1	There're DDR memory connected to CS0.	

CL: CAS Latency.

Bit [5:2]	Description	Remark
0,000	CL = 1 tCK.	(reset value)
0,001	CL = 1.5 tCK.	
1,001	CL = 2 tCK.	
0,010	CL = 2.5 tCK.	
1,010	CL = 3 tCK.	
0,011	CL = 3.5tCK.	
1,011	CL = 4 tCK.	
0,100	CL = 4.5 tCK.	

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1,100	CL = 5 tCK.	
0,101	CL = 5.5 tCK.	
1,101	CL = 6 tCK.	
0,110	CL = 6.5 tCK.	
1,110	CL = 7 tCK.	
Others	Reserved.	

BA0/1: Bank Address width of DDR memory.

Bit [1]	Description	Remark
0	4 bank device, Pin ba[1:0] valid, ba[2] un-used.	(reset value)
1	8 bank device, Pin ba[2:0] valid.	

DW: External DDR Memory Data Width.

Specify the external DDR memory data width.

Bit [0]	Description	Remark
0	External memory data width is 16-bit.	(reset value)
1	External memory data width is 32-bit.	

5.2.3 DCTRL

On the posedge of START, one command selected by CMD field will be performed.

DCTRL 0x13020008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ACTPD	PDT			ACTSTP	Reserved				DPD	SR	UNALIGN	ALH	Reserved	CKE	RESET	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 31~16, 10~7,2: Reserved. Writing has no effect, read as zero.

ACTSTP: Acitve Clock-Stop.

0: Clock can be stopped only after all banks be precharged

1: Clock can be stopped with some bank's row actived

ACTPD: Active Power-Down.

Some SDRAM devices support Active-Power-Down.

By default, ACTPD=0, hardware will percharge all active banks before entering Power-Down mode, so called Precharge-Power-Down.

By setting ACTPD=1, hardware drives SDRAM into Power-Down mode without precharge all active banks, some banks are still active in Power-Down mode, so called Active-Power-Down.

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Bit [15]	Description	Remark
0	Precharge all banks before entering power-down.	(reset value)
1	Do not precharge all banks before entering power-down.	

PDT: Power-Down Timer.

When there's no access to DDR memory for a period of time, hardware drives DDR into power-down mode to save power consumption. Hardware can exit Power-Down mode automatically when new access arrives.

If PDT=0, power-down function disabled.

If use power-down, recommend to enable it after DDR initialization finished.

Bit [14:13]	Description	Remark
000	power-down disabled, hardware never drive SDRAM into power-down mode.	(reset value)
001	Enter power-down after 8 tCK idle.	
010	Enter power-down after 16 tCK idle.	
011	Enter power-down after 32 tCK idle.	
100	Enter power-down after 64 tCK idle.	
101	Enter power-down after 128 tCK idle.	
110 - 111	Reserved.	

SR: Software drive external DDR device entering Self-Refresh mode.

Software set SR=1 drive external DDR device entering self-refresh mode;

Software set SR=0 drive external DDR device exiting self-refresh mode;

In this mode, the CK to external DDR device would be stopped during self-refresh period;

But the clock supply to ddr_controller logic would not stop.

Software can read & write ddr_controller registers in this mode.

Software can NOT read or write memory data in this mode.

NOTE: Since ddr_controller registers are accessed via AXI bus interface, software must guarantee that there's no memory access during self-refresh mode. Otherwise, software can NOT exit this mode, **system would hangup!!**

Bit [5]	Description	Remark
0	Drive external DDR device entering self-refresh mode.	(reset value)
1	Drive external DDR device exiting self-refresh mode.	

DPD: Software drive external Mobile DDR device entering Deep-Power-Down mode.

Software set DPD = 1 drive external Mobile DDR device entering Deep-Power-Down mode instead of Power-Down mode, when there's no access to DDR memory for a period of time.

So you must first enable Power-Down mode (refer to PDT).

Software need to reset DDR controller and re-do a complete initial process to exit

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Deep-Power-Down mode.

When external device go to Deep-Power-Down mode, it will lose all data store in memory and registers.

The memory chip will disable inner power support to save power.

UNALIGN: Enable unaligned transfer on AXI BUS.

Bit [4]	Description	Remark
0	Disable unaligned transfer on AXI BUS.	(reset value)
1	Enable unaligned transfer on AXI BUS.	

ALH: Advanced Latency Hiding.

This is a test purpose register.

Some latency timings can be hidden in special cases.

Bit [3]	Description	Remark
0	Disable ALH.	(reset value)
1	Enable ALH.	

CKE: Control the status of CKE pin.

Write CKE=1 can set CKE pin to HIGH state.

Write CKE=0 would be ignored.

The default value of CKE Pin is low;

CKE0,1 Pins status is represented by DDR_STATUS register.

Caution: This register is used only for DDR initializing sequence; software can NOT update this register when DDR memory is in normal working mode.

Bit [1]	Description	Remark
0	Not set CKE Pin High.	(reset value)
1	Set CKE Pin HIGH.	

RESET: Module reset for ddr_controller.

Software reset ddr_controller by setting RESET bit high. Then, software end reset by setting RESET bit low.

Bit [0]	Description	Remark
0	End resetting ddr_controller.	(reset value)
1	Resetting ddr_controller.	

5.2.4 DLMR

DLMR register is used for initializing the DDR SDRAM memory device.

On the posedge of START, one command selected by CMD field will be performed.

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DLMR **0x1302000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			DDR_ADDR													Reserved					BA			Reserved		CMD		Reserved			START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 31~30, 15~11, 7~6, 3~1: Reserved. Writing has no effect, read as zero.

DDR_ADDR: When performing a DDR command, DDR_ADDR[13:0] corresponding to external DDR address Pin A[13:0]; DDR_ADDR[15:14] are reserved.

Bit [29:16]	Description	Remark
0000_0000	corresponding to external DDR address Pin A[13:0].	(reset value)

BA: Bank Address.

When performing a DDR command, BA[2:0] corresponding to external DDR address Pin BA[2:0].

Bit [10:8]	Description	Remark
000	corresponding to external DDR address Pin BA[2:0].	(reset value)

CMD: Select command to process when setting START from low to high.

On the posedge of START, one of the following commands will be performed.

Bit [5:4]	Description	Remark
00	Precharge one bank / All banks. (dependent field : BA, DDR_ADDR)	(reset value)
01	Auto-Refresh.	
10	Load Mode Register. (dependent field : BA, DDR_ADDR)	
11	Reserved.	

START: Start perform a command to external DDR memory.

The command is performed on the posedge of START; Hardware will clear START bit to zero when command issued out to external DDR memory.

Write 0 to START will be ignored and take no effect;

START=1 means hardware is busy executing current command and can NOT accept new command;

Software must check START=0 before writing 1 to START.

Bit [0]	Description	Remark
0	No command is performed.	(reset value)
1	On the posedge of START, perform a command defined by CMD field.	

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5.2.5 DTIMING1,2 (DDR Timing Config Register 1, 2)

The timing parameters are identical to the JEDEC DDR Specification.

DTIMMING1 **0x13020010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tRAS				Reserved		tRTP		Reserved		tRP		Reserved		tRCD		tRC				Reserved		tRRD		Reserved		tWR		Reserved		tWTR	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 27~26, 23, 19, 11~10, 7, 3-2: Reserved. Writing has no effect, read as zero.

tRAS: ACTIVE to PRECHARGE command period.

tRAS defines the ACTIVE to PRECHARGE command period to the same bank.

Bit [31:28]	Description	Remark
0000	1 tCK.	(reset value)
0001	3 tCK.	
0010	5 tCK.	
0011	7 tCK.	
… …	**… 2 * tRAS + 1 …**	
1101	27 tCK.	
1110	29 tCK.	
1111	31 tCK.	

tRTP: READ to PRECHARGE command period.

Bit [25:24]	Description	Remark
00	1 tCK.	(reset value)
01	2 tCK.	
10	3 tCK.	
11	4 tCK.	

tRP: PRECHARGE command period.

tRP defines the PRECHARGE to next command period to the same bank.

Bit [22:20]	Description	Remark
000	1 tCK.	(reset value)
001	2 tCK.	
010	3 tCK.	
011	4 tCK.	
100	5 tCK.	
101	6 tCK.	

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110	7 tCK.	
111	8 tCK.	

tRCD: ACTIVE to READ or WRITE command period.

tRCD defines the ACTIVE to READ/WRITE command period to the same bank.

Bit [18:16]	Description	Remark
000	1 tCK.	(reset value)
001	2 tCK.	
010	3 tCK.	
011	4 tCK.	
100	5 tCK.	
101	6 tCK.	
110	7 tCK.	
111	8 tCK.	

tRC: ACTIVE to ACTIVE command period.

tRC defines the ACTIVE to ACTIVE command period to the same bank.

Since tRCD + read/write-time + tRP > tRC always match, in most cases, tRC can be disabled.

Bit [15:12]	Description	Remark
0000	1 tCK.	(reset value)
0001	3 tCK.	
0010	5 tCK.	
0011	7 tCK.	
… …	**… 2 * tRC + 1 …**	
1101	27 tCK.	
1110	29 tCK.	
1111	31 tCK.	

tRRD: ACTIVE bank A to ACTIVE bank B command period.

tRRD defines the ACTIVE to ACTIVE command period to **different** banks.

Bit [9:8]	Description	Remark
00	Disable tRRD counter.	(reset value)
01	2 tCK.	
10	3 tCK.	
11	4 tCK.	

tWR: WRITE Recovery Time defined by register MR of DDR2 memory.

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Bit [6:4]	Description	Remark
000	1 tCK.	(reset value)
001	2 tCK.	
010	3 tCK.	
011	4 tCK.	
100	5 tCK.	
101	6 tCK.	
110 - 111	Reserved.	

tWTR: WRITE to READ command delay.

Bit [1:0]	Description	Remark
00	1 tCK.	(reset value)
01	2 tCK.	
10	3 tCK.	
11	4 tCK.	

DTIMING2 **0x13020014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				tRFC					Reserved			tRWCOV		tCKE			Reserved			tMINSR				Reserved		tXP			Reserved		tMRD	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31~30, 23~19, 15~12, 7, 3~2: Reserved. Writing has no effect, read as zero.

tRWCOV: in common, set this value equal to DDELAYCTRL1.Tsel[1:0].

tCKE: minimum CKE pulse width.

tCKE define the minimum CKE pulse width, include high level and low level.

Bit [18:16]	Description	Remark
000	1 tCK.	(reset value)
001	2 tCK.	
010	3 tCK.	
011	4 tCK.	
100	5 tCK.	
101	6 tCK.	
110	7 tCK.	
111	8 tCK.	

tRFC: AUTO-REFRESH command period.

tRFC defines the minimum delay after an AUTO-REFRESH command. During tRFC period,

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no command can be issued to DDR memory.

Delay Time = **2 * tRFC + 1.**

Bit [29:24]	Description	Remark
000000	1 tCK.	(reset value)
000001	3 tCK.	
000010	5 tCK.	
000011	7 tCK.	
… …	**… 2 * tRFC + 1 …**	
111101	125 tCK.	
111110	127 tCK.	
111111	129 tCK.	

* tCK – one DDR memory clock cycle, typical tCK value is 7.5 ns (133MHz clock).

tMINSR: Minimum Self-Refresh / Deep-Power-Down time.

After DDR memory turns into Self-Refresh or Deep-Power-Down mode, it will NOT exit until tMINSR condition meets.

Delay Time = tMINSR * 8 + 1.

Bit [11:8]	Description	Remark
0000	1*8 + 1 tCK.	(reset value)
0001	2*8 + 1 tCK.	
0010	3*8 + 1 tCK.	
0011	4*8 + 1 tCK.	
… …	**… tMINSR * 8 + 1 …**	
1101	14*8 + 1 tCK.	
1110	15*8 + 1 tCK.	
1111	16*8 + 1 tCK.	

tXP: EXIT-POWER-DOWN to next valid command period.

tXP defines the EXIT-POWER-DOWN to next valid command period to all banks.

Bit [6:4]	Description	Remark
000	1 tCK.	(reset value)
001	2 tCK.	
010	3 tCK.	
011	4 tCK.	
100	5 tCK.	
101	6 tCK.	
110	7 tCK.	
111	8 tCK.	

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tMRD: Load-Mode-Register to next valid command period.

tMRD defines the Load-Mode-Register to next valid command period.

Bit [1:0]	Description	Remark
00	1 tCK.	(reset value)
01	2 tCK.	
10	3 tCK.	
11	4 tCK.	

5.2.6 DREFCNT (DDR Auto-Refresh Counter)

DREFCNT **0x13020018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CON								CNT								Reserved				CLK_DIV			REF_EN
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31~24, 7-4: Reserved. Writing has no effect, read as zero.

CON: A constant value used to compare with the CNT value.

After reset, CON=0xFF and CNT=0x00;

It is not recommended to set CON=0x00.

CNT: 8-bit counter; When the value of CNT match the value of CON, flag bit EQU is set high and an auto-refresh command will be issued to DDR memory. READ only.

CLK_DIV : Clock Divider.

Divide the dclk to generate a lower frequency of clock to drive the auto-refresh counter. This helps to save power consumption.

When the DDR memory is in self-refresh mode or in deep-power-down mode, disable the clock of auto-refresh counter can save power consumption. Future more, the module clock (ahb_clk & dclk) to DDRC can also be stopped.

Bit [3:1]	Description	Remark
000	dclk / 16.	(reset value)
001	dclk / 32.	
010	dclk / 64.	
011	dclk / 128.	
100	dclk / 256.	
101	dclk / 512.	
110	dclk / 1024.	
111	--	

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REF_EN: Enable Refresh Counter.

Software set REF_EN=1 right after initialize ddr memory.

Bit [29]	Description	Remark
0	Enable auto-refresh counter.	(reset value)
1	Disable auto-refresh counter.	

5.2.7 DDQS (DDR DQS Delay Control Register)

DDRC contains an on-chip DLL to control the DQS Delay for read data and write data.

DDQS **0x1302001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ERROR	READY	Reserved		SRDET	DET	AUTO	Reserved	CLKD						Reserved		WDQS						Reserved		RDQS					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31~30, 27-26, 22, 15-14, 7-6: Reserved. Writing has no effect, read as zero.

ERROR: ahb_clk Delay Detect ERROR, read-only.

When hardware detect one ahb_clk cycle delay failed, ERROR is set high;

ERROR is cleared zero when a new detection starts;

ERROR is valid only when READY=1.

Bit [29]	Description	Remark
0	delay detect success.	(reset value)
1	delay detect failed.	

READY: ahb_clk Delay Detect READY, read-only.

When hardware detect complete, ERROR is set high.

READY is cleared zero when a new detection starts.

Bit [28]	Description	Remark
0	delay detect NOT complete.	(reset value)
1	delay detect complete.	

SRDET: DDRC auto re-detect and set (if auto = = 1) delay line after clock change.

It will consume extra times in clock change process.

Bit [25]	Description	Remark
0	not enable.	(reset value)
1	Enable.	

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AUTO: Hardware auto-detect & set delay line.

Bit [23]	Description	Remark
0	Hardware do NOT auto-set delay line.	(reset value)
1	Hardware auto-set delay line after detect success.	

DET: Start delay detecting.

Write 1 to START bit starts a new delay detect progress.

When delay detect complete, START is cleared zero by hardware.

START can be used as the BUSY flag. When START=1, it is busy.

Bit [24]	Description	Remark
0	No operation.	(reset value)
1	Delay detect in progress, busy.	

CLKD: Indicate the number of delay elements needed to delay ¼ tCK.

CLKD is a reference value for setting WDQS and RDQS.

CLKD is set when DLL detection finished.

The range of CLKD: [0, +63].

WDQS: Set the number of delay elements used on the write DQS delay-line.

When WDQS increase one, the delay value of write DQS increase approximately 0.1 ns .

The range of WDQS, RDQS: [0, +63].

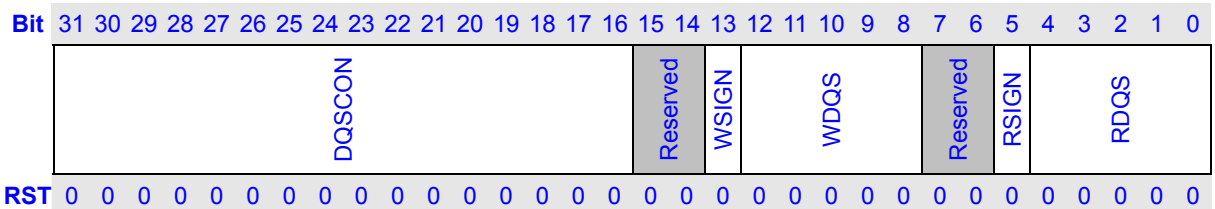
NOTE: The delay value of each delay element depends on the technology and the structure of the delay cell; "0.1 ns" is just an example at .18 technology.

RDQS: Set the number of delay elements used on the read DQS delay-line.

When RDQS increase one, the delay value of read DQS increase approximately 0.1 ns.

5.2.8 DDQSADJ (DDR DQS Delay Adjust Register)

DDQSADJ **0x13020020**



Bits 15~14, 7-6: Reserved. Writing has no effect, read as zero.

DQSCON: DQS detect looping counter threshold. When inner counter equal to DQSCON, then trigger a DQS detect operation to auto adjust DQS delay line.This inner counter use AUTO_REFRESH's divided clock (refer to DREFCNT). When DQSCON set to 0, this function be disabled.

WSIGN, RSIGN: The adjust value's sign. 0: plus; 1: minus.

WDQS, RDQS: The adjust value for WRITE and READ DQS delay.

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WDQS, RDQS can be either positive or negative number.
For negative number, it should be in “complemental code” format;
The range of WDQS, RDQS : [-16, +15].

For READ: DQS_Delay = DDQS.RDQS +/- DDQSADJ.RDQS.
For WRITE: DQS_Delay = DDQS.WDQS +/-DDQSADJ.WDQS.

5.2.9 DMMAP0,1 (DDR Memory Map Config Register)

The physical base address and size of external DDR Memory can be configured by DMMAP register.
The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, ….**

When the following equation is met:
(AXI_BUS_Address[31:24] & MASK[7:0]) == BASE
The DDR Memory is selected.

DMMAP0,1 **0x13020024, 0x13020028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits 31~16: Reserved. Writing has no effect, read as zero.
BASE: base address.
MASK: address mask.
Examples:
1 DDR address space in system memory : 0x2000_0000 ~ 0x2FFF_FFFF (256MB)
BASE=0x20 MASK=0xF0.
2 DDR address space in system memory : 0x5000_0000 ~ 0x57FF_FFFF (128MB)
BASE=0x50 MASK=0xF8.
NOTE: If DDRC is disabled, please set DMMAP=0x0000_FF00 (reset value).

5.2.10 DDELAYCTRL

This register can be re-configured at any time, but this change takes effect after an Auto-Refresh command occurs.

DDELAYCTRL1 **0x1302002C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TSEL		MSEL		HL	QUAR	Reserved							MAUTO	MSIGN	MASK_DELAY_SEL_ADJ					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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DDELAYCTRL2 **0x13020030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										MASK_DELAY_SEL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved: Writing has no effect, read as zero.

MSEL: Mask delay select.

Bit [17:16]	Description	Remark
00	No delay.	(reset value)
01	delay 1 tCK.	
10	delay 2 tCK.	
11	delay 3 tCK.	

HL: Half clock delay select.

Adjust MSEL delay 1/2 tCK.

0: delay no change

1: delay reduced 1/2 tCK

QUAR: Quarter clock delay select.

Adjust MSEL delay 1/4 tCK.

0: delay no change

1: delay add 1/4 tCK

Msel[1]	Msel[0]	HL	QUAR	DELAY
0	0	1	0	- 0.5 tCK
0	0	1	1	- 0.25 tCK
0	0	0	0	0 tCK
0	0	0	1	0.25 tCK
0	1	1	0	0.5 tCK
0	1	1	1	0.75 tCK
0	1	0	0	1 tCK
0	1	0	1	1.25 tCK
1	0	1	0	1.5 tCK
1	0	1	1	1.75 tCK
1	0	0	0	2 tCK
1	0	0	1	2.25 tCK
1	1	1	0	2.5 tCK
1	1	1	1	2.75 tCK
1	1	0	0	3 tCK
1	1	0	1	3.25 tCK

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TSEL: Read delay select.

Bit [19:18]	Description	Remark
00	No delay.	(reset value)
01	delay 1 Tck.	
10	delay 2 tCK.	
11	delay 3 tCK.	

MASK_DELAY_SEL_ADJ , MASK_DELAY_SEL, MSIGN:

Delay configure for an inner mask, use as DDQS and DDQSADJ.

MAUTO:

Enable inner mask delay function. In normal keep this bit to 1.

5.2.11 DSTRB

DSTRB **0x13020034**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			STRB0													Reserved			STRB1												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Inner usage.

Just for Video Decoder.

5.2.12 DDR PAD CONTROLL REGISTER 0

PMEMCTRL0 **0x13020050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ODTDQS3		ODTDQS2		ODTDQS1		ODTDQS0		ODTDQ3		ODTDQ2		ODTDQ1		ODTDQ0		SSELDQS3		SSELDQS2		SSELDQS1		SSELDQS0		SSELDQ3		SSELDQ2		SSELDQ1		SSELDQ0	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	ODTDQS3	ODT configure for DQS3.	RW
29:28	ODTDQS2	ODT configure for DQS2.	RW
27:26	ODTDQS1	ODT configure for DQS1.	RW
25:24	ODTDQS0	ODT configure for DQS0.	RW
23:22	ODTDQ3	ODT configure for DQ3.	RW

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21:20	ODTDQ2	ODT configure for DQ1.	RW
19:18	ODTDQ1	ODT configure for DQ1.	RW
17:16	ODTDQ0	ODT configure for DQ0.	RW
15:14	SSELDQS3	Output mode & strength select for DQS[3].	RW
13:12	SSELDQS2	Output mode & strength select for DQS[2].	RW
11:10	SSELDQS1	Output mode & strength select for DQS[1].	RW
9:8	SSELDQS0	Output mode & strength select for DQS[0].	RW
7:6	SSELDQ3	Output mode & strength select for DQ[31:24].	RW
5:4	SSELDQ2	Output mode & strength select for DQ[23:16].	RW
3:2	SSELDQ1	Output mode & strength select for DQ[15:8].	RW
1:0	SSELDQ0	Output mode & strength select for DQ[7:0].	RW

5.2.13 DDR PAD CONTROLL REGISTER 1

PMEMCTRL1 **0x13020054**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												ODTCK		ODTCKE		ODTADDR		ODTDM3		ODTDM2		ODTDM1		ODTDM0		ODTCMD		ODTCS1		ODTCS0	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
19:18	ODTCK	ODT configure for CK.	RW
17:16	ODTCKE	ODT configure for CKE.	RW
15:14	ODTADDR	ODT configure for ADDR.	RW
13:12	ODTDM3	ODT configure for DM3.	RW
11:10	ODTDM2	ODT configure for DM2.	RW
9:8	ODTDM1	ODT configure for DM1.	RW
7:6	ODTDM0	ODT configure for DM0.	RW
5:4	ODTCMD	ODT configure for CMD.	RW
3:2	ODTCS1	ODT configure for CS1.	R
1:0	ODTCS0	ODT configure for CS0.	RW

ODT[1:0]	ODT Rtt
00	disable ODT
01	75 ohm
10	150 ohm
11	Reserved

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5.2.14 DDR PAD CONTROLL REGISTER 2

This register is used to select strength of SSTL18, SSTL2, MDDR and LVTTL combo single-end/differential transmitter.

PMEMCTRL2 **0x13020058**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												SSELCK		SSELCKE		SSELADDR		SSELDM3		SSELDM2		SSELDM1		SSELDM0		SSELCMD		SSELCS1		SSELCS0	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:18	SSELCK	Output mode & strength select for CKO.	RW
17:16	SSELCKE	Output mode & strength select for CKE.	RW
15:14	SSELADDR	Output mode & strength select for ADDR[16:0].	RW
13:12	SSELDM3	Output mode & strength select for DM3.	RW
11:10	SSELDM2	Output mode & strength select for DM2.	RW
9:8	SSELDM1	Output mode & strength select for DM1.	RW
7:6	SSELDM0	Output mode & strength select for DM0.	RW
5:4	SSELCMD	Output mode & strength select for CMD(RAS, CAS,WE).	RW
3:2	SSELCS1	Output mode & strength select for CS1.	RW
1:0	SSELCS0	Output mode & strength select for CS0.	RW

SSEL configure:

MODE	POWER	SSEL[1:0]			
		Reduced strength		Full strength	
DDR1	2.5v	10(CLASS II)		00(CLASS I)	
DDR2	1.8v	10		00	
MDDR	1.8v	11 (2mA)	10 (4mA)	01(8mA)	00 (10mA)

5.2.15 DDR PAD CONTROLL REGISTER 3

This register is used to select output enable signal (low active) of SSTL18, SSTL2, MDDR and LVTTL combo single-end transceiver.

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PMEMCTRL3 **0x1302005C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDDQS3	PDDQS2	PDDQS1	PDDQS0	PDDQ3	PDDQ2	PDDQ1	PDDQ0	Reserved						SSTL2	LVCMOS	SINGLEDQS	OENCK	OENBA2	OENBA1	OENBA0	OENA13	OENA12	OENA11_0	OENDM3	OENDM2	OENDM1	OENDM0	OENCMD	OENCS1	OENCS0	OENCKE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PDDQS3	input enable signal for CKO. 0: enable; 1: disable.	RW
30	PDDQS2	input enable signal for CKO. 0: enable; 1: disable.	RW
29	PDDQS1	input enable signal for CKO. 0: enable; 1: disable.	RW
28	PDDQS0	input enable signal for CKO. 0: enable; 1: disable.	RW
27	PDDQ3	input enable signal for CKO. 0: enable; 1: disable.	RW
26	PDDQ2	input enable signal for CKO. 0: enable; 1: disable.	RW
25	PDDQ1	input enable signal for CKO. 0: enable; 1: disable.	RW
24	PDDQ0	input enable signal for CKO. 0: enable; 1: disable.	RW
23:18	Reserved	Writing has no effect, read as zero.	R
17	SSTL2	SSTL2 select pin. 0: SSTL2(DDR1); 1:SSTL18(DDR2).	RW
16	LVCMOS	LVCMOS select pin. 0: not LVCMOS; 1: LVCMOS(MDDR).	RW
15	SINGLEDQS	single end DQS 0: differential DQS.	RW
14	OENCK	output enable signal for CKO. 0: enable; 1: disable.	RW
13	OENBA2	output enable signal for BA[2] (ADDR[16]). 0: enable; 1: disable.	RW
12	OENBA1	output enable signal for BA[1] (ADDR[15]). 0: enable; 1: disable.	RW
11	OENBA0	output enable signal for BA[0] (ADDR[14]). 0: enable; 1: disable.	RW
10	OENA13	output enable signal for ADDR[13]. 0: enable; 1: disable.	RW
9	OENA12	output enable signal for ADDR[12]. 0: enable; 1: disable.	RW
8	OENA11_0	output enable signal for ADDR[11:0]. 0: enable; 1: disable.	RW
7	OENDM3	output enable signal for DM3. 0: enable; 1: disable.	RW
6	OENDM2	output enable signal for DM2. 0: enable; 1: disable.	RW
5	OENDM1	output enable signal for DM1. 0: enable; 1: disable.	RW
4	OENDM0	output enable signal for DM0. 0: enable; 1: disable.	RW
3	OENCMD	output enable signal for CMD(RAS,CAS,WE). 0: enable; 1: disable.	RW
2	OENCS1	output enable signal for CS1. 0: enable; 1: disable.	RW
1	OENCS0	output put enable signal for CS0. 0: enable; 1: disable.	RW
0	OENCKE	output put enable signal for CKE. 0: enable; 1: disable.	RW

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5.2.16 DDRMPORT

DDRMPORT **0x13020060**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH5G	CH4G	CH3G	CH2G	CH1G	Reserved		CH4LKEN	CH3LKEN	Reserved						CH1RDFST	CH5PRIEN	CH4PRIEN	CH3PRIEN	CH2PRIEN	CH1PRIEN	Reserved	CH5PRI		CH4PRI		CH3PRI		CH2PRI		CH1PRI	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CH5G	Channel 5 ‘s read will be blocked by other channels write at same address. 0: blocked; 1: not blocked.	RW
30	CH4G	Channel 4 ‘s read will be blocked by other channels write at same address. 0: blocked; 1: not blocked.	RW
29	CH3G	Channel 3 ‘s read will be blocked by other channels write at same address. 0: blocked; 1: not blocked.	RW
28	CH2G	Channel 2 ‘s read will be blocked by other channels write at same address. 0: blocked; 1: not blocked.	RW
27	CH1G	Channel 1‘s read will be blocked by other channels write at same address. 0: blocked; 1: not blocked.	RW
26:25	Reserved	Writing has no effect, read as zero.	R
24	CH4LKEN	Channel 4 support lock function. 0: not support; 1: support.	RW
23	CH3LKEN	Channel 3 support lock function. 0: not support; 1: support.	RW
22:17	Reserved	Writing has no effect, read as zero.	R
16	CH1RDFST	Channel 1 support read first than write function. 0: not support; 1: support.	RW
15	CH5PRIEN	Channel 5 support bus priority function. 0: use CH5PRI instead; 1: use bus priority.	RW
14	CH4PRIEN	Channel 4 support bus priority function. 0: use CH4PRI instead; 1: use bus priority.	RW
13	CH3PRIEN	Channel 3 support bus priority function. 0: use CH3PRI instead; 1: use bus priority.	RW
12	CH2PRIEN	Channel 2 support bus priority function. 0: use CH2PRI instead; 1: use bus priority.	RW
11	CH1PRIEN	Channel 1 support bus priority function. 0: use CH1PRI instead; 1: use bus priority.	RW
10	Reserved	Writing has no effect, read as zero.	R
9:8	CH5PRI	set channel 5’s priority if CH5PRIEN = 0 (3-hightest ~ 0-lowest).	RW
7:6	CH4PRI	set channel 4’s priority if CH5PRIEN = 0 (3-hightest ~ 0-lowest).	RW
5:4	CH3PRI	set channel 3’s priority if CH5PRIEN = 0 (3-hightest ~ 0-lowest).	RW
3:2	CH2PRI	set channel 2’s priority if CH5PRIEN = 0 (3-hightest ~ 0-lowest).	RW
1:0	CH1PRI	set channel 1’s priority if CH5PRIEN = 0 (3-hightest ~ 0-lowest).	RW

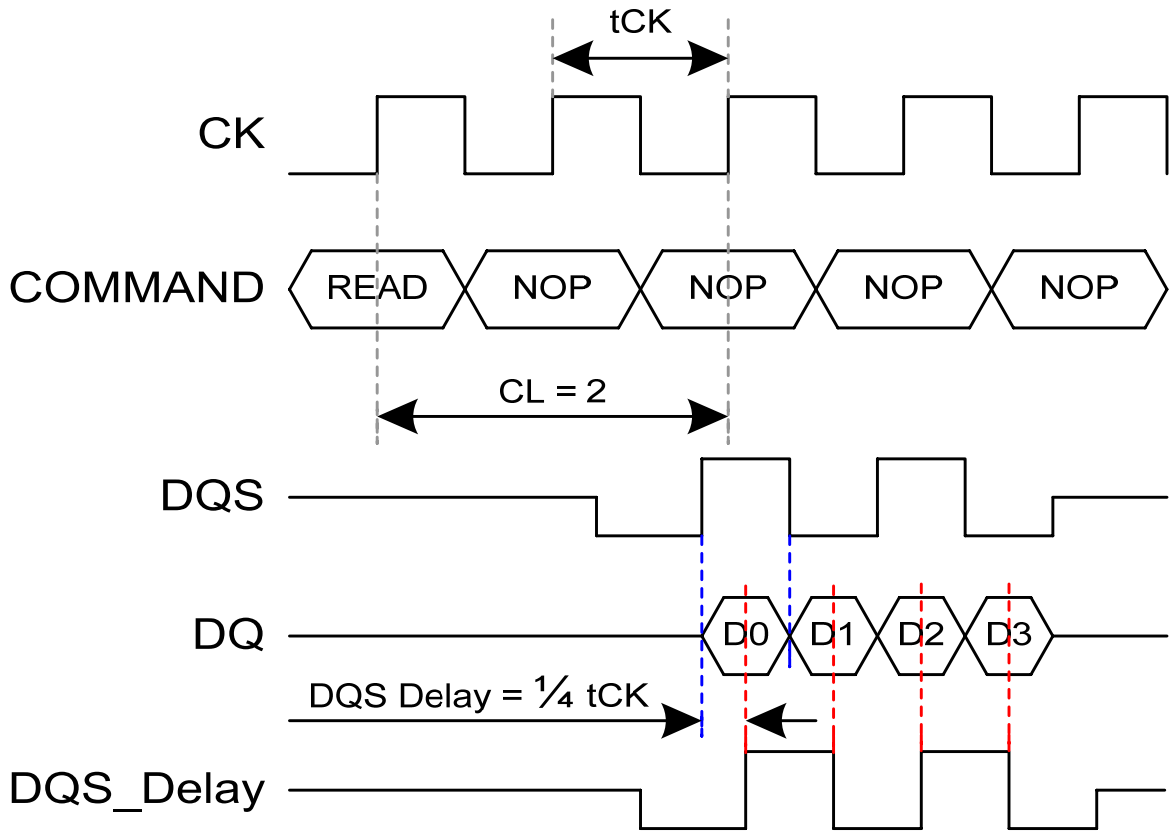
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5.3 Functional Description

5.3.1 DDR DQS Delay Detect-and-Set Processing

Sub-module “DQS Delay Controller” of DDRC generates DQS_Delay signal to capture data;

The following figure illustrates the DQS_Delay in READ case. The DQS_Delay in WRITE case is similar to READ case.



DQS_Delay is used to capture DQ by its posedge and negedge. DQS_Delay signal is generated by the “DQS Delay Controller” sub-module of DDRC.



There’re delay elements in “DQS Delay Controller”; each delay element adds approximately 0.1 ns delay value to between its input and output. The number of delay elements used can be controlled by DDQS.RDQS and DDQS.WDQS.

Note that the delay value of each delay element changes according to the temperature and voltage. It is recommended to adjust the value of DDQS.RDQS and DDQS.WDQS periodically according to the

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temperature change.

The “DQS Delay Controller” provides a mechanism to automatically adjust the DDQS value periodically. Alternatively, this function can be disabled to enable fully manual control.

5.3.2 Detect dclk delay

Setting DDQS.START=1 and DDQS.AUTO=0, hardware do the detect processing one time.
Setting DDQS.START=1 and DDQS.AUTO=1, hardware do the detect-and-set processing one time.
Setting DDQS.START=1 and DDQS.AUTO=2, hardware periodically do the detect-and-set processing after each auto-refresh command.

The detection result stores in DDQS.CLKD. DDQS.CLKD indicates the delay value of half dclk clock cycle (frequency Fdclk=F(DDR CK)). Thus, the delay value:

DQS_Delay = ¼ tCK = ½ DDQS.CLKD <1>

Delay DQS by ¼ tCK means to the ideal case. Actually, there’re always a gap between the ideal value and the real value. The gap comes from many factors such as IC manufacture processing, PCB layout, noise, etc. So, a revised parameter is introduced to equation <1>:

For READ, DQS_Delay = ½ DDQS.CLKD + DDQSADJ.RDQS <2>
For WRITE, DQS_Delay = ½ DDQS.CLKD + DDQSADJ.WDQS <3>
DDQSADJ can be either positive or negative number to add or sub value from DQS_Delay.
After reset, DDQSADJ.RDQS/WDQS = 0.

5.3.3 Set DDQS.RDQS and DDQS.WDQS

When hardware complete a detect processing:

If DDQS.AUTO=0, hardware do NOT set DDQS.RDQS and DDQS.WDQS;
If DDQS.AUTO=1 or 2, hardware set DDQS.RDQS and DDQS.WDQS according to equation <2> and <3>.

5.3.4 Manual Detect-and-Set Processing

DQS delay value can be set manually.

Step 1: Software set DDQS.RDQS and DDQS.WDQS.
Step 2: Software do write- and-read test on DDR Memory, then compare the read data with the write data.
Step 3: Repeat step 1 and 2.

When the tests complete, software can choose the fittest value for RDQS and WDQS.

5.3.5 Handling the DQS delay detection “ERROR”

The number of delay elements for detection dclk: 256;

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The number of delay elements for RDQS: 128;
The number of delay elements for WDQS: 128;

DDRC can't do the detect processing successfully when:

Tmlck > 25.6 ns (256 x 0.1 ns = 25.6 ns)
Or: Fdclk < 40 MHz

According to JEDEC DDR Specification:
For normal DDR, CK > 83 MHz;
For mobile DDR, CK > 0 MHz; there have no requirement for the lower range of CK;
In case detection failed, hardware set RDQS and WDQS with max number if DDQS.AUTO ≠ 0.

5.3.6 DDRC and DDR2 Memory Initialization Sequence

5.3.6.1 Example 1

One 512Mb x16 DDR2 device connected on CS0;
No memory device connected on CS1;
DCK = 133 MHz, CL = 3.

1 After system reset, wait system clock stable before initialize ddrc.
2 Configure the Clock-Control module for ddrc clocks.
3 DDR Memory device need at least 200us initialization time after power-on before it can accept any command.

//----------
// INIT DDRC
//----------

4 Configure DCFG = 0x.
5 Configure DTIMING1 = 0x.
6 Configure DTIMING1 = 0x.
7 Configure DMMAP0 = 0x.
8 Configure DMMAP1 = 0x0000FF00.

//----------
// INIT DDR memory device
//----------

9 Set CKE Pin HIGH : Configure DCTRL = 0x00000002.
10 PRECHAREG-ALL : Configure DCTRL = 0x.
11 Load-Mode-Register EMR2 : Configure DCTRL = 0x.
12 Load-Mode-Register EMR3 : Configure DCTRL = 0x.
13 Load-Mode-Register EMR1 : Configure DCTRL = 0x.
14 Load-Mode-Register MR with DLL reset : Configure DCTRL = 0x.
15 PRECHAREG-ALL : Configure DCTRL = 0x.

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16 AUTO-REFRESH : Configure DCTRL = 0x.
17 AUTO-REFRESH : Configure DCTRL = 0x.
18 Load-Mode-Register MR with DLL reset end : Configure DCTRL = 0x.
19 Load-Mode-Register EMR1 with OCD default : Configure DCTRL = 0x.
20 Load-Mode-Register EMR1 with OCD exit : Configure DCTRL = 0x.
21 Wait at least 200 tCK before next step.

//----------
// Enable Refresh Counter
//----------

22 Enable Refresh Counter : Configure DREFCNT = 0x.
23 AUTO-REFRESH : Configure DCTRL = 0x.

//----------
// DQS Delay Detect
//----------

24 Configure DDQSADJ = 0x.
25 Configure DDQS = 0x.
26 Read register DDQS.
27 configure TSEL form min to max, under each value of TSEL, do 28.
28 Configure {MSEL, HL, QUAR} register, form min delay to max delay (relate to 1.2.7). You need write/read some data by CPU or DMA or other device, to check if the sdram work properly. During this process, record the pass configure, you may found there has several configure pass the test, then chose the one that TSEL min & {MSEL, HL, QUAR} min passed <= {MSEL,HL,QUAR} <= {MSEL, HL, QUAR}max passed.

//----------
// END INITIALIZING SEQUENCE
//----------

5.4 Change Clock Frequency

To save power consumption, the system clock frequency may be changed frequently according to the application. There're 3 ways to change the clock frequency.

5.4.1 Clock-Stop Mode(only in Mobile-ddr)

CPM will auto drive DDRC to clock-stop mode, when use mobile-ddr.
How to change clock, relate CPM spec.

5.4.2 Manually SELF-REFRESH Mode

DDR can stay in SELF-REFRESH & DEEP-POWER-DOWN mode for a long period of time. System clock frequency can be changed during this time. Even more, the clocks to DDRC module can also be stopped to save power-consumption.
Reference Sequence:

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1 Manually issue SELF-REFRESH command to DDR.
2 Change relates register in CPM.
3 Change system clock frequency.
4 Drive DDR exit SELF-REFRESH mode.

5.4.3 CPM driven SELF-REFRESH Mode

CPM will auto drive DDRC to self-refresh mode, when use ddr2, ddr1.
How to change clock, relate CPM spec.

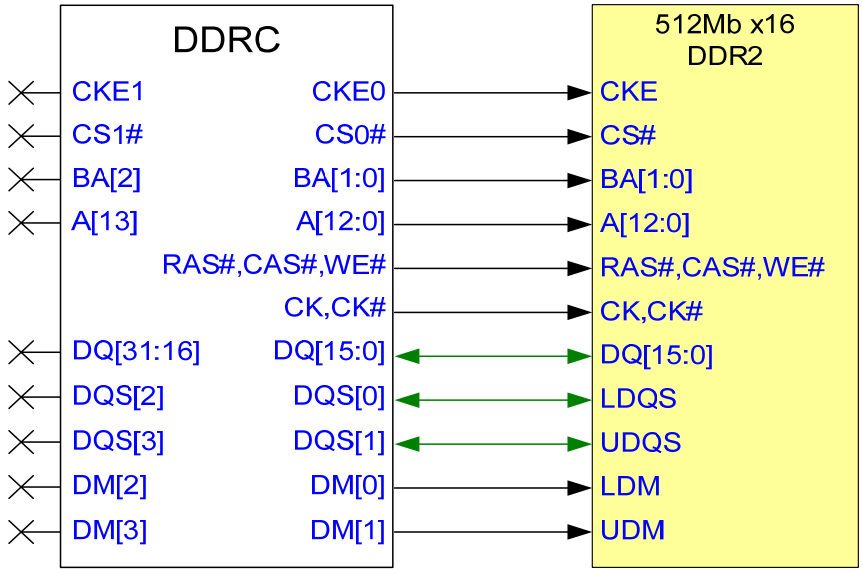
5.5 Data Endian

Fix to little Endian.

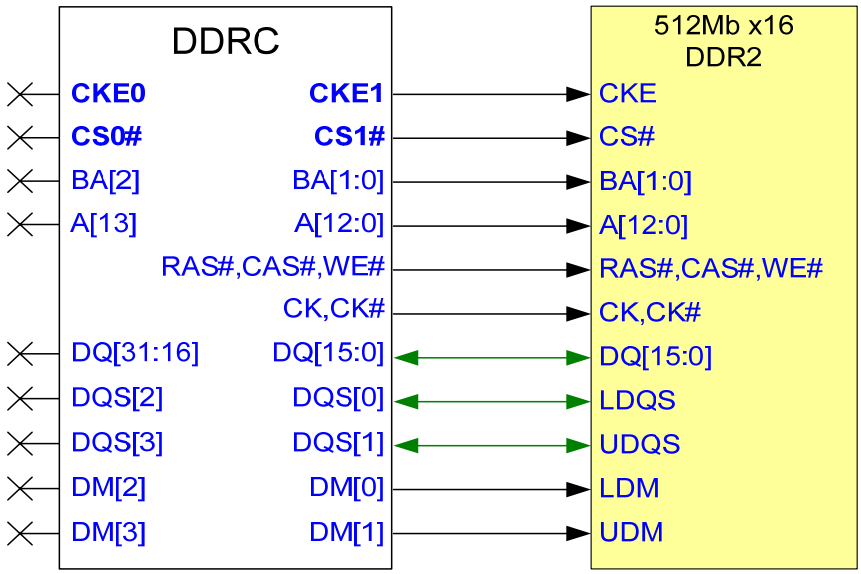
5.6 DDR Connection Diagrams

The following diagrams give examples on the connection to external DDR2 devices.
Note not all the possible connections are listed.

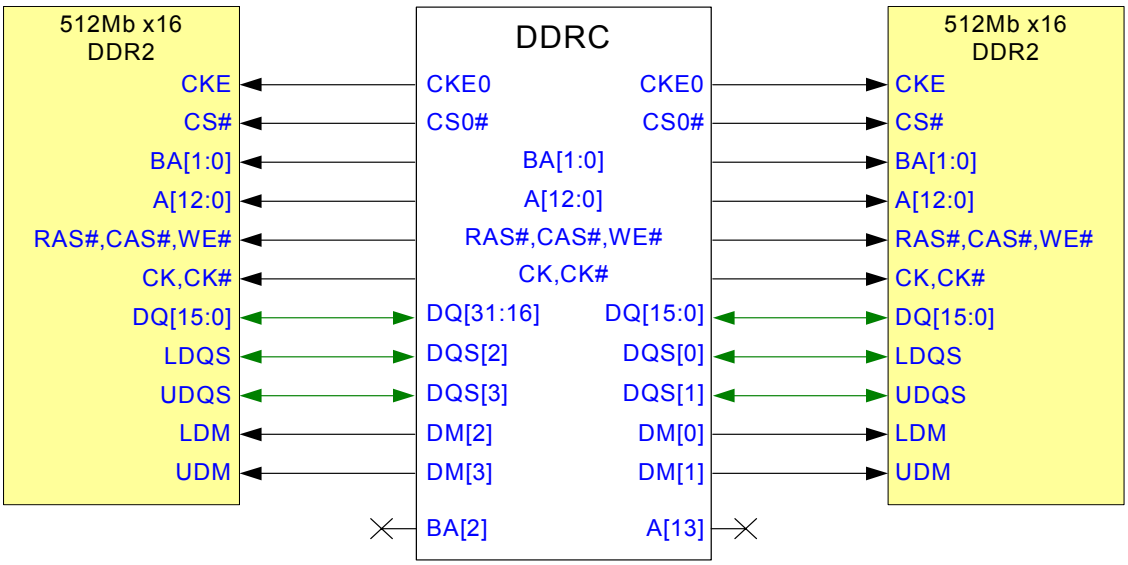
5.6.1 Connection to one 512Mb x16 DDR2 device



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5.6.2 Connection to two 512Mb x16 DDR2 devices



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6 External NAND Memory Controller

6.1 Overview

The External NAND Memory Controller (NEMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of static memory and bus interfaces. It enables the connection of static memory such as NAND flash memory, etc. to this processor.

- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit or 16-bit (no byte control) bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

- NAND flash interface
  - Support on CS6~CS1, sharing with static memory bank6~bank1
  - Support most types of NAND flashes, including 8-bit and 16-bit bus width, 512B/2K/4K/8KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2K/4K/8KB page size, 4 and 5 address cycles are supported
  - Support read/erase/program NAND flash memory
  - Support boot from NAND flash

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6.2 Pin Description

Following table list the NEMC pins.

Table 6-1 NEMC Pin Description

Pin Name	I/O	Signal	Description
Data Bus	I/O	SD15 – SD0	Data I/O.
Address bus	O	SA5–SA0	Address output.
Static chip select 6 ~ 1	O	CS6~1#	Chip select signal that indicates the static bank being accessed.
Read enable	O	RD# /	For Static memory read enable signal.
Write enable	O	WE# /	Static memory write enable signal.
Wait	I	Wait# /	External wait state request signal for memory-like devices.
NAND flash read enable	O	FRE#	NAND flash read enable signal.
NAND flash write enable	O	FWE#	NAND flash write enable signal.
NAND flash ready/busy	I	FRB#	Indicates NAND flash is ready or busy. (When Nand flash boot, GPC30 is used as FRB# of CS1#)

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6.3 Physical Address Space Map

Both virtual spaces and physical spaces are 32-bit wide in this architecture. Virtual addresses are translated by MMU into physical address which is further divided into several partitions for static memory, SDRAM, and internal I/O.

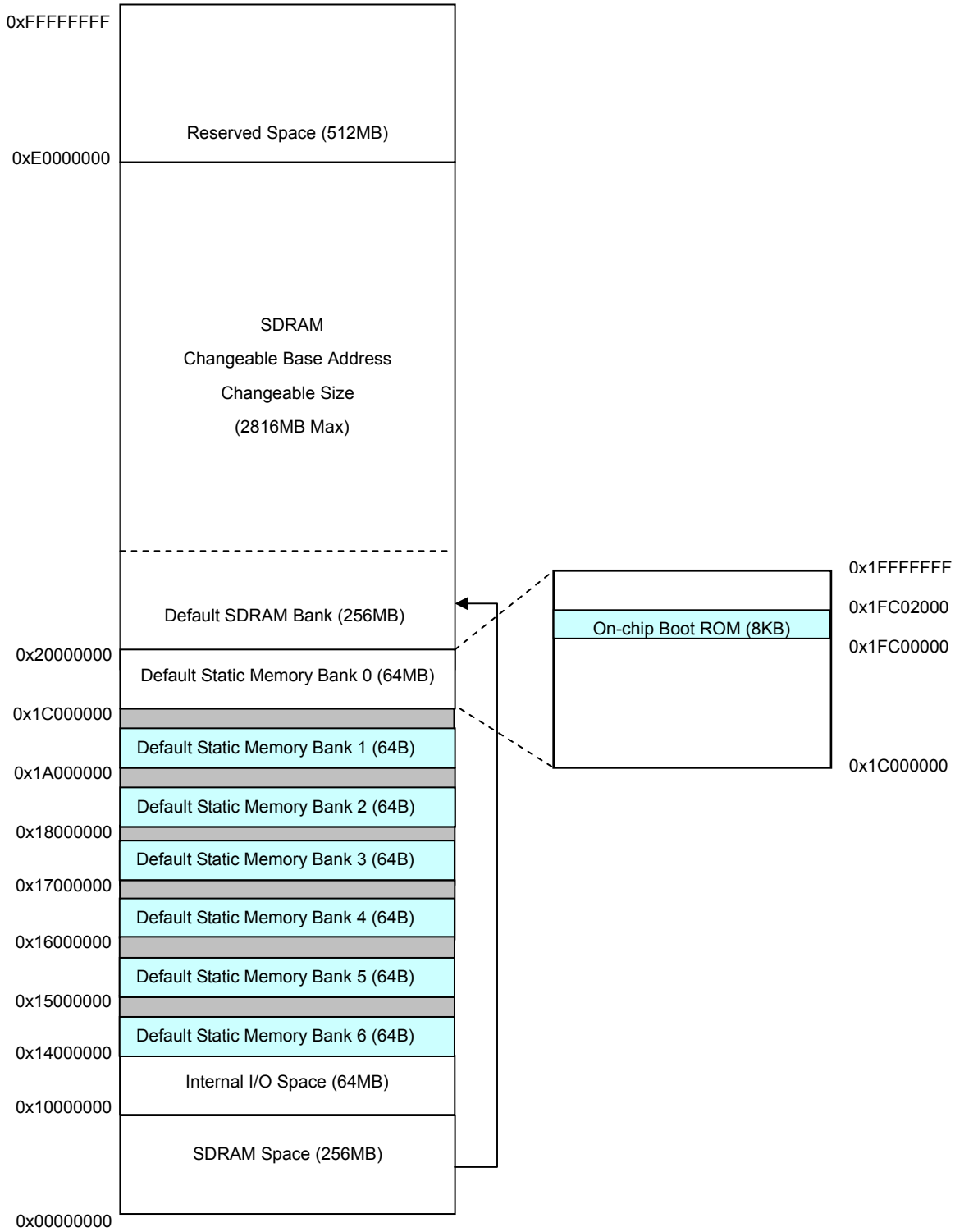


Figure 6-1 Physical Address Space Map

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Table 6-2 Physical Address Space Map

Start Address	End Address	Connectable Memory	Capacity
0x00000000	0x0FFFFFFF	SDRAM Memory	256
0x10000000	0x10FFFFFF	I/O Devices on APB Bus	16
0x11000000	0x12FFFFFF	Reserved	32
0x13000000	0x13FFFFFF	I/O Devices on AHB Bus	16
0x14000000	0x1400003F	Static Memory, CS6#	64B
0x14000040	0x14FFFFFF	Reserved	
0x15000000	0x1500003F	Static Memory, CS5#	64B
0x15000040	0x15FFFFFF	Reserved	
0x16000000	0x1600003F	Static Memory, CS4#	64B
0x16000040	0x16FFFFFF	Reserved	
0x17000000	0x1700003F	Static Memory, CS3#	64B
0x17000040	0x17FFFFFF	Reserved	
0x18000000	0x1800003F	Static Memory, CS2#	64B
0x18000040	0x19FFFFFF	Reserved	
0x1A000000	0x1A00003F	Static Memory, CS1#	64B
0x1A000040	0x1BFFFFFF	Reserved	
0x1C000000	0x1FBFFFFF	Reserved	60
0x1FC00000	0x1FC01FFF	On-chip Boot ROM (8kB)	0.008
0x1FC02000	0x1FFFFFFF	Reserved	3.992
0x20000000	0xDFFFFFFF	SDRAM Memory	3072
0xE0000000	0xFFFFFFFF	Reserved	512

The base address and size of each memory banks are configurable. Software can re-configure these memory banks according to the actual connected memories. Following table lists the default configuration after reset.

Table 6-3 Default Configuration of NEMC Chip Select Signals

Chip-Select Signal	Connected Memory	Capacity	Memory Width *1	Start Address	End Address
CS1#	Static memory bank 1	64 B	8, 16, 32	0x1A000000	0x1A00003F
CS2#	Static memory bank 2	64 B	8, 16, 32	0x18000000	0x1800003F
CS3#	Static memory bank 3	64 B	8, 16, 32	0x17000000	0x1700003F
CS4#	Static memory bank 4	64 B	8, 16, 32	0x16000000	0x1600003F
CS5#	Static memory bank 5	64 B	8, 16, 32	0x15000000	0x1500003F
CS6#	Static memory bank 6	64 B	8, 16, 32	0x14000000	0x1400003F

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NOTES:

1 Data width of static memory banks can be configured to 8, 16 bits by software.

2 The 8KB address space from H'1FC00000 to H'1FC01FFF in bank 0 is mapped to on-chip boot ROM. The other memory spaces in bank 0 are not used.

6.4 Static Memory Interface

NEMC provides a glueless interface to normal static memory which don't need byte control like SRAM, memory interface IO devices, etc.. It can directly control up to 6 devices using six chip select lines. Additional devices may be supported through external decoding of the address bus.

Each chip select can directly access memory or IO devices that are 8-bits or 16-bits wide. Each device connected to a chip select line has 2 associated registers that control its operation and the access timing to the external device. The Static Memory Control Register SMCRn specifies various configurations for the device. The Static Memory Address Configuration Register SACRn specifies the base address and size for each device, enabling any device to be located anywhere in the physical address range.

The static memory interface includes the following signals:

- Six chip selects, CS6~1#
- Six address signals, SA5-SA0
- One read enable, RD#
- One write enable, WE#
- One wait pin, WAIT#

The SMT field in SMCRn registers specifies the type of memory and BW field specifies the bus width. BOOT_SEL[1:0] pin defines whether system boot from Nor or Nand flash and the page size when boot from Nand flash.

6.4.1 Register Description

Table 6-4 Static Memory Interface Registers

Name	Description	RW	Reset Value	Address	Access Width
SMCR1	Static memory control register 1	RW	0x0FFF7700	0x13410014	32
SMCR2	Static memory control register 2	RW	0x0FFF7700	0x13410018	32
SMCR3	Static memory control register 3	RW	0x0FFF7700	0x1341001C	32
SMCR4	Static memory control register 4	RW	0x0FFF7700	0x13410020	32
SMCR5	Static memory control register 5	RW	0x0FFF7700	0x13410024	32
SMCR6	Static memory control register 6	RW	0x0FFF7700	0x13410028	32
SACR1	Static memory bank 1 address configuration register	RW	0x00001AFE	0x13410034	32
SACR2	Static memory bank 2 address configuration register	RW	0x000018FE	0x13410038	32
SACR3	Static memory bank 3 address	RW	0x000017FF	0x1341003C	32

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	configuration register				
SACR4	Static memory bank 4 address configuration register	RW	0x000016FF	0x13410040	32
SACR5	Static memory bank 5 address configuration register	RW	0x000015FF	0x13410044	32
SACR6	Static memory bank 6 address configuration register	RW	0x000014FF	0x13410048	32

6.4.1.1 Static Memory Control Register (SMCR1~6)

SMCR1~6 are 32-bit read/write registers that contain control bits for static memory. On reset, SMCR1~6 are initialized to 0x0FFF7700.

SMCR1 **0x13410014**
SMCR2 **0x13410018**
SMCR3 **0x1341001C**
SMCR4 **0x13410020**
SMCR5 **0x13410024**
SMCR6 **0x13410028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			STRV					TAW				TBP				TAH				TAS				BW		Reserved			BL		SMT
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	STRV	**Static Memory Recovery Time.** Its value is the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank. Its initial value is 0xF (15 cycles).	RW
23:20	TAW	**Access Wait Time.** For normal memory, these bits specify the number of wait cycles to be inserted in read strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in first data read strobe time. **TAW3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled	RW

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		0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	
19:16	TBP	**Burst Pitch Time.** For burst ROM, these bits specify the number of wait cycles to be inserted in subsequent access. For normal memory, these bits specify the number of wait cycles to be inserted in write strobe time. **TBP3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	RW
15	Reserved	Writing has no effect, read as zero.	R
15:12	TAH	**Address Hold Time.** These bits specify the number of wait cycles to be inserted from negation of read/write strobe to address. **TAH2~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value)	RW

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		1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
11	Reserved	Writing has no effect, read as zero.	R
11:8	TAS	**Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of read/write strobe. **TAS2~0 Wait cycle** 000 0 cycle 001 1 cycle 010 2 cycles 011 3 cycles 100 4 cycles 101 5 cycles 110 6 cycles 111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
7:6	BW	**Bus Width.** These bits specify the bus width. this filed is writeable and are initialized to 0 by a reset. **BW1~0 Bus Width** 00 8 bits (Initial Value) 01 16 bits 10 Reserved 11 Reserved	RW
5:3	Reserved	Writing has no effect, read as zero. **NOTE:** Don't write Bit3 to 1.	R
2:1	BL	**Burst Length (BL1, BL0).** When Burst ROM is connected; these bits specify the number of burst in an access. These bits are only valid when SMT is set to 1. **BL1~0 Burst Length**	

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		00 4 consecutive accesses. Can be used with 8- or 16-bit bus width (Initial Value) 01 8 consecutive accesses. Can be used with 8- or 16-bit bus width 10 16 consecutive accesses. Can only be used with 8- or 16-bit bus width 11 32 consecutive accesses. Can only be used with 8-bit bus width	
0	SMT	**Static Memory Type (SMT).** This bit specifies the type of static memory. **SMT Description** 0 Normal Memory (Initial Value) 1 Burst ROM	RW

6.4.1.2 Static Bank Address Configuration Register (SACR1~6)

SACR1~6 defines the physical address for static memory bank 1 to 6, respectively. Each register contains a base address and a mask. When the following equation is met:

(*physical_address* [31:24] & **MASK$_n$**) == **BASE$_n$**

The bank n is active. The *physical_address* is address output on internal system bus. Static bank regions must be programmed so that each bank occupies a unique area of the physical address space. Programming overlapping bank regions will result in unpredictable error. These registers are initialized by a reset.

SACR1 **0x13410034**
SACR2 **0x13410038**
SACR3 **0x1341003C**
SACR4 **0x13410040**
SACR5 **0x13410044**
SACR6 **0x13410048**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	0
RST2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0
RST3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
RST4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1
RST5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
RST6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	**Address Base:** Defines the base address of Static Bank n (n = 1 to 6).	RW

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		The initial values are: SACR1.BASE 0x1A SACR2.BASE 0x18 SACR3.BASE 0x17 SACR4.BASE 0x16 SACR5.BASE 0x15 SACR6.BASE 0x14	
23:20	MASK	**Address Mask**: Defines the mask of Static Bank n (n = 1 to 6). The initial values are: SACR1.MASK 0xFE SACR2.MASK 0xFE SACR3.MASK 0xFF SACR4.MASK 0xFF SACR5.MASK 0xFF SACR6.MASK 0xFF	RW

6.4.2 Example of Connection

Following figures shows examples of connection to 16- and 8-bit data width normal memory.

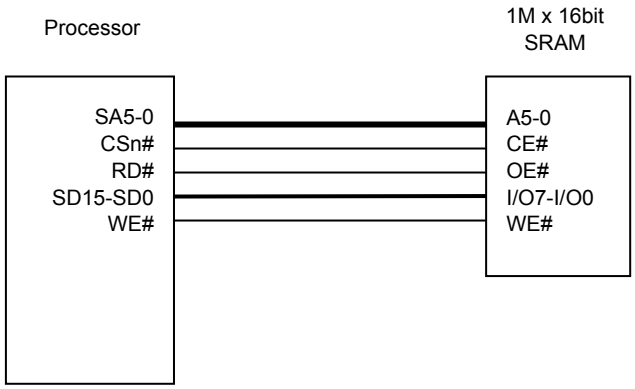


Figure 6-2 Example of 16-Bit Data Width SRAM Connection

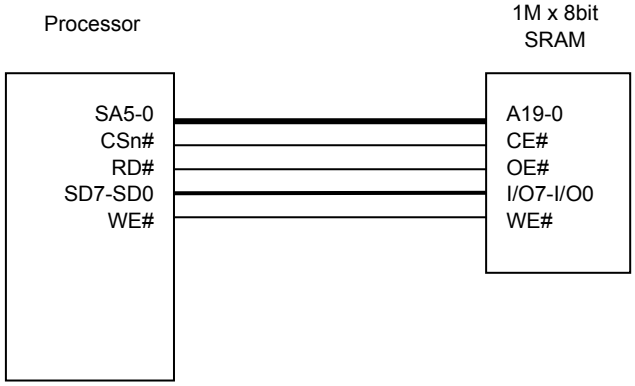


Figure 6-3 Example of 8-Bit Data Width SRAM Connection

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6.4.3 Basic Interface

When SMT field in SMCRn (n = 1 to 6) is 0, normal memory (non-burst ROM, Flash, normal SRAM or memory-like device) is connected to bank n. When bank n (n = 1 to 6) is accessed, CSn# is asserted as soon as address is output. In addition, the RD# signal, which can be used as OE#, and write control signals WE# is asserted.

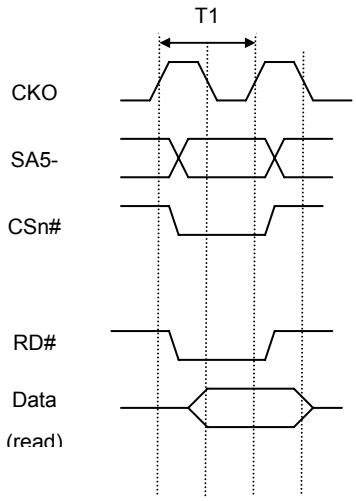
The TAS field in SMCRn is the latency from CSn# to read/write strobe. The TAW3 field is the delay time of RD# in read access. TBP3~0 field is the delay time of WE# and WEn# in write access. In addition, any number of waits can be inserted by means of the external pin (WAIT#). The TAH field is the latency from RD# and WEn# negation to CSn# negation, also the hold time to address and write data.

All kinds of normal memories (non-burst ROM, normal SRAM and Flash) have the same read and write timing. There are some requirements for writes to flash memory. Flash memory space must be un-cacheable and un-buffered. Writes must be exactly the width of the populated Flash devices on the data bus (no byte writes or word writes to a 16-bit bus, and so on). Software is responsible for partitioning commands and data, and writing them out to Flash in the appropriate sequence.

Glossary

Th – hold cycle
Tw – wait cycle
Ts – setup cycle
T1 – read inherent cycle or first write inherent cycle
T2 – last write inherent cycle
Tb – burst read inherent cycle

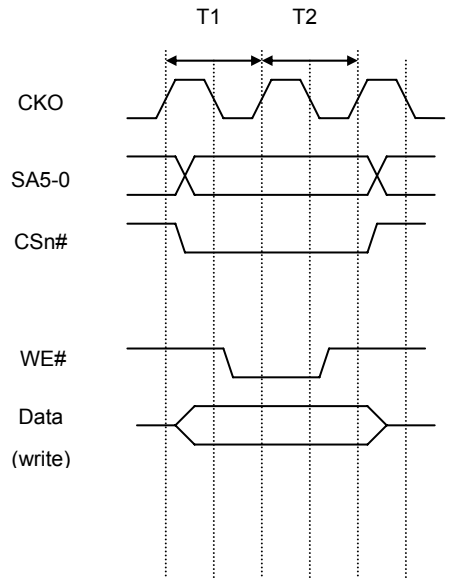
Following figures show the timing of normal memory. A no-wait read access is completed in one cycle and a no-wait write access is completed in two cycles. Therefore, there is no negation period in case of access at minimum pitch.



*In this example, SMCRn:MT = 0, TAS = 0, TAW = 0, TAH = 0

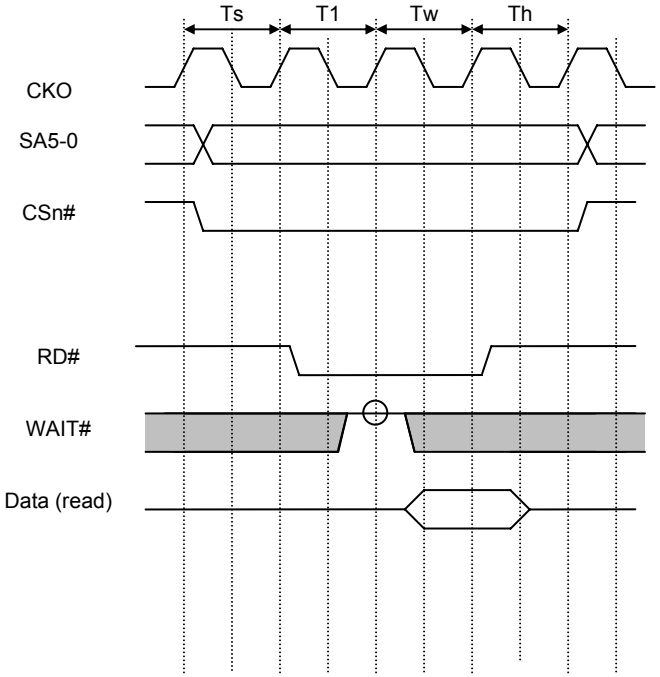
Figure 6-4 Basic Timing of Normal Memory Read

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*In this example, SMCRn: SMT = 0, TAS = 0,
TBP = 0, TAH = 0

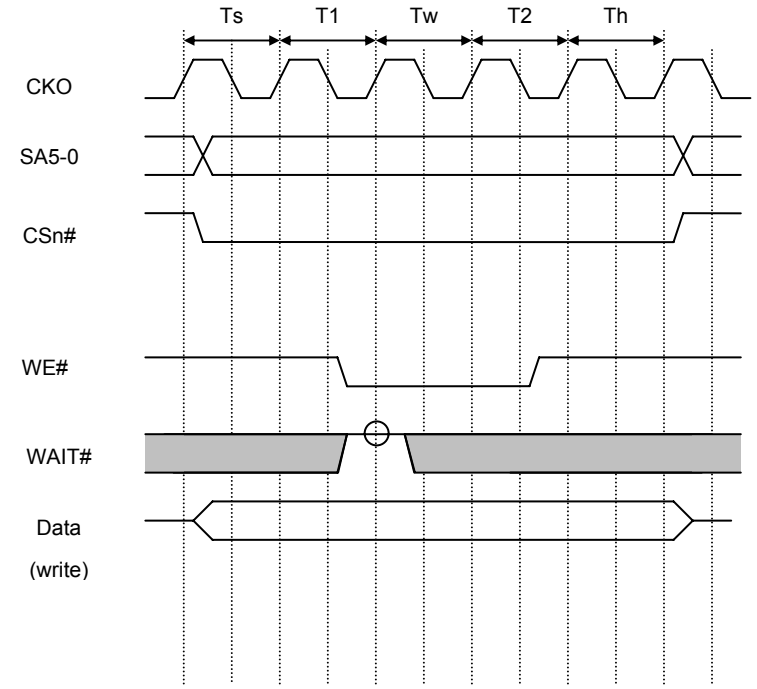
Figure 6-5 Basic Timing of Normal Memory Write



*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH = 1

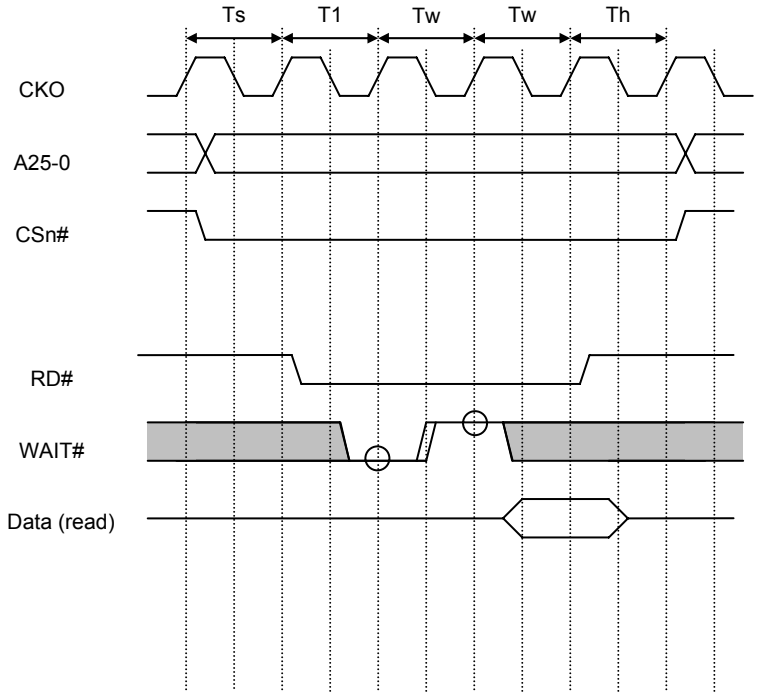
Figure 6-6 Normal Memory Read Timing With Wait (Software Wait Only)

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*In this example, SMCRn: SMT = 0, TAS = 1, TBP = 1, TAH = 1

Figure 6-7 Normal Memory Write Timing With Wait (Software Wait Only)



*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH=1

Figure 6-8 Normal Memory Read Timing With Wait (Wait Cycle Insertion by WAIT# pin)

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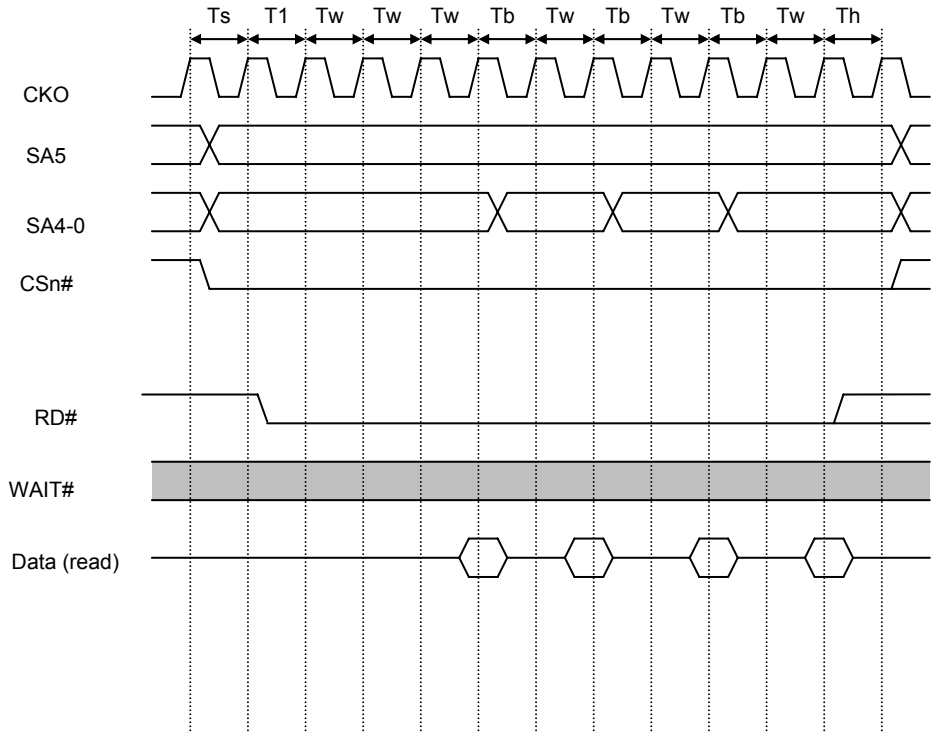
6.4.4 Burst ROM Interface

Setting SMT to 1 in SMCRn allows burst ROM to be connected to bank n (n = 1 to 6). The burst ROM interface provides high-speed access to ROM that has a nibble access function. Basically, access is performed in the same way as for normal memory, but when the first cycle ends, only the address is changed before the next access is executed. When 8-bit burst ROM is connected, the number of consecutive accesses can be set as 4, 8, 16, or 32 with bits BL1~0. When 16-bit ROM is connected, 4, 8, or 16 can be set in the same way.

For burst ROM read, TAW sets the delay time from read strobe to the first data, TBP sets the delay time from consecutive address to data. Burst ROM writes have the same timing as normal memory except TAW instead of TBP is used to set the delay time of write strobe.

WAIT# pin sampling is always performed when one or more wait states are set.

Following figures show the timing of burst ROM.



*In this example, SMT = 1, BL = 0, TAS = 1, TAW = 3,TBP = 1,TAH = 1

Figure 6-9 Burst ROM Read Timing (Software Wait Only)

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6.5 NAND Flash Interface

NAND flash can be connected to static memory bank 6~ band 1. Both 8-bit and 16-bit NAND flashes are supported. A mechanism for booting from NAND flash is also supported.

6.5.1 Register Description

Table 6-5 NAND Flash Interface Registers

Name	Description	RW	Reset Value	Address	Access Width
NFCSR	NAND flash control/status register	RW	0x00000000	0x13410050	32
PNCR	NAND PN control register	RW	0x00000000	0x13410100	32
PNDR	NAND PN data register	RW	0x00005AA5	0x13410104	32
BITCNT	NAND bit counter	R	0x00000000	0x13410108	32

6.5.1.1 NAND Flash Control/Status Register (NFCSR)

NFCSR is a 32-bit read/write register that is used to configure NAND flash. It is initialized by any reset.

NFCSR **0x13410050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				NFCE6	NFE6	NFCE5	NFE5	NFCE4	NFE4	NFCE3	NFE3	NFCE2	NFE2	NFCE1	NFE1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
1/3/5/7/9/11	FCEn (n=1,2,3,4,5,6)	**NAND Flash FCE# Assertion Control :** Controls the assertion of NAND Flash FCEn#. When set, FCEn# is always asserted until this bit is cleared. When the NAND flash require FCEn# to be asserted during read busy time, this bit should be set. **FCE** **Description** 0 FCEn# is asserted as normal static chip enable(Initial value) 1 FCEn# is always asserted	RW
0/2/4/6/8/10	NFEn (n=1,2,3,4,5,6)	**NAND Flash Enable:** Specifies if NAND flash is connected to static bank n. When system is configured to boot from NAND flash, this bit is initialized to 1. **NFE** **Description** 0 Static bank n is not used as NAND flash 1 Static bank n is used as NAND flash	RW

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6.5.1.2 NAND PN Control Register (PNCR)

PNCR is a 32-bit read/write register that is used to control NAND flash data randomization. It is initialized by any reset.

PNCR **0x13410100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										BIT_RST	BIT_SEL	BIT_EN	Reserved	PNRST	PNEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	BIT_RST	**NAND BIT Counter Reset:** Reset Bit counter. When this bit is written to 1, the bit counter is reset to 0. This bit is write-only.	W
4	BIT_SEL	**NAND BIT Counter Select:** Bit counter's counting select. **BIT_SEL Description** 0 Calculate number of "0" in NAND read data 1 Calculate number of "1" in NAND read Data	RW
3	BIT_EN	**NAND BIT Counter Enable:** Enable/disable bit counter counting. **BIT_EN Description** 0 Bit counting is disabled 1 Bit counting is enabled	RW
2	Reserved	Writing has no effect, read as zero.	R
1	PNRST	**NAND Flash PN Reset:** Reset seed of randomizer. When this bit is written to 1, the seed of randomizer is reset. This bit is write-only.	W
0	PNEN	**NAND Flash PN Enable:** Specifies if NAND flash read/write data randomization is enabled. This bit is initialized to 0. **PNEN Description** 0 Data randomization is disabled 1 Data randomization is enabled	RW

6.5.1.3 NAND PN Data Register (PNDR)

PNDR is a 23-bit read/write register that is used for seed of randomizer during NAND read/write.

PNDR **0x13410104**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									PNDR																						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1

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6.5.1.4 NAND Bit Counter (BITCNT)

BITCNT is a 32-bit read/write register that is used to counting the number of “1” or “0” (based on BIT_SEL) in Nand read data and keep counting during Nand read till BIT Counter Reset. It is initialized by any reset.

BITCNT																															0x13410108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BITCNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.5.2 NAND Flash Boot Loader

To support boot from NAND flash, 8KB on-chip Boot ROM is implemented. Following figure illustrates the structure of NAND Flash Boot Loader.

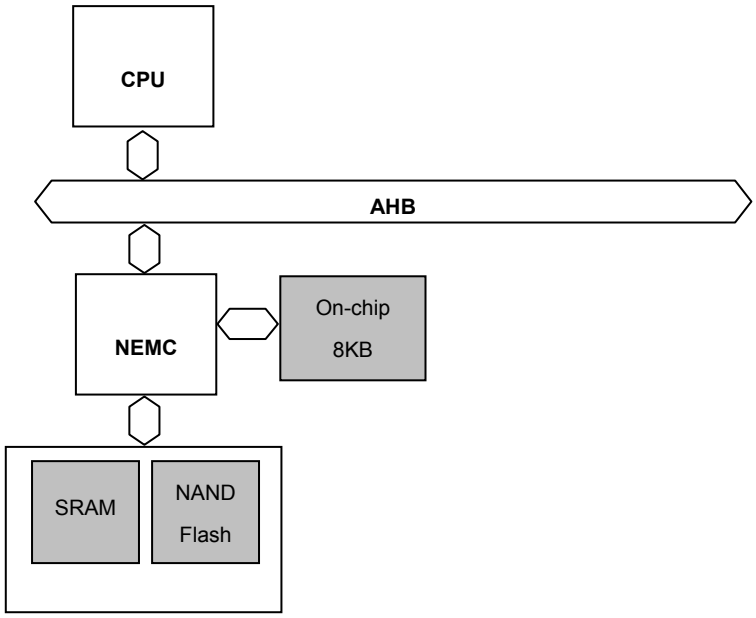


Figure 6-10 Structure of NAND Flash Boot Loader

When system is configured to boot from NAND flash, after reset, the program in Boot ROM is executed and the program will copy the first 8K bytes of NAND flash to internal memory for further initialization.

Generally, the boot code will copy more NAND flash content to DRAM. Then the main program will be executed on DRAM.

When system is configured to boot from NAND flash, software may know the nand flash page size through BOOT_SEL[2:0] pin.

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6.5.3 NAND Flash Operation

Set NFEn bit of NAND Flash Control/Status Register (NFCSR) will enable access to NAND flash. The partition of static bank n (n=1~6) is changed as following figure. Writes to any of address space will be translated to NAND flash address cycle. Writes to any of command space will be translated to NAND flash command cycle. **CAUTION:** don't read to address and command space, and these two partitions should be uncacheable. Reads and writes to any of data space will be translated to NAND flash data read/write cycle. DMA access to data space is supported to increase the speed of data read/write. The DMA access cannot exceed the page boundary (512 bytes or 2K bytes) of NAND.

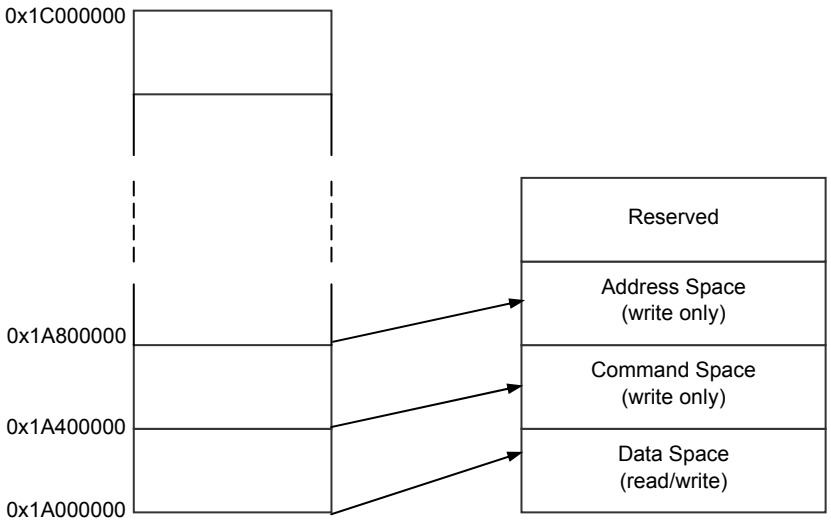


Figure 6-11 Static Bank 1 Partition When NAND Flash is Used (an example)

The timing of NAND flash access is configured by SMCRn and is same as normal static memory timing, except that CSn# is controlled by NFCE bit NFCSR. CSn# is always asserted when NFCE is 1. When NFCE is 0, CSn# is asserted as normal static memory access.

The control signals for direction connection of NAND flash are CSn#, FRE#, FWE#, FRB#(GPIO), A1 and A0. Following figure shows the connection between processor and NAND Flash.

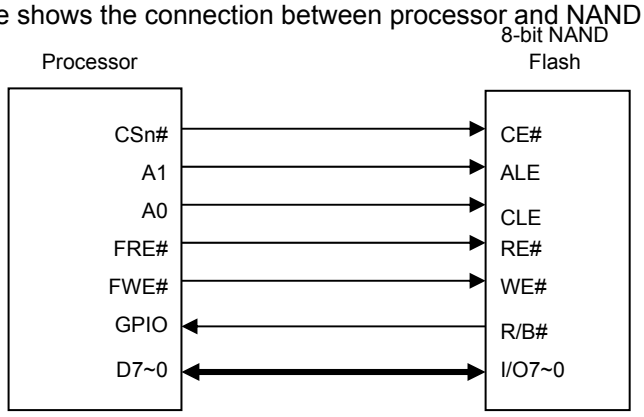


Figure 6-12 Example of 8-bit NAND Flash Connection

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7 BCH Controller

7.1 Overview

The BCH Controller implements data ECC encoding and decoding.

7.2 Register Description

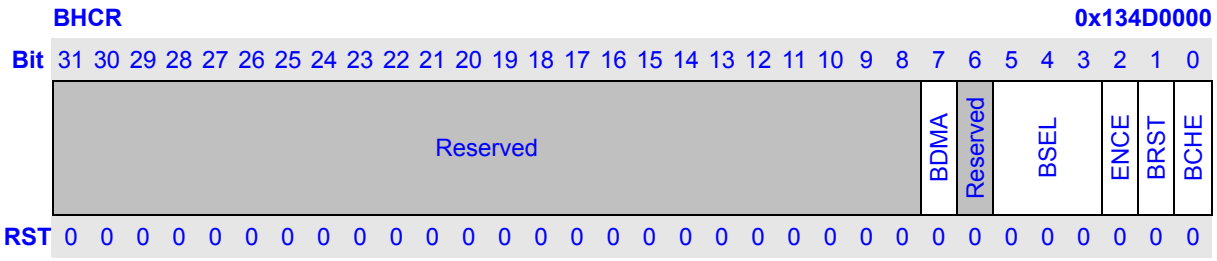
Table 7-1 BCH Registers

Name	Description	RW	Reset Value	Address	Access Width
BHCR	BCH Control register	R	0x00000000	0x134D0000	32
BHCSR	BCH Control Set register	W	Undefined	0x134D0004	32
BHCCR	BCH Control Clear register	W	Undefined	0x134D0008	32
BHCNT	BCH ENC/DEC Count register	RW	0x00000000	0x134D000C	32/16
BHDR	BCH data register	W	Undefined	0x134D0010	8
BHPAR0	BCH Parity 0 register	RW	0x00000000	0x134D0014	32/16/8
BHPAR1	BCH Parity 1 register	RW	0x00000000	0x134D0018	32/16/8
BHPAR2	BCH Parity 2 register	RW	0x00000000	0x134D001C	32/16/8
BHPAR3	BCH Parity 3 register	RW	0x00000000	0x134D0020	32/16/8
BHPAR4	BCH Parity 4 register	RW	0x00000000	0x134D0024	32/16/8
BHPAR5	BCH Parity 5 register	RW	0x00000000	0x134D0028	32/16/8
BHPAR6	BCH Parity 6 register	RW	0x00000000	0x134D002C	32/16/8
BHPAR7	BCH Parity 7 register	RW	0x00000000	0x134D0030	32/16/8
BHPAR8	BCH Parity 8 register	RW	0x00000000	0x134D0034	32/16/8
BHPAR9	BCH Parity 9 register	RW	0x00000000	0x134D0038	32/16/8
BHERR0	BCH Error Report 0 register	R	0x00000000	0x134D003C	32/16
BHERR1	BCH Error Report 1 register	R	0x00000000	0x134D0040	32/16
BHERR2	BCH Error Report 2 register	R	0x00000000	0x134D0044	32/16
BHERR3	BCH Error Report 3 register	R	0x00000000	0x134D0048	32/16
BHERR4	BCH Error Report 4 register	R	0x00000000	0x134D004C	32/16
BHERR5	BCH Error Report 5 register	R	0x00000000	0x134D0050	32/16
BHERR6	BCH Error Report 6 register	R	0x00000000	0x134D0054	32/16
BHERR7	BCH Error Report 7 register	R	0x00000000	0x134D0058	32/16
BHERR8	BCH Error Report 8 register	R	0x00000000	0x134D005C	32/16
BHERR9	BCH Error Report 9 register	R	0x00000000	0x134D0060	32/16
BHERR10	BCH Error Report 10 register	R	0x00000000	0x134D0064	32/16
BHERR11	BCH Error Report 11 register	R	0x00000000	0x134D0068	32/16
BHINT	BCH Interrupt Status register	R	0x00000000	0x134D006C	32
BHINTE	BCH Interrupt Enable register	RW	0x00000000	0x134D0070	32
BHINTES	BCH Interrupt Set register	W	Undefined	0x134D0074	32
BHINTEC	BCH Interrupt Clear register	W	Undefined	0x134D0078	32

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7.2.1 BCH Control Register (BHCR)

BHCR is a 32-bit read/write register that is used to configure BCH controller. It is initialized by any reset.



Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	BDMA	**BCH DMA Enable**: It is used to enable or disable dma transfer during correction. **BDMA** **Description** 0 DMA transfer is disabled (Initial value) 1 DMA transfer is enabled	RW
6	Reserved	Writing has no effect, read as zero.	R
5:3	BSEL	**BCH Encoding/Decoding Bit Select**: It is used to select the correction algorithm among 4-bit, 8-bit, 12-bit, 16-bit, 20-bit and 24-bit BCH. **BSEL** **Description** 000 4-bit correction (initial value) 001 8-bit correction 010 12-bit correction 011 16-bit correction 100 20-bit correction 101 24-bit correction	
2	ENCE	**BCH Encoding/Decoding Select**: It is used to define whether in encoding or in decoding phase when BCH is used. **ENCE** **Description** 0 Decoding (Initial value) 1 Encoding	RW
1	BRST	**BCH Reset:** It is used to reset BCH controller. This bit is cleared automatically by hardware and always read as 0. **BRST** **Description** 0 BCH controller is not reset (Initial value) 1 BCH controller is reset	W
0	BCHE	**BCH Enable:** BCH correction is enable/disable. **BCHE** **Description** 0 BCH is disabled (initial value) 1 BCH is enabled	RW

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7.2.2 BCH Control Set Register (BHCSR)

BHCSR is a 32-bit write-only register that is used to set BCH controller to 1.

When write 1 to BHCSR, the corresponding bit in BHCR register is set to 1. Write 0 to BHCSR is ignored.

BHCSR **0x134D0004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								BDMAS		BSELS			ENCES	BRSTS	BCHES
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	BDMAS	**BCH DMA Enable Set**: It is used to set BHCR.BDMA to 1.	W
6	Reserved	Writing has no effect, read as zero.	R
5:3	BSELS	**BCH Encoding/Decoding Bit Select Set**: It is used to set BHCR.BSEL to 1.	W
2	ENCES	**BCH Encoding/Decoding Select Set**: It is used to set BHCR.ENCE to 1.	W
1	BRSTS	**BCH Reset Set:** It is used to set BHCR.BRST to 1.	W
0	BCHES	**BCH Enable Set:** It is used to set BHCR.BCHE to 1.	W

7.2.3 BCH Control Clear Register (BHCCR)

BHCCR is a 32-bit write-only register that is used to clear BCH controller to 0.

When write 1 to BHCCR, the corresponding bit in BHCR register is cleared to 0. Write 0 to BHCCR is ignored.

BHCCR **0x134D0008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								BDMAC	Reserved	BSELC			ENCEC	BRSTC	BCHEC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	BDMAC	**BCH DMA Enable Clear**: It is used to clear BHCR.BDMA to 0.	W
6	Reserved	Writing has no effect, read as zero.	R
5:3	BSELC	**BCH Encoding/Decoding Bit Select Clear**: It is used to clear BHCR.BSEL to 0.	W

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2	ENCEC	**BCH Encoding/Decoding Select Clear**: It is used to clear BHCR.ENCE to 0.	W
1	Reserved	Writing has no effect, read as zero.	R
0	BCHEC	**BCH Enable Clear:** It is used to clear BHCR.BCHE to 0.	W

7.2.4 BCH ENC/DEC Count Register (BHCNT)

BCHCNT is a 32-bit read/write register that is used to indicate the total number of 4-bit data during encoding or decoding. It is initialized by any reset.

BHCNT **0x134D000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										DEC Count						Reserved					ENC Count											
RST	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	DEC Count	**DEC Count**: It is used to indicate total 4-bit data count in BCH decoding which includes data + parity. For example, total data + parity is 538 bytes, the field of DEC Count should be set to ‘h434 which is the initial value.	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	ENC Count	**ENC Count**: It is used to indicate total byte count in BCH encoding which just includes 4-bit data and should be less and equal to 1996 4-bit (which is equal to 998 Bytes) when 16-bit BCH is selected.	RW

7.2.5 BCH Data Register (BHDR)

BHDR is an 8-bit write-only register that is used to transfer ecc data to BCH.

BHDR **0x134D0010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								BCHDR							
RST	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	X	x	x	X

7.2.6 BH Parity Register (BHPARn, n=0,1,2,3,4,5,6,7,8,9)

BHPARn (n=0,1,2,3,4,5,6,7,8,9) are all 32-bit read/write register that contains the encoding parity data during BCH correction. It is initialized by any reset and BRST of BHCR.

When 24-bit BCH is selected, BHPAR0~BHPAR9 consist of the 312 bits of parity data and bit 0 of

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BHPAR0 is the 312th bit of parity data and bit 23 of BHPAR9 is the 1st bit of parity data.

When 20-bit BCH is selected, BHPAR0~BHPAR8 consist of the 260 bits of parity data, and bit 0 of BHPAR0 is the 260th bit of parity data and bit 3 of BHPAR8 is the 1st bit of parity data.

When 16-bit BCH is selected, BHPAR0~BHPAR6 consist of the 208 bits of parity data, and bit 0 of BHPAR0 is the 208th bit of parity data and bit 15 of BHPAR6 is the 1st bit of parity data.

When 12-bit BCH is selected, BHPAR0~BHPAR4 consist of the 156 bits of parity data, and bit 0 of BHPAR0 is the 156th bit of parity data and bit 27 of BHPAR4 is the 1st bit of parity data.

When 8-bit BCH is selected, BHPAR0~BHPAR3 consist of the 104 bits of parity data and bit 0 of BHPAR0 is the 104th bit of parity data and bit 7 of BHPAR3 is the 1st bit of parity data.

Similarly, when 4-bit BCH is selected, the two parity register, BHPAR0 and BHPAR1 together consist of the 52 bits of parity data and bit 0 of BHPAR0 is the 52th bit of parity data and bit 19 of BHPAR1 is the 1st bit of parity data.

BHPAR0		**0x134D0014**
BHPAR1		**0x134D0018**
BHPAR2		**0x134D001C**
BHPAR3		**0x134D0020**
BHPAR4		**0x134D0024**
BHPAR5		**0x134D0028**
BHPAR6		**0x134D002C**
BHPAR7		**0x134D0030**
BHPAR8		**0x134D0034**
BHPAR9		**0x134D0038**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BHPAR0~BHPAR9																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.2.7 BCH Error Report Register (BCHERRn, n=0,1,2,3,4,5,6,7,8,9,10,11)

BCHERRn is 32-bit read/write register that contains the index for each error after BCH decoding. It is initialized by any reset and BRST of BCHCR.

BCHERR0 contains INDEX1 and INDEX0.
BCHERR1 contains INDEX3 and INDEX2.
BCHERR2 contains INDEX5 and INDEX4.
BCHERR3 contains INDEX7 and INDEX6.
BCHERR4 contains INDEX9 and INDEX8.
BCHERR5 contains INDEX11 and INDEX10.
BCHERR6 contains INDEX13 and INDEX12.
BCHERR7 contains INDEX15 and INDEX14.

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BCHERR8 contains INDEX17 and INDEX16.
BCHERR9 contains INDEX19 and INDEX18.
BCHERR10 contains INDEX21 and INDEX20.
BCHERR11 contains INDEX23 and INDEX22.

BCHERR0 **0x134D003C**
BCHERR1 **0x134D0040**
BCHERR2 **0x134D0044**
BCHERR3 **0x134D0048**
BCHERR4 **0x134D004C**
BCHERR5 **0x134D0050**
BCHERR6 **0x134D0054**
BCHERR7 **0x134D0058**
BCHERR8 **0x134D005C**
BCHERR9 **0x134D0060**
BCHERR10 **0x134D0064**
BCHERR11 **0x134D0068**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reserved															
									INDEXn(n=1,3,5,7,9,11,13,15,17,19,21,23)														INDEXn(n=0,2,4,6,8,10,12,14,16,18,20,22)									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:16	INDEXn	**Error Bit Index:** It is used to indicate the location of the error bit. For example, INDEX=2, it means the second bit is an error bit.	R
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	INDEXn	**Error Bit Index:** It is used to indicate the location of the error bit. For example, INDEX=2, it means the second bit is an error bit.	R

7.2.8 BCH Interrupt Status Register (BHINT)

BHINT is a 32-bit read-only register that contains the interrupt flag and error count information during BCH correction. It is initialized by any reset. Software write 1 to clear the corresponding bit except ERRC.

BHINT **0x134D006C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERRC																Reserved												ALL_f	DECF	ENCF	UNCOR	ERR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:27	ERRC	**Error Count:** It indicates the number of errors in the data block and these bits are also reset by BHCR.BRST bit. **ERRC Description** 0 No errors or uncorrection error occurs (Initial value) 1 One error in the data block 2 Two errors in the data block 3 Three errors 4 Four errors 5 Five errors 6 Six errors 7 Seven errors 8 Eight errors … 24 Twenty-four errors	R
27:5	Reserved	Writing has no effect, read as zero.	R
4	ALL_f	**ALL_f:** It indicates that all data received during decoding are 0xf. When receiving all 0xf data, BCH doesn't correct the data and no error occurs. **ALL_f Description** 0 Not all data (data + parity bytes) are 0xf (Initial value) 1 All data (data + parity bytes) are 0xf	R
3	DECF	**Decoding Finish:** It indicates that hardware finish BCH decoding. **DECF Description** 0 Decoding not Finish (Initial value) 1 Decoding Finish	R
2	ENCF	**Encoding Finish:** It indicates that hardware finish BCH encoding. **ENCF Description** 0 Encoding not Finish (Initial value) 1 Encoding Finish	R
1	UNCOR	**Uncorrection Error:** It indicates that hardware finish BCH encoding. **UNCOR Description** 0 No uncorrectable error (Initial value) 1 Uncorrectable error occur	R
0	ERR	**Error:** It indicates that hardware detects error bits in data in the data block during BCH decoding. **ERR Description** 0 No error (Initial value) 1 Error occur	R

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7.2.9 BCH Interrupt Enable Set Register (BHINTES)

BHINTES is a 32-bit write-only register that is used to set BHINTE register. Writing 1 to BHINTES will set the corresponding bit in BHINTE to 1. Writing 0 to BHINTES is ignored.

BHINTES **0x134D0074**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											ALL_FES	DECFES	ENCFES	UNCORES	ERRES
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	ALL_FES	**ALL_F Interrupt Enable Set:** It is used to set BHINTE.ALL_FE to 1.	W
3	DECFES	**Decoding Finish Interrupt Enable Set:** It is used to set BHINTE.DECFE to 1.	W
2	ENCFES	**Encoding Finish Interrupt Enable Set:** It is used to set BHINTE.ENCFE to 1.	W
1	UNCORES	**Uncorrection Error Interrupt Enable Set:** It is used to set BHINTE.ENCFE to 1.	W
0	ERRES	**Error Interrupt Enable Set:** It is used to set BHINTE.ERRE to 1.	W

7.2.10 BCH Interrupt Enable Clear Register (BHINTEC)

BHINTEC is a 32-bit write-only register that is used to clear BHINTE register. Writing 1 to BHINTEC will clear the corresponding bit in BHINTE to 0. Writing 0 to BHINTEC is ignored.

BHINTEC **0x134D0078**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											ALL_FEC	DECFEC	ENCFEC	UNCORC	ERREC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	ALL_FEC	**ALL_F Interrupt Enable Clear:** It is used to clear BHINTE.ALL_FE to 0.	W
3	DECFEC	**Decoding Finish Interrupt Enable Clear:** It is used to clear BHINTE.DECFE to 0.	W
2	ENCFEC	**Encoding Finish Interrupt Enable Clear:** It is used to clear BHINTE.ENCFE to 0.	W

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1	UNCOREC	**Uncorrection Error Interrupt Enable Clear:** It is used to clear BHINTE.ENCFE to 0.	W
0	ERREC	**Error Interrupt Enable Clear:** It is used to set BHINTE.ERRE to 0.	W

7.2.11 BCH Interrupt Enable Register (BHINTE)

BHINTE is a 32-bit read/write register that is used to enable/disable interrupts during BCH correction. It is initialized by any reset.

BHINTE **0x134D0070**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											ALL_FE	DECFE	ENCFE	UNCORE	ERRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	ALL_FE	**ALL_F Interrupt Enable:** It is used enable or disable all_f data interrupt. **ALL_FE Description** 0 Disable ALL_F data interrupt (Initial value) 1 Enable ALL_F data interrupt	RW
3	DECFE	**Decoding Finish Interrupt Enable:** It is used to enable or disable decoding finish interrupt. **DECFE Description** 0 Disable Decoding Finish Interrupt (Initial value) 1 Enable Decoding Finish Interrupt	RW
2	ENCFE	**Encoding Finish Interrupt Enable:** It is used to enable or disable encoding finish interrupt. **ENCFE Description** 0 Disable Encoding Finish Interrupt (Initial value) 1 Enable Encoding Finish Interrupt	RW
1	UNCORE	**Uncorrection Error Interrupt Enable:** It is used to enable or disable uncorrection error interrupt. **UNCORE Description** 0 Disable Uncorrectable Error interrupt (Initial value) 1 Enable Uncorrectable Error Interrupt	RW
0	ERRE	**Error Interrupt Enable:** It is used to enable or disable error interrupt. **ERRE Description** 0 Disable Error interrupt (Initial value) 1 Enable Error interrupt	RW

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7.3 BCH Operation

BCH controller uses BCH(n, k) codes. Here n is less and equal to 8191-bit and k is less and equal to 7879-bit in 24-bit correction, 7931-bit in 20-bit correction, 7983-bit in 16-bit correction, 8035-bit in 12-bit correction, 8087-bit in 8-bit correction and 8139-bit in 4-bit correction. During encoding, hardware will generate 312-bit parity data in 24-bit correction, 260-bit parity data in 20-bit correction, 208-bit parity data in 16-bit correction, 156-bit parity data in 12-bit correction, 104-bit parity data in 8-bit correction or 52-bit parity data in 4-bit correction. Parity data can be read out by cpu or dma. During decoding, if there are error bits in data block, after decoding BCHERRn registers will hold the error bit location that can be read by cpu or dma.

7.3.1 Encoding Sequence

BCH encoding can be operated by cpu or dma.

7.3.1.1 CPU

1 Set BCHCR.BCHE to 1 to enable BCH controller.
2 Select 24-bit, 20-bit, 16-bit, 12-bit, 8-bit or 4-bit correction by setting BCHCR.BSEL.
3 Set BCHCR.ENCE to 1 to enable encoding.
4 Set BCHCR.BRST to 1 to reset BCH controller.
5 Set BCHCNT.ENC_COUNT to data block size in bytes.
6 Byte-write all data block to BCHDR.
7 Check BCHINTS.ENCF bit or by enabling encoding finish interrupt.
8 When encoding finishes, read out the parity data in BCHPARn.

7.3.1.2 DMA

1 Set BCHCR.BCHE to 1 to enable BCH controller.
2 Select 24-bit, 20-bit, 16-bit, 12-bit, 8-bit or 4-bit correction by setting BCHCR.BSEL.
3 Set BCHCR.ENCE to 1 to enable encoding.
4 Set BCHCR.BRST to 1 to reset BCH controller.
5 Set BCHCNT.ENC_COUNT to data block size in bytes.
6 Set BCHCR.BDMA to 1 to select DMA transfer.
7 Start DMA transfer after configuring DMA channel.
8 DMA read data block from system memory and write to BCH controller automatically.
9 DMA will wait BCH encoding request when finishes writing data block.
10 BCH controller will issue encoding request to DMA when encoding ends.
11 DMA start to read out parity data.
12 After parity data is read out, BCH automatically reset itself and clear BCHINT.ENCF.

NOTE: When DMA is enabled, software should guarantee not to enable encoding finish interrupt.

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7.3.2 Decoding Sequence

BCH decoding can be operated by cpu or dma.

7.3.2.1 CPU

1 Set BCHCR.BCHE to 1 to enable BCH controller.
2 Select 24-bit, 20-bit, 16-bit, 12-bit, 8-bit or 4-bit correction by setting BCHCR.BSEL.
3 Clear BCHCR.ENCE to 0 to enable decoding.
4 Set BCHCR.BRST to 1 to reset BCH controller.
5 Set BCHCNT.DEC_COUNT to data block size in bytes.
6 Byte-write all data block to BCHDR.
7 Check BCHINTS.DECF bit or by enabling decoding finish interrupt.
8 When decoding finishes, read out the status in BCHINT and error report in BCHERRn.

7.3.2.2 Decoding Sequence

1 Set BCHCR.BCHE to 1 to enable BCH controller.
2 Select 24-bit, 20-bit, 16-bit, 12-bit, 8-bit or 4-bit correction by setting BCHCR.BSEL.
3 Clear BCHCR.ENCE to 0 to enable decoding.
4 Set BCHCR.BRST to 1 to reset BCH controller.
5 Set BCHCNT.DEC_COUNT to data block size in bytes.
6 Set BCHCR.BDMA to 1 to select DMA transfer.
7 Start DMA transfer after configuring DMA channel.
8 DMA read data block from system memory and write to BCH controller automatically.
9 DMA will wait BCH decoding request when finishes writing data block.
10 BCH controller will issue decoding request to DMA when decoding ends.
11 DMA start to read out bch int status and error report data and write to memory.
12 If using descriptor DMA, if the data block needs error correction, the current data block syndrome generation and last data block error correction can be executed in pipeline automatically by DMA.
13 After status and error report data is read out, BCH automatically reset itself and clear BCHINT.DECF and Error status in BCHINT.

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8 BDMA Controller

BDMA controller (BDMAC) is dedicated to transfer data between BCH, external memories and memory-mapped external devices.

8.1 Features

- Support up to 3 independent DMA channels
- Descriptor or No-Descriptor Transfer
- Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte, 32-byte or 64-byte
- Transfer number of data unit: 1 ~ 224
- Independent source and target port width: 8-bit, 16-bit, 32-bit

8.2 Register Descriptions

Table 8-1 BDMAC Registers

Name	Description	RW	Reset Value	Address	Access Size (bit)
DSA0	DMA Source Address 0	RW	0x0	0x13450000	32
DTA0	DMA Target Address 0	RW	0x0	0x13450004	32
DTC0	DMA Transfer Count 0	RW	0x0	0x13450008	32
DRT0	DMA Request Source 0	RW	0x0	0x1345000C	32
DCS0	DMA Channel Control/Status 0	RW	0x0	0x13450010	32
DCM0	DMA Command 0	RW	0x0	0x13450014	32
DDA0	DMA Descriptor Address 0	RW	0x0	0x13450018	32
DSD0	DMA Stride Address 0	RW	0x0	0x1345001C	32
DSA1	DMA Source Address 1	RW	0x0	0x13450020	32
DTA1	DMA Target Address 1	RW	0x0	0x13450024	32
DTC1	DMA Transfer Count 1	RW	0x0	0x13450028	32
DRT1	DMA Request Source 1	RW	0x0	0x1345002C	32
DCS1	DMA Channel Control/Status 1	RW	0x0	0x13450030	32
DCM1	DMA Command 1	RW	0x0	0x13450034	32
DDA1	DMA Descriptor Address 1	RW	0x0	0x13450038	32
DSD1	DMA Stride Address 1	RW	0x0	0x1345003C	32
DSA2	DMA Source Address 2	RW	0x0	0x13450040	32
DTA2	DMA Target Address 2	RW	0x0	0x13450044	32
DTC2	DMA Transfer Count 2	RW	0x0	0x13450048	32
DRT2	DMA Request Source 2	RW	0x0	0x1345004C	32
DCS2	DMA Channel Control/Status 2	RW	0x0	0x13450050	32

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DCM2	DMA Command 2	RW	0x0	0x13450054	32
DDA2	DMA Descriptor Address 2	RW	0x0	0x13450058	32
DSD2	DMA Stride Address 2	RW	0x0	0x1345005C	32
DNT0	DMA Nand Timer 0	RW	0xC	0x134500C0	32
DNT1	DMA Nand Timer 1	RW	0xC	0x134500C4	32
DNT2	DMA Nand Timer 2	RW	0xC	0x134500C8	32
DMAC1	DMA Control 1 Register	R/ W	0x0	0x13450300	32
DIRQP1	DMA Interrupt Pending 1	R	0x0	0x13450304	32
DDR1	DMA Doorbell 1 Register	RW	0x0	0x13450308	32
DDRS1	DMA Doorbell Set 1 Register	W	0x0	0x1345030C	32
DCKE1	DMA Clock Enable 1 Register	RW	0x0	0x13450310	32
DCKES1	DMA Clock Enable Set Register	W	0x0	0x13450314	32
DCKEC1	DMA Clock Enable Clear Register	W	0x0	0x13450318	32

8.2.1 DMA Source Address (DSAn, n = 0 ~ 2)

DSA0, DSA1, DSA2 **0x13450000, 0x13450020, 0x13450040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:0	SA	Source physical address.	RW

8.2.2 DMA Target Address (DTAn, n = 0 ~ 2)

DTA0, DTA1, DTA2 **0x13450004, 0x13450024, 0x13450044**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TA	Target physical address.	RW

8.2.3 DMA Transfer Count (DTCn, n = 0 ~ 2)

DTC0, DTC1, DTC2 **0x13450008, 0x13450028, 0x13450048**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	When Stride address transfer is disabled: TC holds the number of data unit to transfer and it counts down to 0 at the end. When Stride address transfer is enabled: TC composes of two parts: The lower 16 bits: the number of data unit for sub-block transfer The higher 8 bits: the number of sub-block And both the two parts count down to 0 at the end.	RW

8.2.4 DMA Request Types (DRTn, n = 0 ~ 2)

DRT0, DRT1, DRT2 **0x1345000c, 0x1345002c, 0x1345004c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														RT	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	RT	Transfer request type.	RW

Table 8-2 Transfer Request Types

RT5-0	Description
000000	Reserved.
000001	Reserved.
000010	BCH Encoding DMA request.
000011	BCH Decoding DMA request.
000100	Reserved.
000101	Reserved.
000110	NAND0 DMA request.
000111	NAND1 DMA request.
001000	Auto-request.
001001	Reserved.
001010	Reserved.
001011	Reserved.
001100	External request with DREQn. (external address ←→ external device with DACKn)
Other	Reserved.

NOTES:

1 Only auto request can be concurrently selected in all channels with different source and target address.

2 Only channel 1 and channel 2 can handle external request. Channel 2 handles external request 0, and channel 1 handles external request 1.

8.2.5 DMA Channel Control/Status (DCSn, n = 0 ~ 2)

DCS0, DCS1, DCS2 **0x13450010, 0x13450030, 0x13450050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	DES8	LASTMD	Reserved	FRBS				CDOA								Reserved				BERR					Reserved	BUERR	AR	TT	HLT	BAC	CTE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30	DES8	Descriptor 8 Word.	RW

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		0: 4-word descriptor; 1: 8-word descriptor.	
29:28	LASTMD	BCH Decoding Last Mode. 00: Last Mode 0 which means there is one descriptor for a BCH decoding block 01: Last Mode 1 which means there is two descriptor for a BCH decoding block, the last descriptor points to parity or part of data and parity 10: Last Mode 2 which means there is three descriptor for a BCH decoding block, the last descriptor points to parity data 11: reserved **NOTES:** 1 Here a BCH decoding block includes decoding data and parity. 2 LASTMD is only for channel 0.	RW
27	Reserved	Write has no effect, read as zero.	R
26:24	FRBS	FRB Pin Select. 000: GPIO Group A 27 bit as frb1 001: GPIO Group A 28 bit as frb1 010: GPIO Group A 29 bit as frb1 011: GPIO Group B 4 bit as frb1 100: GPIO Group B 5 bit as frb1 101~111: reserved **NOTE:** FRBS is only for channel 1.	RW
23:16	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. Software could know which descriptor is just completed combining with count terminate interrupt resulted by DCSn.CT. (Ignored in No-Descriptor Transfer)	RW
15:12	Reserved	Write has no effect, read as zero.	R
11:7	BERR	BCH error number. It indicates the biggest error number within a BCH decoding block during the whole descriptor chain. If it is 0, it means there is no error during the whole descriptor chain. (Only channel 0 has this field for BCH transfer)	RW
6	Reserved	Write has no effect, read as zero.	R
5	BUERR	BCH Uncorrectable Error. 0: No uncorrectable error occurs during the whole descriptor chain 1: Uncorrectable error occurs during the whole descriptor chain (Only channel 0 has this field for BCH transfer)	RW
4	AR	Address Error. 0: no address error; 1: address error.	RW
3	TT	Transfer Terminate. 0: No-Link Descriptor or No-Descriptor DMA transfer does not end	RW

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		1: No-Link Descriptor or No-Descriptor DMA transfer end	
2	HLT	DMA halt. 0: DMA transfer is in progress; 1: DMA halt.	RW
1	BAC	BCH Auto Correction. 0: BCH auto-correction is disabled 1: BCH auto-correction is enabled (Only channel 0 has this bit for BCH auto correction)	RW
0	CTE	Channel transfer enable. 0: disable; 1: enable.	RW

8.2.6 DMA Channel Command (DCMn, n = 0 ~ 2)

DCM0, DCM1, DCM2 **0x13450014, 0x13450034, 0x13450054**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EACKS	EACKM	ERDM		Reserved		BLAST	Reserved	SAI	DAI	Reserved						SP		DP		Reserved		TSZ		NRD	NWR	NAC	Reserved		STDE	TIE	LINK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	EACKS	External DACK Output Level Select. 0: active high; 1: active low.	RW
30	EACKM	External DACK Output Mode Select. 0: output in read cycle; 1: output in write cycle.	RW
29:28	ERDM	External DREQ Detection Mode Select. 00: Low level detection 01: Falling edge detection 10: High level detection 11: Rising edge detection	RW
27:26	Reserved	Write has no effect, read as zero.	R
25	BLAST	BCH/NAND last. 0: non-last data block for BCH/NAND; 1: last data block for BCH/NAND. (Only channel 0 support BCH transfer; all channel support Nand transfer, when it is used for nand, it means the last data block transfer for one nand dma request detection)	RW
24	Reserved	Write has no effect, read as zero.	R
23	SAI	Source Address Increment. 0: no increment; 1: increment.	RW
22	DAI	Target Address Increment. 0: no increment; 1: increment.	RW
19:16	Reserved	Write has no effect, read as zero.	R
15:14	SP	Source port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
13:12	DP	Target port width.	RW

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		00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved. (**NOTE:** for bch transfer encoding, DP only can be 32-bit or 8-bit; for bch decoding, DP only can be 32-bit)	
11	Reserved	Write has no effect, read as zero.	R
10:8	TSZ	Transfer Data Size of a data unit. 000: 32-bit; 001: 8-bit; 010: 16-bit; 011: 16-byte; 100: 32-byte; 101: 64-byte; others: reserved.	RW
7	NRD	Direct read nand. 0: non-direct read nand; 1: enable direct read nand. (Only channel 1 has this field for Nand transfer)	RW
6	NWR	Direct write nand. 0: non-direct write nand; 1: enable direct write nand. (Only channel 1 has this field for Nand transfer)	RW
5	NAC	Nand AL/CL from Data. 0: AL/CL from data is disabled; 1: enable AL/CL from data. (If AL/CL from data is disabled, AL/CL is from address[23:22] written to nand; When AL/CL from data is enabled, bit 31 of the data indicates AL, bit 30 of the data indicates CL; When AL/CL from data is enabled, be sure to set SP to 32-bit, set DP according to SMCR.BW in memory controller) (Only channel 1 has this field for Nand transfer)	RW
4:3	Reserved	**NOTE:** Don't write 1 to these bits, reserved them to 0.	RW
2	STDE	Stride Disable/Enable. 0: address stride disable; 1: address stride enable.	RW
1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (Ignored in No-Descriptor Transfer)	RW

8.2.7 DMA Descriptor Address (DDAn, n = 0 ~ 2)

This register is ignored in No-Descriptor Transfer.

DDA0, DDA1, DDA2 **0x13450018, 0x13450038, 0x13450058**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address.	RW

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11:4	DOA	Descriptor Offset Address. When 4-descriptor is used, DOA is used for the offset address of DDA for next descriptor fetch.	RW
3:0	Reserved	Write has no effect, read as zero.	R

NOTE: When 8-descriptor is used, next descriptor fetch address is from 8th word of last descriptor, that is the 0th~27th bit of the 8th word of last descriptor is mapped to DDA[31:4] for next descriptor fetch.

8.2.8 DMA Stride Address (DSDn, n = 0 ~ 2)

This register is ignored in No-Descriptor Transfer.

When address stride transfer is enabled in Descriptor mode, after a sub-block defined in DTCRn is finished transferring, the source or target stride address will be added up to the corresponding source or target address and the transfer will keep going until the transfer ends which means TC in DTCRn reach 0.

DSD0, DSD1, DSD2 **0x1345001C, 0x1345003C, 0x1345005C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD																SSD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	TSD	Target Stride Address.	RW
15:0	SSD	Source Stride Address.	RW

8.2.9 DMA Nand Timer (DNTn, n = 0 ~ 2)

This register is used for nand low pulse detect and for AL and CL from data.

DNT0, DNT1, DNT2 **0x134500C0, 0x134500C4, 0x134500C8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										DTCT						DNTE	Reserved											DNT			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
31:23	Reserved	Write has no effect, read as zero.	R
22:16	DTCT	Tail Counter. When Nand AL/CL from data is enabled, the counter indicates the	RW

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		actual word written to nand in the last transfer. It is used for transfer count when nand AL/CL from data is enabled. During the last transfer (DTCR == 1), if DCMR.TSZ is set for 16-byte, 32-byte or 64-byte, when DTCT is not equal to 0, the value in DTCT indicates the actual word number written to nand in the last transfer.	
15	DNTE	Nand Detect Timer enable. 0: Nand detect timer disable; 1: Nand detect timer enable.	RW
14:6	Reserved	Write has no effect, read as zero.	R
5:0	DNT	Nand Detect Timer. When Nand detect timer is enabled, the timer starts running down, when the timer is down to zero, it generates a request to DMA for data transfer.	RW

8.2.10 DMA Control

DMAC1 controls channel 0~2.

DMAC1 **0x13450300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						PM		Reserved				HLT	AR	Reserved	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Write has no effect, read as zero.	R
9:8	PM	Channel priority mode. 00: CH0, CH1 > CH2 01: CH1, CH2 > CH0 10: CH2 > CH0, CH1 11: CH0, CH1, CH2 For example, when PM == 2'b00, it means set1 includes ch0 and ch1 and set2 includes ch2, set 1 has the higher priority than set 2, within one set, channel priority is round robin, that is: ch0→ch1→ch2.	RW
7:4	Reserve	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should set to 1. 0: no halt; 1: halt occurred.	RW
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1.	RW

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		0: no address error; 1: address error occurred.	
1	Reserved	Write has no effect, read as zero.	R
0	DMAE	Global DMA transfer enable. 0: disable DMA channel transfer; 1: enable DMA channel transfer.	RW

8.2.11 DMA Interrupt Pending (DIRQP)

DMAC supports total 3 pending interrupt which are in DIRQP.

DIRQP **0x13450304**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CIRQ2	CIRQ1	CIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	CIRQn	CIRQn (n=0~2) denotes pending status for corresponding channel. 0: no abnormal situation or normal DMA transfer is in progress 1: abnormal situation occurred or normal DMA transfer done	RW

8.2.12 DMA Doorbell (DDR)

DDR supports channel 0~2.

DDR **0x13450308**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DB2	DB1	DB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DBn	DMA Doorbell for each channel, n=0~2, for example DB0 is for DMA channel 0. Software set it to 1 and hardware clears it to 0. 0: disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1: Write 1 to DDS will set the corresponding DBn bit to 1 and enable DMA controller to fetch the first descriptor	R

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		For example, write 0x00000001 to DDS, DB0 bit is set to 1 and enable DMA channel 0 to fetch the first descriptor. Write 0 to DDS, no meaning.	

8.2.13 DMA Doorbell Set (DDRS)

DDRS supports channel 0~2.

DDRS **0x1345030c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DBS2	DBS1	DBS0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DBSn	DMA Doorbell Set for each channel. 0: ignore; 1: Set the corresponding DBn bit to 1.	W

8.2.14 DMA Clock Enable (DCKE)

DCKE supports channel 0~2.

DCKE **0x13450310**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DCKE2	DCKE1	DCKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DCKEn	DMA Clock Enable for each channel. 0: ignore; 1: Set the corresponding DCKEn bit to 1.	RW

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8.2.15 DMA Clock Enable Set (DCKES)

DCKES supports channel 0~2.

DCKES **0x13450314**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DCKES2	DCKES1	DCKES0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DCKESn	DMA Clock Enable Set for each channel. 0: ignore; 1: Set the corresponding DCKESn bit to 1 to enable corresponding channel clock	W

8.2.16 DMA Clock Clear Set (DCKEC)

DCKEC supports channel 0~2.

DCKEC **0x13450318**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DCKEC2	DCKEC1	DCKEC0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DCKECn	DMA Clock Enable Clear for each channel. 0: ignore 1: Set the corresponding DCKECn bit to 1 to disable corresponding channel clock	W

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8.3 DMA manipulation

8.3.1 Descriptor Transfer

8.3.1.1 Normal Transfer

To do proper Descriptor DMA transfer, do as following steps:

1 First of all, open channel clock by setting DCKEn register for corresponding channel.
2 Check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0 and DTCn=0.
3 Select 4 word or 8 word descriptor by DCSn.DES8.
4 For Descriptor transfer, guarantee DCSn.NDES=0.
5 Initiate channel request register DRSRn.
6 Build descriptor in memory. Write the first descriptor address in DDAn and the address must be 16Bytes aligned in 4word descriptor and 32Bytes aligned in 8word descriptor. The descriptor address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DES3.DOA and the four LSB is 0x0. See Table 8-3 for the detailed 4-word descriptor structure.

   NOTE: if stride address transfer is enabled, the address must be 32Bytes aligned because DES4 needs to read out.

7 Set 1 to the corresponding bit in DDR to initiate descriptor fetch.
8 Set DMAC.DMAE=1 and expected DCSn.CTE=1 to launch DAM transfer.
9 Hardware clears the corresponding bit in DDR as soon as it starts to fetch the descriptor.
10 Waits for dma request from peripherals to start dma transfer.
11 After DMAC completes the current descriptor dma transfer, if DES0.Link=0, it sets DCSn.TT to 1. If the interrupt enabled, it will generates the corresponding interrupts.
12 If DES0.LINK=1, after DMAC completes the current descriptor dma transfer and return to fetch the next descriptor and continues dma transfer until completes the descriptor dma transfer which DES0.LINK=0.
13 When transfer end, clr DCSn.CTE to 0 to close the channel, and then clear DCSn.TT bits.

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Table 8-3 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	EACKS	External DMA DACKn output polarity select
	30	EACKM	External DMA DACKn output Mode select
	29-28	ERDM	External DMA request detection Mode
	27	EOPM	External DMA End of process mode
	26	Reserved	
	25	BLAST	BCH Last (Only for BCH and Nand transfer)
	24	Reserved	
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	
	10-8	TSZ	Transfer Data Size
	7	NRD	Direct read nand
	6	NWR	Direct write nand
	5	NAC	Nand AL/CL from data
	4:3	Reserved	
	2	STDE	Stride transfer enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable
2nd (DES1)	31-0	DSA	Source Address
3rd (DES2)	31-0	DTA	Target Address
4th (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter
5th (DES4)	31-16	TSD	Target Stride Address
	15-0	SSD	Source Stride Address
6th(DES5)	31-16	Reserved	
	15:6	Reserved	
	5-0	DRT	DMA Request Type
7th(DES6)	31-23	DNTE1	Nand request 1 timer enable
	30:23	DNT1	Nand request 1 detect timer
	22-16	DTCT	Nand tail counter
	15	DNTE	Nand request 0 detect timer enable
	14-6	Reserved	
	5-0	DNT	Nand request 0 detect timer
8th(DES7)	31-4	DDA	Next descriptor address
	3-0	Reserved	

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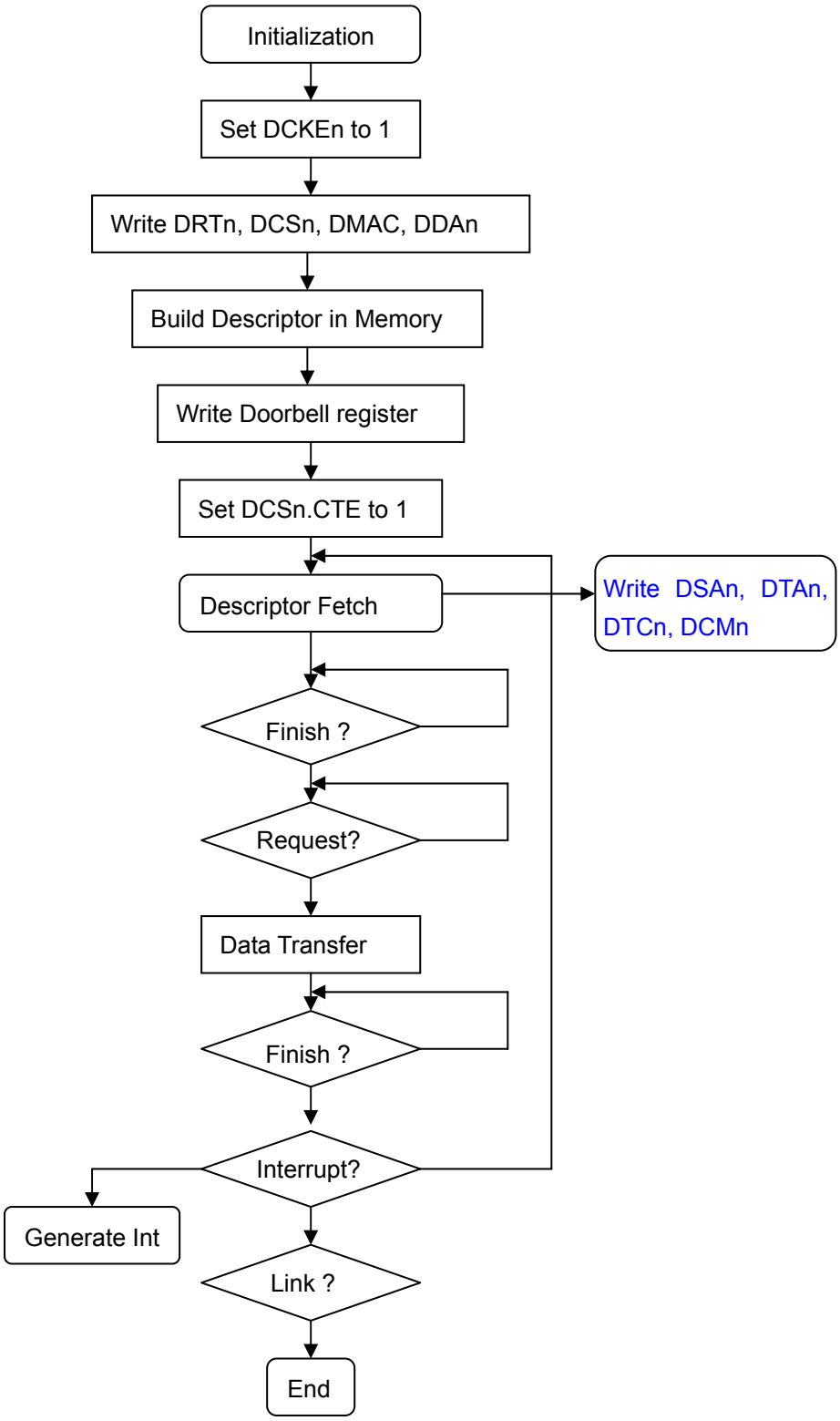


Figure 8-1 Descriptor Transfer Flow

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8.3.1.2 Stride Address Transfer

During transfer, source or target address can be not continuous and the source and target stride offset address are showed in DSDn registers.

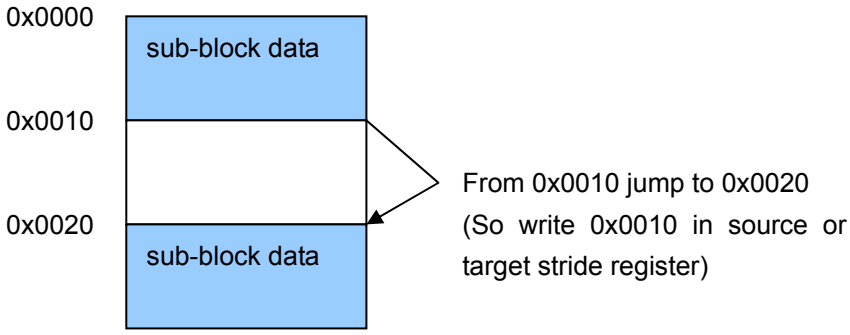


Figure 8-2 Example for Stride Address Transfer

8.3.1.3 BCH DMA Transfer

Channel 0 supports BCH DMA transfer.

During BCH encoding, DMA read data from memory pointed by DSAR0 and write to BCH data register BHDR, after BCH encoding finishes, DMA write BHINT and BCH parity data BHPAR0~9 respectively to memory pointed by DTAR0, and then DMA clear BHINT and set BCH reset to BCH automatically.

During BCH decoding, DMA read data from memory pointed by DSAR0 and write to BCH data register BHDR, after BCH decoding finishes, if there is error in the data block, DMA will write BHINT, BHERR0~11 to memory pointed by DTAR0 or if there is no error in the data block, DMA will only write BHINT to memory, and then DMA clear BHINT and set BCH reset to BCH. If multiple data block are linked to wait for BCH decoding, data transfer and decoding can be executed in pipeline, that is when the first data block is being decoding, and second data can be transfer to BCH for syndrome generation.

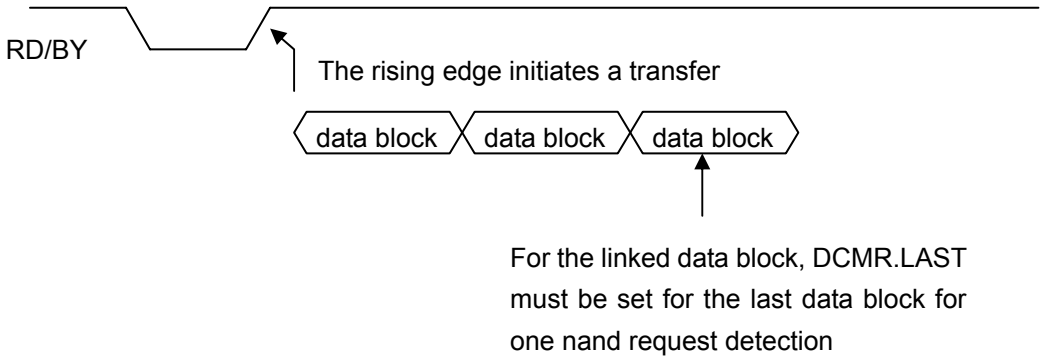
Here one data block means, for encoding, the entire data bytes need encoding, for decoding, the entire data bytes and parity bytes need decoding. DCM.BLAST must be used in descriptor BCH transfer. When one data block is in a continuous memory space, BLAST must be set to 1 for this data block; when one data block is linked in multiple data space, BLAST must be set to 1 for the last data space.

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8.3.1.4 Nand Transfer

Two ways are for nand RB detect.

One way is to detect RD/BY rising edge as the following waveform.



The other way is using DNT register. When the rising edge is missed by DMA, DNT timer also can be used for nand RB detect. The timer is used to detect the high level duration of RD/BY signal, when the high level keep high longer than DNT counting periods, then nand transfer request generates.

DCMR1.DNT and DCMR1.DNTE are for nand request 0. DCMR1.DNT1 and DCMR1.DNTE1 are for nand request 1.

8.3.2 No-Descriptor Transfer

To do proper DMA transfer, do as following steps:

2 First of all, check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0 and DCSn.TT=0 and DTCn=0.

3 For each channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly.

4 Set DMAC.DMAE=1 and expected DCSn.CTE=1 and DCSn.NDES=1 to launch DAM transfer.

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile corresponding bit of DIRQP is set to 1. If DCMn.TIE bit is set to 1, an interrupt request is sent to the CPU. However, during the transfer, if a DMA address error occurs, the transfer is suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP. Then an interrupt request is sent to the CPU despite of DCMn.TIE.

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Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

For non-descriptor BCH transfer, there is no pipeline execution for BCH decoding. DCM.BLAST doesn't need to be set in non-descriptor BCH transfer.

8.4 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

8.4.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

8.4.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals. All request types except 0x8 (value of DRT) belong to the mode. **NOTE:** the transfer byte number for one request detection according to DCMn.RDIL must be equal or less than the byte number according to receive or transmit trigger value of source or target devices.

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8.5 Channel Priorities

There are two dma cores, each one supports 6 channels dma transfer. The two cores have the same priority.

In each core, there are two sets: set 1 has the higher priority than set 2, within each set priority is round robin.

Table 8-4 Relationship among DMA transfer connection, request mode & transfer mode

Transfer Connection	Request Mode	Transfer Mode	Data Size (bits)	Channel
External memory or memory-mapped external device and on-chip peripheral module	Auto on-chip	Single	8/16/32 16-byte/32-byte	0~5

8.6 Examples

8.6.1 Memory-to-memory auto request No-Descriptor Transfer

Suppose you want to do memory move between two different memory regions through channel 3, for example, moving 1KB data from address 0x20001000 to 0x20011000, do as following steps:

1 Check if (DMAC.AR==0 && DMAC.HLT==0 && DCS3.AR==0 && DCS3.HLT==0 && DCS3.CT==0 && DCS3.NDES=1 && DTC3==0).
2 If above condition is true, set value 0 to DCS3.CTE to disable the channel 3 temporarily.
3 Set source address 0x20001000 to DSA3 and target address 0x20011000 to DTA3.
4 Suppose the data unit is word, set transfer count number 256 (1024/4) to DTC3.
5 Set auto-request (0x8) to DRT3.
6 Up to now, only the most important channel control register DCM3 is left, set it carefully:
   – Set value 1 to SAI and DAI[*1].
   – Ignore RDIL because in the case there is no explicit request signal can be detected.
   – Set word size (0) to SP and DP[*2].
   – Set value 1 to TIE to let CPU do some post process after the transfer done.
7 Set value 1 to DCS3.CTE and DMAC.DMAE to launch the transfer in channels 3.
8 When the transfer terminates normally (DTC3==0 && DCS3.TT==1), DIRQP.CIRQ3 will automatically be set value 1 and an interrupt request will be sent to CPU.
9 When CPU grants the interrupt request, in the corresponding IRQ handler, software must clear the DCS3.CT to value 0, and the behavior will automatically clear DIRQP.CIRQ3.

NOTES:

1 Either source or target is a FIFO, must not enable corresponding address increment.
2 When either source or target need be accessed through EMC (external memory controller), the real port with of the device is encapsulated by EMC, so you can set any favorite port with for it despite of the real one.

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9 DMA Controller

DMA controller (DMAC) is dedicated to transfer data between on-chip peripherals (MSC, AIC, UART, etc.), external memories, and memory-mapped external devices.

9.1 Features

- Support up to 12 independent DMA channels
- Two independent DMA core, each supports 6 channels
- Descriptor or No-Descriptor Transfer
- Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte, 32-byte or 64-byte
- Transfer number of data unit: 1 ~ 224
- Independent source and target port width: 8-bit, 16-bit, 32-bit
- Two channel priority modes: fixed, round robin

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9.2 Register Descriptions

Table 9-1 DMAC Registers

Name	Description	RW	Reset Value	Address	Access Size (bit)
DSA0	DMA Source Address 0	RW	0x0	0x13420000	32
DTA0	DMA Target Address 0	RW	0x0	0x13420004	32
DTC0	DMA Transfer Count 0	RW	0x0	0x13420008	32
DRT0	DMA Request Source 0	RW	0x0	0x1342000C	32
DCS0	DMA Channel Control/Status 0	RW	0x0	0x13420010	32
DCM0	DMA Command 0	RW	0x0	0x13420014	32
DDA0	DMA Descriptor Address 0	RW	0x0	0x13420018	32
DSD0	DMA Stride Address 0	RW	0x0	0x1342001C	32
DSA1	DMA Source Address 1	RW	0x0	0x13420020	32
DTA1	DMA Target Address 1	RW	0x0	0x13420024	32
DTC1	DMA Transfer Count 1	RW	0x0	0x13420028	32
DRT1	DMA Request Source 1	RW	0x0	0x1342002C	32
DCS1	DMA Channel Control/Status 1	RW	0x0	0x13420030	32
DCM1	DMA Command 1	RW	0x0	0x13420034	32
DDA1	DMA Descriptor Address 1	RW	0x0	0x13420038	32
DSD1	DMA Stride Address 1	RW	0x0	0x1342003C	32
DSA2	DMA Source Address 2	RW	0x0	0x13420040	32
DTA2	DMA Target Address 2	RW	0x0	0x13420044	32
DTC2	DMA Transfer Count 2	RW	0x0	0x13420048	32
DRT2	DMA Request Source 2	RW	0x0	0x1342004C	32
DCS2	DMA Channel Control/Status 2	RW	0x0	0x13420050	32
DCM2	DMA Command 2	RW	0x0	0x13420054	32
DDA2	DMA Descriptor Address 2	RW	0x0	0x13420058	32
DSD2	DMA Stride Address 2	RW	0x0	0x1342005C	32
DSA3	DMA Source Address 3	RW	0x0	0x13420060	32
DTA3	DMA Target Address 3	RW	0x0	0x13420064	32
DTC3	DMA Transfer Count 3	RW	0x0	0x13420068	32
DRT3	DMA Request Source 3	RW	0x0	0x1342006C	32
DCS3	DMA Channel Control/Status 3	RW	0x0	0x13420070	32
DCM3	DMA Command 3	RW	0x0	0x13420074	32
DDA3	DMA Descriptor Address 3	RW	0x0	0x13420078	32
DSD3	DMA Stride Address 3	RW	0x0	0x1342007C	32
DSA4	DMA Source Address 4	RW	0x0	0x13420080	32
DTA4	DMA Target Address 4	RW	0x0	0x13420084	32
DTC4	DMA Transfer Count 4	RW	0x0	0x13420088	32
DRT4	DMA Request Source 4	RW	0x0	0x1342008C	32

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DCS4	DMA Channel Control/Status 4	RW	0x0	0x13420090	32
DCM4	DMA Command 4	RW	0x0	0x13420094	32
DDA4	DMA Descriptor Address 4	RW	0x0	0x13420098	32
DSD4	DMA Stride Address 4	RW	0x0	0x1342009C	32
DSA5	DMA Source Address 5	RW	0x0	0x134200A0	32
DTA5	DMA Target Address 5	RW	0x0	0x134200A4	32
DTC5	DMA Transfer Count 5	RW	0x0	0x134200A8	32
DRT5	DMA Request Source 5	RW	0x0	0x134200AC	32
DCS5	DMA Channel Control/Status 5	RW	0x0	0x134200B0	32
DCM5	DMA Command 5	RW	0x0	0x134200B4	32
DDA5	DMA Descriptor Address 5	RW	0x0	0x134200B8	32
DSD5	DMA Stride Address 5	RW	0x0	0x134200BC	32
DSA6	DMA Source Address 6	RW	0x0	0x13420100	32
DDA6	DMA Target Address 6	RW	0x0	0x13420104	32
DTC6	DMA Transfer Count 6	RW	0x0	0x13420108	32
DRT6	DMA Request Source 6	RW	0x0	0x1342010C	32
DCS6	DMA Channel Control/Status 6	R/W	0x0	0x13420110	32
DCM6	DMA Command 6	RW	0x0	0x13420114	32
DDA6	DMA Descriptor Address 6	RW	0x0	0x13420118	32
DSD6	DMA Stride Address 6	RW	0x0	0x1342011C	32
DSA7	DMA Source Address 7	RW	0x0	0x13420120	32
DDA7	DMA Target Address 7	RW	0x0	0x13420124	32
DTC7	DMA Transfer Count 7	RW	0x0	0x13420128	32
DRT7	DMA Request Source 7	RW	0x0	0x1342012C	32
DCS7	DMA Channel Control/Status 7	R/W	0x0	0x13420130	32
DCM7	DMA Command 7	RW	0x0	0x13420134	32
DDA7	DMA Descriptor Address 7	RW	0x0	0x13420138	32
DSD7	DMA Stride Address 7	RW	0x0	0x1342013C	32
DSA8	DMA Source Address 8	RW	0x0	0x13420140	32
DDA8	DMA Target Address 8	RW	0x0	0x13420144	32
DTC8	DMA Transfer Count 8	RW	0x0	0x13420148	32
DRT8	DMA Request Source 8	RW	0x0	0x1342014C	32
DCS8	DMA Channel Control/Status 8	R/W	0x0	0x13420150	32
DCM8	DMA Command 8	RW	0x0	0x13420154	32
DDA8	DMA Descriptor Address 8	RW	0x0	0x13420158	32
DSD8	DMA Stride Address 8	RW	0x0	0x1342015C	32
DSA9	DMA Source Address 9	RW	0x0	0x13420160	32
DDA9	DMA Target Address 9	RW	0x0	0x13420164	32
DTC9	DMA Transfer Count 9	RW	0x0	0x13420168	32
DRT9	DMA Request Source 9	RW	0x0	0x1342016C	32
DCS9	DMA Channel Control/Status 9	R/W	0x0	0x13420170	32

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DCM9	DMA Command 9	RW	0x0	0x13420174	32
DDA9	DMA Descriptor Address 9	RW	0x0	0x13420178	32
DSD9	DMA Stride Address 9	RW	0x0	0x1342017C	32
DSA10	DMA Source Address 10	RW	0x0	0x13420180	32
DDA10	DMA Target Address 10	RW	0x0	0x13420184	32
DTC10	DMA Transfer Count 10	RW	0x0	0x13420188	32
DRT10	DMA Request Source 10	RW	0x0	0x1342018C	32
DCS10	DMA Channel Control/Status 10	R/W	0x0	0x13420190	32
DCM10	DMA Command 10	RW	0x0	0x13420194	32
DDA10	DMA Descriptor Address 10	RW	0x0	0x13420198	32
DSD10	DMA Stride Address 10	RW	0x0	0x1342019C	32
DSA11	DMA Source Address 11	RW	0x0	0x134201A0	32
DDA11	DMA Target Address 11	RW	0x0	0x134201A4	32
DTC11	DMA Transfer Count 11	RW	0x0	0x134201A8	32
DRT11	DMA Request Source 11	RW	0x0	0x134201AC	32
DCS11	DMA Channel Control/Status 11	R/W	0x0	0x134201B0	32
DCM11	DMA Command 11	RW	0x0	0x134201B4	32
DDA11	DMA Descriptor Address 11	RW	0x0	0x134201B8	32
DSD11	DMA Stride Address 11	RW	0x0	0x134201BC	32
DMAC1	DMA Control 1 Register	R/W	0x0	0x13420300	32
DIRQP1	DMA Interrupt Pending 1	R	0x0	0x13420304	32
DDR1	DMA Doorbell 1 Register	RW	0x0	0x13420308	32
DDRS1	DMA Doorbell Set 1 Register	W	0x0	0x1342030C	32
DCKE1	DMA Clock Enable 1 Register	W	0x0	0x13420310	32
DCKES1	DMA Clock Enable 1 Set Register	W	0x0	0x13420314	32
DCKEC1	DMA Clock Enable 1 Clear Register	W	0x0	0x13420318	32
DMAC2	DMA Control 2 Register	R/W	0x0	0x13420400	32
DIRQP2	DMA Interrupt Pending 2	R	0x0	0x13420404	32
DDR2	DMA Doorbell 2 Register	RW	0x0	0x13420408	32
DDRS2	DMA Doorbell Set Register	W	0x0	0x1342040C	32
DCKE2	DMA Clock Enable 2 Register	W	0x0	0x13420410	32
DCKES2	DMA Clock Enable 2 Set Register	W	0x0	0x13420414	32
DCKEC2	DMA Clock Enable 2 Clear Register	W	0x0	0x13420418	32

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9.2.1 DMA Source Address (DSAn, n = 0 ~ 11)

DSA0, DSA1, DSA2, **0x13420000, 0x13420020, 0x13420040,**
DSA3, DSA4, DSA5, **0x13420060, 0x13420080, 0x134200A0,**
DSA6, DSA7, DSA8, **0x13420100, 0x13420120, 0x13420140,**
DSA9, DSA10, DSA11 **0x13420160, 0x13420180, 0x134201A0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	Source physical address.	RW

9.2.2 DMA Target Address (DTAn, n = 0 ~ 11)

DTA0, DTA1, DTA2, **0x13420004, 0x13420024, 0x13420044,**
DTA3, DTA4, DTA5, **0x13420064, 0x13420084, 0x134200A4,**
DTA6, DTA7, DTA8, **0x13420104, 0x13420124, 0x13420144,**
DTA9, DTA10, DTA11 **0x13420164, 0x13420184,0x134201A4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TA	Target physical address.	RW

9.2.3 DMA Transfer Count (DTCn, n = 0 ~ 11)

DTC0, DTC1, DTC2, **0x13420008, 0x13420028, 0x13420048,**
DTC3, DTC4, DTC5, **0x13420068, 0x13420088, 0x134200A0,**
DTC6, DTC7, DTC8, **0x13420108, 0x13420128, 0x13420148,**
DTC9, DTC10, DTC11 **0x13420168, 0x13420188, 0x134201A8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	When Stride address transfer is disabled: TC hold the number of data unit to transfer and it counts down to 0 at the end. When Stride address transfer is enabled: TC composes of two parts: The lower 16 bits: the number of data unit for sub-block transfer The higher 8 bits: the number of sub-block And both the two parts count down to 0 at the end.	RW

9.2.4 DMA Request Types (DRTn, n = 0 ~ 11)

DRT0, DRT1, DRT2, **0x1342000c, 0x1342002c, 0x1342004c,**
DRT3, DRT4, DRT5, **0x1342006c, 0x1342008c, 0x134200Ac,**
DRT6, DRT7, DRT8, **0x1342010c, 0x1342012c, 0x1342014c,**
DRT9, DRT10, DRT11 **0x1342016c, 0x1342018c, 0x134201Ac**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RT					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	RT	Transfer request type.	RW

Table 9-2 Transfer Request Types

RT5-0	Description
000000	Reserved.
000001	Reserved.
000010	Reserved.
000011	Reserved.
000100	Reserved.
000101	Reserved.
000110	Reserved.
000111	Reserved.
001000	Auto-request. (ignore RDIL3-0, external address → external address)
001001	TSSI receive-fifo-full transfer request. (TS fifo → external address)
001010	Reserved.
001011	Reserved.

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001100	External request with DREQn. (external address ←→ external device with DACKn)
001101	Reserved.
001110	UART3 transmit-fifo-empty transfer request. (external address → UTHR)
001111	UART3 receive-fifo-full transfer request. (URBR → external address)
010000	UART2 transmit-fifo-empty transfer request. (external address → UTHR)
010001	UART2 receive-fifo-full transfer request. (URBR → external address)
010010	UART1 transmit-fifo-empty transfer request. (external address → UTHR)
010011	UART1 receive-fifo-full transfer request. (URBR → external address)
010100	UART0 transmit-fifo-empty transfer request. (external address → UTHR)
010101	UART0 receive-fifo-full transfer request. (URBR → external address)
010110	SSI transmit-fifo-empty transfer request.
010111	SSI receive-fifo-full transfer request.
011000	AIC transmit-fifo-empty transfer request.
011001	AIC receive-fifo-full transfer request.
011010	MSC transmit-fifo-empty transfer request.
011011	MSC receive-fifo-full transfer request.
011100	TCU channel n. (overflow interrupt, external address→external address space)
011101	SADC transfer request. (SADC → external address)
011110	MSC1 transmit-fifo-empty transfer request.
011111	MSC1 receive-fifo-full transfer request.
100000	SSI1 transmit-fifo-empty transfer request.
100001	SSI1 receive-fifo-full transfer request.
100010	PM transmit-fifo-empty transfer request.
100011	PM receive-fifo-full transfer request.
100100	MSC2 transmit-fifo-empty transfer request.
100101	MSC2 receive-fifo-full transfer request.
101000	I2C transmit-fifo-empty transfer request.
101001	I2C receive-fifo-full transfer request.
101010	I2C1 transmit-fifo-empty transfer request.
101011	I2C1 receive-fifo-full transfer request.
101100	Reserved.
101101	Reserved.
101110	I2C1 transmit-fifo-empty transfer request.
101111	I2C1 receive-fifo-full transfer request.
Other	Reserved.

NOTES:

1 Only auto request can be concurrently selected in all channels with different source and target address.

2 For on-chip device DMA request except TCU, the corresponding source or target address that map to on-chip device must be set as fixed.

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9.2.5 DMA Channel Control/Status (DCSn, n = 0 ~ 11)

DCS0, DCS1, DCS2, **0x13420010, 0x13420030, 0x13420050,**
DCS3, DCS4, DCS5, **0x13420070, 0x13420090, 0x134200B0**
DCS6, DCS7, DCS8, **0x13420110, 0x13420130, 0x13420150,**
DCS9, DCS10, DCS11 **0x13420170, 0x13420190, 0x134201B0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	DES8	Reserved						CDOA								Reserved											AR	TT	HLT	Reserved	CTE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30	DES8	Descriptor 8 Word. 0: 4-word descriptor; 1: 8-word descriptor.	RW
29:24	Reserved	Write has no effect, read as zero.	R
23:16	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. Software could know which descriptor is just completed combining with count terminate interrupt resulted by DCSn.CT. (Ignored in No-Descriptor Transfer)	RW
15:5	Reserved	Write has no effect, read as zero.	R
4	AR	Address Error. 0: no address error; 1: address error.	RW
3	TT	Transfer Terminate. 0: No-Link Descriptor or No-Descriptor DMA transfer does not end 1: No-Link Descriptor or No-Descriptor DMA transfer end	RW
2	HLT	DMA halt. 0: DMA transfer is in progress; 1: DMA halt.	RW
1	Reserved	Write has no effect, read as zero.	R
0	CTE	Channel transfer enable. 0: disable; 1: enable.	RW

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9.2.6 DMA Channel Command (DCMn, n = 0 ~ 11)

DCM0, DCM1, DCM2, **0x13420014, 0x13420034, 0x13420054,**
DCM3, DCM4, DCM5, **0x13420074, 0x13420094, 0x134200B4,**
DCM6, DCM7, DCM8, **0x13420114, 0x13420134, 0x13420154,**
DCM9. DCM10, DCM11 **0x13420174, 0x13420194, 0x134201B4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EACKS	EACKM	ERDM		Reserved				SAI	DAI	Reserved		RDIL				SP		DP		Reserved		TSZ		Reserved					STDE	TIE	LINK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	EACKS	External DACK Output Level Select. 0: active high; 1: active low.	RW
30	EACKM	External DACK Output Mode Select. 0: output in read cycle; 1: output in write cycle.	RW
29:28	ERDM	External DREQ Detection Mode Select. 00: Low level detection 01: Falling edge detection 10: High level detection 11: Rising edge detection	RW
27:24	Reserved	Write has no effect, read as zero.	R
23	SAI	Source Address Increment. 0: no increment; 1: increment.	RW
22	DAI	Target Address Increment. 0: no increment; 1: increment.	RW
19:16	RDIL	Request Detection Interval Length. Set the number of transfer unit between two requests detection in single mode. Please refer to following Table 9-3.	RW
15:14	SP	Source port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
13:12	DP	Target port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
11	Reserved	Write has no effect, read as zero.	R
10:8	TSZ	Transfer Data Size of a data unit. 000: 32-bit; 001: 8-bit; 010: 16-bit; 011: 16-byte; 100: 32-byte; 101: 64-byte; others: reserved.	RW
7:3	Reserved	Write has no effect, read as zero.	R
2	STDE	Stride Disable/Enable. 0: address stride disable; 1: address stride enable.	RW
1	TIE	Transfer Interrupt Enable (TIE).	RW

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		0: disable interrupt; 1: enable interrupt when TT is set to 1.	
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (Ignored in No-Descriptor Transfer)	RW

Table 9-3 Detection Interval Length

RDIL	Description
0	Interval length is 0.
1	Interval length is 2 transfer unit.
2	Interval length is 4 transfer unit.
3	Interval length is 8 transfer unit.
4	Interval length is 12 transfer unit.
5	Interval length is 16 transfer unit.
6	Interval length is 20 transfer unit.
7	Interval length is 24 transfer unit.
8	Interval length is 28 transfer unit.
9	Interval length is 32 transfer unit.
10	Interval length is 48 transfer unit.
11	Interval length is 60 transfer unit.
12	Interval length is 64 transfer unit.
13	Interval length is 124 transfer unit.
14	Interval length is 128 transfer unit.
15	Interval length is 200 transfer unit.

9.2.7 DMA Descriptor Address (DDAn, n = 0 ~ 11)

This register is ignored in No-Descriptor Transfer.

DDA0, DDA1, DDA2, DDA3, DDA4, DDA5, DDA6, DDA7, DDA8, DDA9, DDA10, DDA11

0x13420018, 0x13420038, 0x13420058, 0x13420078, 0x13420098, 0x134200B8, 0x13420118, 0x13420138, 0x13420158, 0x13420178, 0x13420198, 0x134201B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address.	RW
11:4	DOA	Descriptor Offset Address.	RW
3:0	Reserved	Write has no effect, read as zero.	R

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9.2.8 DMA Stride Address (DSDn, n = 0 ~ 11)

This register is ignored in No-Descriptor Transfer.

When address stride transfer is enabled in Descriptor mode, after a sub-block defined in DTCRn is finished transferring, the source or target stride address will be added up to the corresponding source or target address and the transfer will keep going until the transfer ends which means TC in DTCRn reach 0.

DSD0, DSD1, DSD2, **0x1342001C, 0x1342003C, 0x1342005C,**
DSD3, DSD4, DSD5, **0x1342007C, 0x1342009C, 0x134200BC**
DSD6, DSD7, DSD8, **0x1342011C, 0x1342013C, 0x1342015C,**
DSD9, DSD10, DSD11 **0x1342017C, 0x1342019C, 0x134201BC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD																SSD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	TSD	Target Stride Address.	RW
15:0	SSD	Source Stride Address.	RW

9.2.9 DMA Control

DMAC1 controls channel 0~5 and DMAC2 controls channel 6~11.

DMAC1 **0x13420300**
DMAC2 **0x13420400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FMSC	FSSI	FTSSI	FUART	FAIC	Reserved																	PM	Reserved					HLT	AR	Reserved	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	FMSC	MSC Fast DMA mode. 0: normal DMA transfer; 1: fast DMA transfer.	RW
30	FSSI	SSI Fast DMA mode. 0: normal DMA transfer; 1: fast DMA transfer.	RW
29	FTSSI	TSSI Fast DMA mode. 0: normal DMA transfer; 1: fast DMA transfer.	RW
28	FUART	UART Fast DMA mode. 0: normal DMA transfer; 1: fast DMA transfer.	RW

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27	FAIC	AIC Fast DMA mode. 0: normal DMA transfer; 1: fast DMA transfer.	RW
26:10	Reserved	Write has no effect, read as zero.	R
9:8	PM	Channel priority mode. 00: CH0, CH1 > CH2, CH3, CH4 01: CH1, CH2 > CH0, CH3, CH4 10: CH2, CH3 > CH0, CH1, CH4 11: CH3, CH4 > CH0, CH1, CH2 For example, when PM == 2'b00, it means set1 includes ch0 and ch1 and set2 includes ch2~ch4, set 1 has the higher priority than set 2, within one set, channel priority is round robin, that is: ch0→ch1→ch2→ch0→ch1→ch3→ch0→ch1→ch4→ch0→ch1	RW
7:4	Reserve	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should set to 1. 0: no halt 1: halt occurred	RW
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1. 0: no address error 1: address error occurred	RW
1	Reserved	Write has no effect, read as zero.	R
0	DMAE	Global DMA transfer enable. 0: disable DMA channel transfer 1: enable DMA channel transfer	RW

NOTE: FMSC/FSSI/FTSSI/FUART/FAIC bit either in DMAC1 or in DMAC2 is set, the corresponding dma transfer for MSC(MSC1, MSC2), SSI(SSI1), UART0~3, AIC is in fast dma mode.

9.2.10 DMA Interrupt Pending (DIRQP)

DMAC supports total 12 pending interrupt, 6 of them are in DIRQP and the other 6 are in DIRQP2.

DIRQP **0x13420304**

DIRQP2 **0x13420404**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CIRQ5	CIRQ4	CIRQ3	CIRQ2	CIRQ1	CIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	CIRQn	CIRQn (n=0~5) denotes pending status for corresponding channel.	RW

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		0:no abnormal situation or normal DMA transfer is in progress 1: abnormal situation occurred or normal DMA transfer done	

9.2.11 DMA Doorbell (DDR)

DDR supports channel 0~5 and DDR2 supports channel 6~11.

DDR **0x13420308**

DDR2 **0x13420408**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DB5	DB4	DB3	DB2	DB1	DB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	DBn	DMA Doorbell for each channel, n=0~5, for example DB0 is for DMA channel 0. Software set it to 1 and hardware clears it to 0. 0: disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1: Write 1 to DDS will set the corresponding DBn bit to 1 and enable DMA controller to fetch the first descriptor For example, write 0x00000001 to DDS, DB0 bit is set to 1 and enable DMA channel 0 to fetch the first descriptor. Write 0 to DDS, no meaning.	R

9.2.12 DMA Doorbell Set (DDRS)

DDRS supports channel 0~5 and DDRS2 supports channel 6~11.

DDRS **0x1342030c**

DDRS2 **0x1342040c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DBS5	DBS4	DBS3	DBS2	DBS1	DBS0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	DBSn	DMA Doorbell Set for each channel. 0: ignore 1: Set the corresponding DBn bit to 1	W

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9.2.13 DMA Clock Enable (DCKE)

DCKE supports channel 0~5 and DCKE2 supports channel 6~11.

DCKE **0x13420310**

DCKE2 **0x13420410**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DCKE5	DCKE4	DCKE3	DCKE2	DCKE1	DCKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	DCKEn	DMA Clock Enable for each channel. 0: ignore 1: Set the corresponding DCKEn bit to 1	RW

9.2.14 DMA Clock Enable Set (DCKES)

DCKES supports channel 0~5 and DCKES2 supports channel 6~11.

DCKES **0x13450314**

DCKES2 **0x13450414**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DCKES5	DCKES4	DCKES3	DCKES2	DCKES1	DCKES0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DCKESn	DMA Clock Enable Set for each channel. 0: ignore 1: Set the corresponding DCKESn bit to 1 to enable corresponding channel clock	W

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9.2.15 DMA Clock Clear Set (DCKEC)

DCKEC supports channel 0~5 and DCKEC2 supports channel 6~11.

DCKEC **0x13450318**

DCKEC2 **0x13450418**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DCKEC5	DCKEC4	DCKEC3	DCKEC2	DCKEC1	DCKEC0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	R
2:0	DCKECn	DMA Clock Enable Clear for each channel. 0: ignore 1: Set the corresponding DCKECn bit to 1 to disable corresponding channel clock	W

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9.3 DMA manipulation

9.3.1 Descriptor Transfer

9.3.1.1 Normal Transfer

To do proper Descriptor DMA transfer, do as following steps:

1 First of all, open channel clock by setting DCKESn register for corresponding channel.
2 Check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0 and DCSn.INV=0.
3 Select 4 word or 8 word descriptor by DCSn.DES8.
4 For Descriptor transfer, guarantee DCSn.NDES=0.
5 Initiate channel request register DRTn.
6 Build descriptor in memory. Write the first descriptor address in DDAn and the address must be 16Bytes aligned in 4word descriptor and 32Bytes aligned in 8word descriptor. The descriptor address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DES3.DOA and the four LSB is 0x0. See Table 9-4 for the detailed 4-word descriptor structure.

   NOTE: if stride address transfer is enabled, the address must be 32Bytes aligned because DES4 needs to read out.

7 Set 1 to the corresponding bit in DDR to initiate descriptor fetch.
8 Set DMAC.DMAE=1 and expected DCSn.CTE=1 to launch DAM transfer.
9 Hardware clears the corresponding bit in DDR as soon as it starts to fetch the descriptor.
10 Waits for dma request from peripherals to start dma transfer.
11 After DMAC completes the current descriptor dma transfer, if DES0.Link=0, it sets DCSn.TT to 1. If the interrupt enabled, it will generates the corresponding interrupts.
12 If DES0.LINK=1, after DMAC completes the current descriptor dma transfer and return to fetch the next descriptor and continues dma transfer until completes the descriptor dma transfer which DES0.LINK=0.
13 When transfer end, clr DCSn.CTE to 0 to close the channel, and then clear DCSn.TT bits.

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Table 9-4 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	EACKS	External DMA DACKn output polarity select
	30	EACKM	External DMA DACKn output Mode select
	29-28	ERDM	External DMA request detection Mode
	27	EOPM	External DMA End of process mode
	26-24	Reserved	--
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	--
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	--
	10-8	TSZ	Transfer Data Size
	7-3	Reserved	--
	2	STDE	Stride transfer enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable
2nd (DES1)	31-0	DSA	Source Address
3rd (DES2)	31-0	DTA	Target Address
4th (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter
5th (DES4)	31-16	TSD	Target Stride Address
	15-0	SSD	Source Stride Address
6th(DES5)	31-6	Reserved	--
	5-0	DRT	DMA Request Type
7th(DES6)	31-0	Reserved	--
8th(DES7)	31-0	Reserved	--

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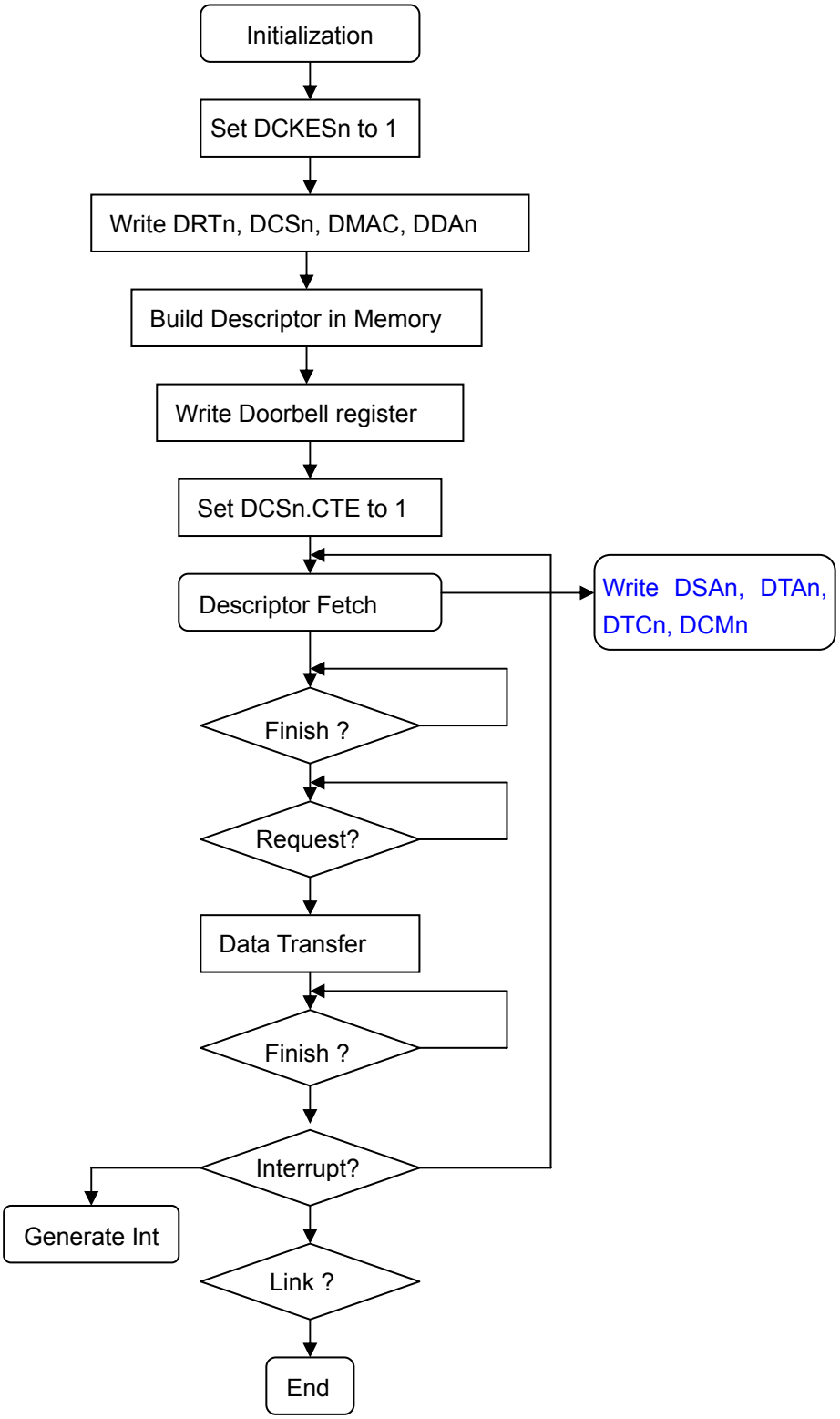


Figure 9-1 Descriptor Transfer Flow

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9.3.1.2 Stride Address Transfer

During transfer, source or target address can be not continuous and the source and target stride offset address are showed in DSDn registers.

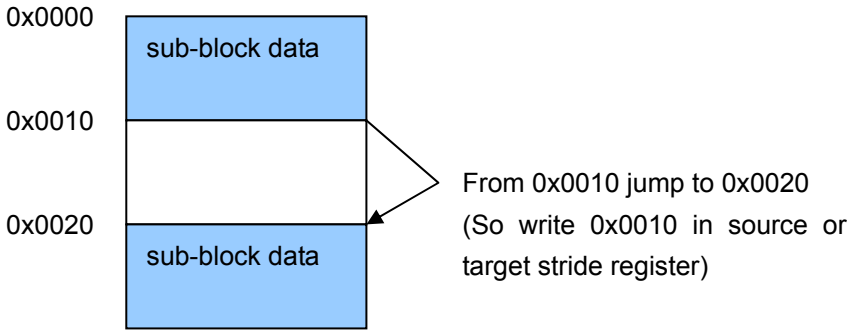


Figure 9-2 Example for Stride Address Transfer

9.3.2 No-Descriptor Transfer

To do proper DMA transfer, do as following steps:

1 First of all, check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0 and DCSn.TT=0 and DTCn=0.
2 For each channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly.
3 Set DMAC.DMAE=1 and expected DCSn.CTE=1 and DCSn.NDES=1 to launch DMA transfer.

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile corresponding bit of DIRQP is set to 1. If DCMn.TIE bit is set to 1, an interrupt request is sent to the CPU. However, during the transfer, if a DMA address error occurs, the transfer is suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP. Then an interrupt request is sent to the CPU despite of DCMn.TIE.

Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

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9.4 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

9.4.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

9.4.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals. All request types except 0x8 (value of DRT) belong to the mode. **NOTE:** the transfer byte number for one request detection according to DCMn.RDIL must be equal or less than the byte number according to receive or transmit trigger value of source or target devices.

9.5 Channel Priorities

There are two dma cores, each one supports 6 channels dma transfer. The two cores have the same priority.

In each core, there are two sets: set 1 has the higher priority than set 2, within each set priority is round robin.

Table 9-5 Relationship among DMA Transfer connection, Request & Transfer Mode

Transfer Connection	Request Mode	Transfer Mode	Data Size (bits)	Channel
External memory or memory-mapped external device and on-chip peripheral module	Auto on-chip	Single	8/16/32 16-byte/32-byte/64-byte	0~5

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9.6 Examples

9.6.1 Memory-to-memory auto request No-Descriptor Transfer

Suppose you want to do memory move between two different memory regions through channel 3, for example, moving 1KB data from address 0x20001000 to 0x20011000, do as following steps:

1 Check if (DMAC.AR==0 && DMAC.HLT==0 && DCS3.AR==0 && DCS3.HLT==0 && DCS3.NDES=1 && DTC3==0).
2 If above condition is true, set value 0 to DCS3.CTE to disable the channel 3 temporarily.
3 Set source address 0x20001000 to DSA3 and target address 0x20011000 to DTA3.
4 Suppose the data unit is word, set transfer count number 256 (1024/4) to DTC3.
5 Set auto-request (0x8) to DRT3.
6 Up to now, only the most important channel control register DCM3 is left, set it carefully:
   – Set value 1 to SAI and DAI[*1].
   – Ignore RDIL because in the case there is no explicit request signal can be detected.
   – Set word size (0) to SP and DP[*2].
   – Set value 1 to TIE to let CPU do some post process after the transfer done.
7 Set value 1 to DCS3.CTE and DMAC.DMAE to launch the transfer in channels 3.
8 When the transfer terminates normally (DTC3==0 && DCS3.TT==1), DIRQP.CIRQ3 will automatically be set value 1 and an interrupt request will be sent to CPU.
9 When CPU grants the interrupt request, in the corresponding IRQ handler, software must clear the DCS3.TT to value 0, and the behavior will automatically clear DIRQP.CIRQ3.

NOTES:

1 Either source or target is a FIFO, must not enable corresponding address increment.
2 When either source or target need be accessed through EMC (external memory controller), the real port with of the device is encapsulated by EMC, so you can set any favorite port with for it despite of the real one.

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10 AHB Bus Arbiter

10.1 Overview

AHB bus arbiter is responsible for AHB bus transactions' arbitrating to provide a fair chance for each AHB master to possess the AHB bus. The refined arbiter adopts a new arbitrating technique to fulfill the back-to-back feature of AHB protocol. In detail, total 4 priority master groups are supported, a master belonging to higher priority group will be granted first. Moreover, in each group, round-robin strategy is used. Every AHB master can dynamically asserts different priority value (0 ~ 3) accompanying with each individual bus transaction to inform arbiter to arbitrate it in corresponsive master group, thus, more balanced bus workload may be capitalized.

There are three sets of AHB buses including AHB0, AHB1 and AHB2, and they all instance this arbiter.

10.2 AHB Extension

To get better DDR performance, a little protocol extension is devised, additional AHB master owned signals are added for AHB protocol, they are:

emergency – *tell AHB arbiter to try to grant the current granted master's next time's BUSREQ when no other pending bus request with higher priority exists. AHB master can assert this hint signal when its continuous bus transactions locate in the same DDR bank and the same DDR row, or it is a real-time device thus interrupting its several continuous bus transactions may cause HW error. The signal must keep active when an AHB master wants to perform several bus transactions with above features back-to-back. Its 0->1 transition should be active accompanying with BUSREQ of first bus transaction, and at least at the last AP phase of the last time's bus transaction, it should be set to inactive 0.*

curr_len[6:0] – *data phase beats of a flexible fixed-length bus transaction. 0 denotes inactive; 2 ~ 64 is available. The signal must be active/inactive at the NONSEQ phase.*

next_len[6:0] – *data phase beats of next bus transaction with a flexible fixed-length. 0 denotes inactive; 2 ~ 64 is available. The signal must be active/inactive at the NONSEQ phase.*

offset[6:0] – *start address' offset between next bus transaction and current granted bus transaction. 0 ~ 127 is available. The signal must be active/inactive at the NONSEQ phase.*

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10.3 Register Descriptions

The base addresses for memory-mapped registers of arbiter are listed below:

AHB0: 0x13000000

AHB1: 0x13200000

AHB2: 0x13400000

Table 10-1 AHB Bus Arbiter Registers List

Register Name	Offset	Size	R/W	Reset Value	Description
RPIOR	0x00	32	R/W	0x00000000	Default master priorities.
CTRL	0x04	32	R/W	0x00000000	AHB monitor control.
CLKL	0x08	32	R/W	undefined	AHB clock counter low.
EVENT0L	0x0C	32	R/W	undefined	AHB bus event 0 counter low.
EVENT1L	0x10	32	R/W	undefined	AHB bus event 1 counter low.
EVENTH	0x14	32	R/W	undefined	AHB bus event & clock counter high.
WATCHCTRL	0x18	32	RW	0x00000000	AHB bus watch control.
WATCHADDR	0x1C	32	RW	undefined	AHB bus watch address.
WATCHAMSK	0x20	32	RW	undefined	AHB bus watch address mask.
WATCHDATA	0x24	32	RW	undefined	AHB bus watch data.
WATCHDMSK	0x28	32	RW	undefined	AHB bus watch data mask.

10.3.1 Priority Order Register

HARB_PRIOR **offset 0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										PRIMX		PRIM9		PRIM8		PRIM7		PRIM6		PRIM5		PRIM4		PRIM3		PRIM2		PRIM1		PRIM0	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0

Bits	Name	Description	R/W
31:22	Reserved	Writing has no effect, read as zero.	R
21:0	PRI	PRIM0 ~ PRIMX. Default master's priority. Any AHB master can determine how to assert its priority. If an AHB master does not provide its priority aggressively, Its default static priority can be set to relative bit fields by SW. Value 0 ~ 3 are available, and 0 is the lowest priority.	RW

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10.3.2 Monitor Control Register

HARB_MC offset 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								M1				M0				EV1				EV0				Reserved					EV1E	EV0E	CLKE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Write is ignored, read as zero.	R
23:20	M1	Monitored Master ID in monitor channel 1[*1].	RW
19:16	M0	Monitored Master ID in monitor channel 0[*1].	RW
15:12	EV1	AHB bus event encoding for monitor channel 1[*2].	RW
11:8	EV0	AHB bus event encoding for monitor channel 0[*2].	RW
7:3	Reserved	Write has no effect, read as zero.	R
2	EV1E	Enable monitor channel 1. 0: disable; 1: enable.	RW
1	EV0E	Enable monitor channel 0. 0: disable; 1: enable.	RW
0	CLKE	AHB clock counting enable. 0: disable; 1: enable.	RW

NOTES:

1 [*1] denotes the masterID encoding is described in the68H
2 Table 10-3 AHB0 Master-ID.
3 [*2] the event encoding is described in the 2569H
4 Table 10-2 AHB Bus Monitor Events.

Table 10-2 AHB Bus Monitor Events

Events	Full Name	Comment
0	bus transaction cycles	exclude idle cycles.
1	bus transaction times	count NONSEQ times.
2	grant latency[*3]	count pending request (not granted) cycles.
3	critical grant latency trigger[*4]	Once the grant latency for a bus transaction exceeds the critical value preset in the counter low register, the associative counter high register will accumulate 1.
4	single beat transaction times	BURST type is SINGLE.
5	fixed length burst transaction times	BURST type is INCR4/8/16/32 or WRAP4/8/16/32.
6	INCR burst transaction times	BURST type is INCR.
7	critical transaction cycles trigger[*5]	Once the active transaction cycles for a bus transaction exceeds the critical value preset in the counter low register, the associative counter high

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		register will accumulate 1.
8~15	reserved	

NOTE: *3, *4, *5 denotes that such events are undefined when masterID is ALL.

Table 10-3 AHB0 Master-ID

Masters	Full Name
0	CIM
1	LCD
2	IPU
3	AXI-to-AHB BRIDGE
4	DMA
5	-
6	CORE0
7	VPU
8	-
9	AOSD
10	AHB2-to-AHB0 BRIDGE
11~14	-
15	ALL (events triggered by any master should be monitored)

Table 10-4 AHB1 Master-ID

Masters	Full Name
0	CORE0
1	IDCT
2	MOTION
3	DBLK
4	MDMA1
5	MDMA0
6	CABAC
7	AUX
8~14	-
15	ALL (events triggered by any master should be monitored)

Table 10-5 AHB2 Master-ID

Masters	Full Name
0	USB
1	-
2	UHC

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3	BDMA
4	ETHC
5	-
6	AHB2-to-AHB0 BRIDGE
10	DMA
7~9, 11~14	-
15	ALL (events triggered by any master should be monitored)

10.3.3 AHB Clock Counter Low Register

HARB_CLKL **offset 8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKL																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	CLKL	Record the low 32 bits of AHB clock counter.	RW

10.3.4 Event0 Low Register

HARB_EVENT0L **offset 12**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EVENT0L																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	EVENT0L	Record the low 32 bits of event 0 counter.	RW

10.3.5 Event1 Low Register

HARB_EVENT1L **offset 16**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EVENT1L																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	R/W
31:0	EVENT1L	Record the low 32 bits of event 1 counter.	RW

10.3.6 Event High Register

HARB_EVENTH **offset 20**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKH																EVENT1H								EVENT0H							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:16	CLKH	Record the high 16 bits of AHB clock counter.	RW
15:8	EVENT1H	Record the high 8 bits of event 1 counter.	RW
7:0	EVENT0H	Record the high 8 bits of event 0 counter.	RW

Note that fields of EVENTH register will not overflow automatically. For example, when EVENT1H reaches 0xFF during monitoring, it remains the value until software modifies it.

10.3.7 AHB Watch Control Register

WATCH_CTRL **offset 24**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WF	RF	MasterID														Reserved							IRQE	Reserved					DE	WE	RE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	0	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31	WF	0: no write watch point detected; 1: a write watch point is detected.	RW
30	RF	0: no read watch point detected; 1: a read watch point is detected.	RW
29:16	MasterID	0: ID of the master just triggering watch point, one-hot encoding.	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8	IRQE	Interrupt enable. 1: if WF or RF is set value 1, an interrupt request arises immediately.	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	DE	Watch data enable. 1: enable.	RW
1	WE	Switch of triggering watch point by write. 1: enable.	RW
0	RE	Switch of triggering watch point by read. 1: enable.	RW

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10.3.8 AHB Watch Address Register

WATCH_ADDR offset 28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	ADDR	Watch address to be monitored.	RW

10.3.9 AHB Watch Address Mask Register

WATCH_AMSK offset 32

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MASK																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MASK	If a bit is set 0, which means in WATCH_ADDR, corresponding bit position should be monitored, otherwise, the bit position should be ignored.	RW

10.3.10 AHB Watch Data Register

WATCH_DATA offset 36

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	DATA	Read or Write data to be monitored.	RW

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10.3.11 AHB Watch Data Mask Register

WATCH_DMSK																														offset 40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MASK																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MASK	If a bit is set 0, which means in WATCH_DATA, corresponding bit position should be monitored, otherwise, the bit position should be ignored.	RW

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11 Clock Reset and Power Controller

11.1 Overview

The Clock & Power management block consists of three parts: Clock control, PLL control, and Power control, Reset control.

The Clock control logic can generate the required clock signals including CCLK for CPU, HCLK for the AHB0 and DDR，AUX_CCLK and H1CLK for VPU , H2CLK for the AHB2 bus peripherals, PCLK for the APB bus peripherals. The Chip has two Phase Locked Loops (PLL): for CCLK, AUX_CCLK, H0CLK, H1CLK, H2CLK and PCLK, GPUCLK, SSICLK, MSCLK, LPCLK, USBCLK, I2SCLK. The clock control logic can make slow clocks without PLL and connect/disconnect the clock to each peripheral block by software, which will reduce the power consumption.

For the power control logic, there are various power management schemes to keep optimal power consumption for a given task. The power management block can activate four modes: NORMAL mode, DOZE mode, IDLE mode, SLEEP mode.

Support power supply shut down for 3 power domain separately. Software may separately shut down AHB1 module. When in Sleep mode, software may shut down J1. Thus, the chip may best reduce leakage current.

For reset control logic, the hardware reset and hibernate reset is extended to more 40ms. It controls or distributes all of the system reset signals.

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11.2 Clock Generation UNIT

The clock generation unit (CGU) contains one PLL driven by an external oscillator and the clock generation circuit from which the following clocks are derived.

Signal	Description
CCLK	Fast clock for internal operations such as executing instructions from the cache. It can be gated during doze and idle mode when all the criteria to enter a low power are met.
AUX_CCLK	AUX_CPU Clock.
H0CLK	AHB0 and DDR Bus Clock.
H1CLK	VPU Clock.
H2CLK	AHB2 Speed Bus Clock.
PCLK	APB Speed Bus Clock.
CKO	DDR or SDRAM Clock.
LPCLK	LCD pixel clock.
TVECLK	TV encoder 27M clock.
CIM_MCLK	Clock output from CIM module.
CIM_PCLK	Clock input to CIM module.
GPUCLK	GPU clock.
I2SCLK	I2S codec clock.
BITCLK	AC97 bit clock.
PCMCLK	PCM clock.
MSCCLK	MSC clock.
SSICLK	SSI clock.
TSSICLK	TSSI clock.
EXCLK	12M clock output for UART I2C TCU USB2.0-PHY AUDIO CODEC.

Feature:

- On-chip 2MHz~27MHZ oscillator circuit
- On-chip 32.768KHZ oscillator circuit
- One two-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, H0CLK, H1CLK, PCLK, H2CLK, CKO and LPCLK, GPUCLK, MSCCLK , UHCCLK, SSICLK frequency can be changed separately for software by setting registers
- SSI clock supports 50M clock
- MSC clock supports 50M clock
- Functional-unit clock gating
- Shut down power supply for J1, VPU

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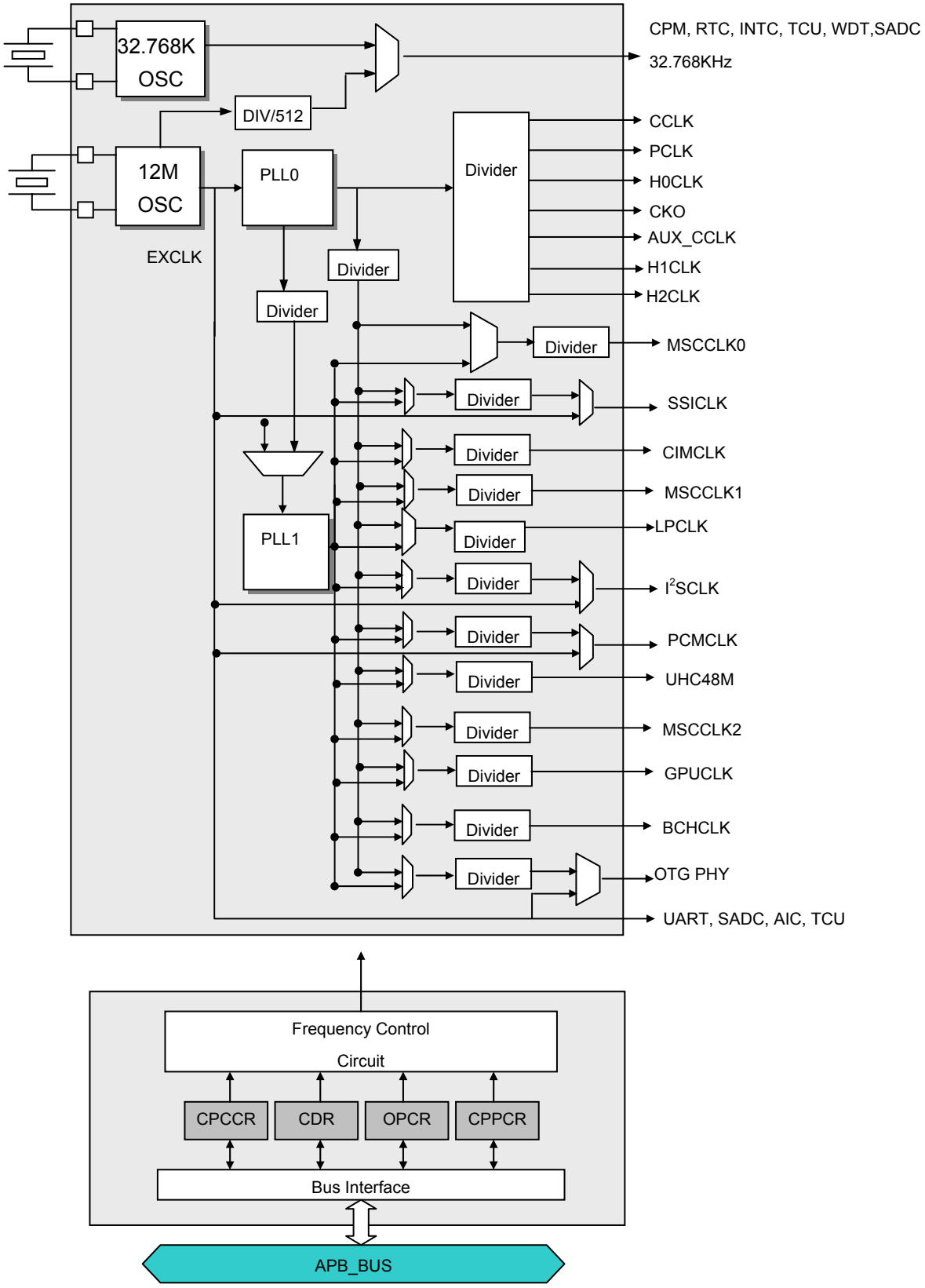
11.2.1 Pin Description

Name	I/O	Description
RTCLK_XI	Input	32.768KHZ Oscillator input signal.
RTCLK_XO	Output	32.768KHZ Oscillator output signal.
EXCLK	Input	Oscillator input signal.
EXCLKO	Output	Oscillator output signal.
CIM_MCLK	Output	Clock output from CIM module signal.
CIM_PCLK	Input	Clock input to CIM module signal.
LPCLK	Output	LCD pix clock signal.
CKO	Output	DDR clock signal.
TSSICLK	Input	TSSI clock signal.
BITCLK	Inout	I2S/AC97 bit clock.
PCMCLK	Inout	PCM bit clock.
MSC_CLK	Output	Clock output For MMC/SD Card signal.
SSI_CLK	Output	Clock output from SSI module signal.

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11.2.2 CGU Block Diagram

Following figure illustrates a block diagram of CGU.



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11.2.3 Clock Overview

There is an internal PLL in this chip. PLL input clock is an external input clock EXCLK. Theoretically, EXCLK can be 2MHz ~ 27MHz.

CCLK is CPU clock. It is usually the fastest clock in the chip. This clock represents the chip speed.

AUX_CCLK is for AUX_CPU clock , it is should equal to half of CCLK.

H0CLK is for on chip high speed peripherals connected to AHB0 bus.

H1CLK is for on chip high speed peripherals connected to VPU bus.

H2CLK is for on chip high speed peripherals connected to AHB2 bus.

PCLK is for on chip slow speed peripherals connected to APB bus.

CCLK, AUX_CCLK, H0CLK, H1CLK, H2CLK, PCLK are synchronous clocks that may have different frequencies. They are from the same clock source, the on chip PLL output clock in most cases. H0CLK , H1CLK, H2CLK frequency can be equal to CCLK/2 or divided CCLK by an integer. PCLK frequency can be equal to H2CLK/2 or divided CCLK by an integer.

AC97 in AIC module needs a 12.288MHz BIT clock. It is input from the external AC97 CODEC chip or other clock source. I2S and PCM clock are generated from PLL output clock.

Besides PLL input, EXCLK also provides device clock or one of device clocks for many peripherals, such as, UART, TCU, SSI, SADC and WDT.

Device clock of MSC (MMC/SD) is taken from software divided PLL0/PLL1 output clock.

USB device and host controllers need a 48MHz USB clock. USB clock can be selected by software divided PLL0/PLL1 output clock.

Device clock of SSI is taken from software divided PLL output clock. or 12M from oscillator.

LCD’s pixel clock is generated from PLL output clock, which are divided by one independent dividers.

GPU clock is generated from PLL output clock, which is divided by one independent dividers.

BCH clock is generated from PLL output clock, which is divided by one independent dividers.

The slowest clock is RTCLK, which is usually 12M/512 or 32768Hz.

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11.2.4 CGU Registers

All CGU register 32bit access address is physical address.

Table 11-1 CGU Registers Configuration

Name	description	RW	Reset Value	Address	Access Size
CPCCR	Clock Control Register	RW	0x01010110	0x10000000	32
CPPCR	PLL Control Register0	RW	0x????0020	0x10000010	32
CPPSR	PLL switch and status register	RW	0x80000000	0x10000014	32
CPPCR1	PLL Control Register1	RW	0x????0002	0x10000030	32
CPSPR	CPM Scratch Pad Register	RW	0x????????	0x10000034	32
CPSPPR	CPM Scratch Protected Register	RW	0x0000a5a5	0x10000038	32
USBPCR	USB Parameter control register	RW	0x429919b8	0x1000003C	32
USBRDT	USB Reset Detect Timer Register	RW	0x02000096	0x10000040	32
USBVBFIL	USB jitter filter Register	RW	0x00ff0080	0x10000044	32
USBPCR1	USB Parameter control register 1	RW	0x00000004	0x10000048	32
USBCDR	OTG PHY clock divider Register	RW	0x00000000	0x10000050	32
I2SCDR	I2S device clock divider Register	RW	0x00000000	0x10000060	32
LPCDR	LCD pix clock divider Register	RW	0x00000000	0x10000064	32
MSC0CDR	MSC0 clock divider Register	RW	0x00000000	0x10000068	32
UHCCDR	UHC 48M clock divider Register	RW	0x00000000	0x1000006C	32
SSICDR	SSI clock divider Register	RW	0x00000000	0x10000074	32
CIMCDR	CIM MCLK clock divider Register	RW	0x00000000	0x1000007C	32
PCMCDR	PCM device clock divider Register	RW	0x00000000	0x10000084	32
GPUCDR	GPU clock divider Register	RW	0x00000000	0x10000088	32
MSC1CDR	MSC1 clock divider Register	RW	0x80000000	0x100000A4	32
MSC2CDR	MSC2 clock divider Register	RW	0x80000000	0x100000A8	32
BCHCDR	BCH clock divider Register	RW	0x00000000	0x100000AC	32
CPM_INTR	CPM interrupt Register	RW	0x00000000	0x100000B0	32
CPM_INTRE	CPM interrupt Enable Register	RW	0x00000000	0x100000B4	32

11.2.4.1 Clock Control Register

The Clock Control Register (CPCCR) is a 32-bit read/write register, which controls CCLK, AUX_CCLK, H0CLK, H1CLK, H2CLK and PCLK division ratios. It is initialized to 0x01010110 by any reset. Only word access can be used on CPCCR.

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CPCCR **0x10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	MEM	Reserved		H1DIV				Reserved	CE	PCS	Reserved	H2DIV				C1DIV				PDIV				H0DIV				CDIV			
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	MEM	0: mobile ddr; 1: ddr or ddr2 memory.	RW
29:28	Reserved	Writing has no effect, read as zero.	R
27:24	H1DIV	Divider for VPU Bus Clock Frequency. Specified the H1CLK division ratio.	RW
22	CE	change enable. If CE is 1, writes on CDIV, C1DIV, H2DIV, H0DIV, PDIV, H1DIV, USBCDR, LPCDR, CIMCDR, MSCCDR, SSICDR, BCHCDR UHCCDR, GPUCDR , PCMCDR , I2SCDR will start a frequency changing sequence immediately. When CE is 0, writes on CDIV, C1DIV, H2DIV, HDIV, PDIV, H0DIV, USBCDR, LPCDR, CIMCDR, MSCCDR, SSICDR, UHCDR, PCMCDR, GPUCDR, I2SCDR will not start a frequency changing sequence immediately. The division ratio is actually updated in PLL multiple ratio changing sequence or PLL Disable Sequence. 0: Division ratios are updated in PLL multiple ratio changing sequence or PLL Disable Sequence 1: Division ratios are updated immediately	RW
21	PCS	PLL out clock source clock selection. It supplies source clock for MSC I2S LCD UHC OTG SSI PCM GPU GPS BCH. 0: divider clock source is PLL output divided by 2 1: divider clock source is PLL output Software should set the bit according to various needs.	RW
20	Reserved	Writing has no effect, read as zero.	R

Bit 27~24: H1DIV				Description
0	0	0	0	X1
0	0	0	1	X1/2
0	0	1	0	X1/3
0	0	1	1	X1/4
0	1	0	0	X1/6
0	1	0	1	X1/8
0	1	1	0	X1/12
0	1	1	1	X1/16
1	0	0	0	X1/24
1	0	0	1	X1/32
Other Value				Reserved

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<table>
<tr><td>19:16</td><td>H2DIV</td><td>Divider for AHB2 Clock Frequency. Specified the H2CLK division ratio.
<table>
<tr><th colspan="4">Bit 19~16: H2DIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X1/12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X1/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X1/24</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>X1/32</td></tr>
<tr><td colspan="4">Other Value</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>15:12</td><td>C1DIV</td><td>Divider for AUX CPU Frequency. Specified the AUX_CLK division ratio.
<table>
<tr><th colspan="4">Bit 15~12: C1DIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X1/12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X1/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X1/24</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>X1/32</td></tr>
<tr><td colspan="4">Other Value</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>11:8</td><td>PDIV</td><td>Divider for Peripheral Clock Frequency. Specified the PCLK division ratio.
<table>
<tr><th colspan="4">Bit 11~8: PDIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X1/12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X1/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X1/24</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>X1/32</td></tr>
<tr><td colspan="4">Other Value</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>7:4</td><td>H0DIV</td><td>Divider for AHB0 Clock Frequency. Specified the H0CLK division ratio.
<table>
<tr><th colspan="4">Bit 7~4: H0DIV</th><th>Description</th></tr>
</table></td><td>RW</td></tr>
</table>

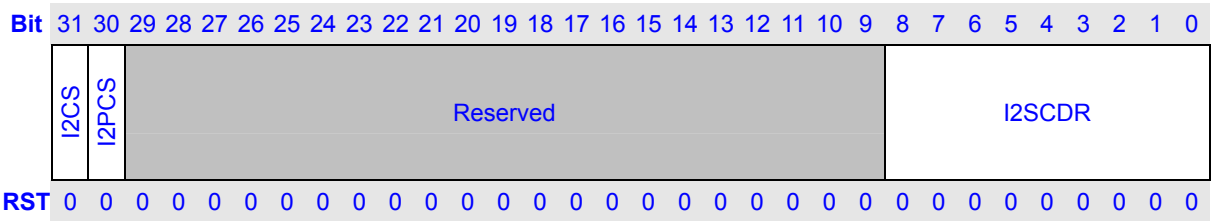
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			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/6	
			0	1	0	1	X1/8	
			0	1	1	0	X1/12	
			0	1	1	1	X1/16	
			1	0	0	0	X1/24	
			1	0	0	1	X1/32	
			Other Value				Reserved	
3:0	CDIV	Divider for CPU Clock Frequency. Specifies the CCLK division ratio.						RW
			Bit 3~0: CDIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/6	
			0	1	0	1	X1/8	
			0	1	1	0	X1/12	
			0	1	1	1	X1/16	
			1	0	0	0	X1/24	
			1	0	0	1	X1/32	
			Other Value				Reserved	

11.2.4.2 I2S device clock divider Register

I2S device clock divider Register (I2SCDR) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SCDR.

I2SCDR **0x10000060**



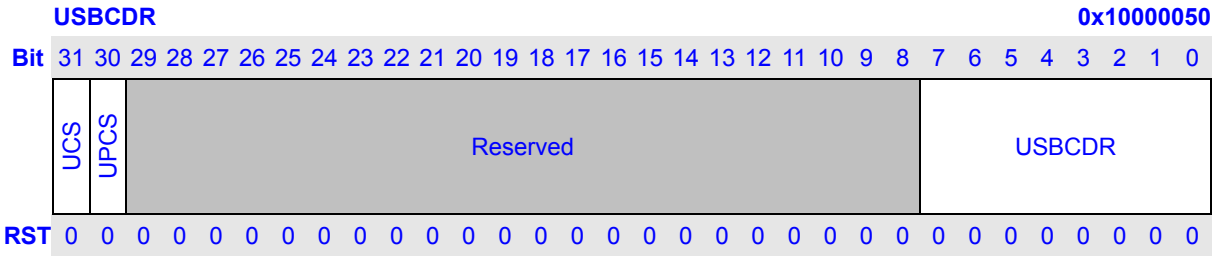
Bits	Name	Description	RW
31	I2CS	I2S Clock Source Selection. Selects the I2S clock source between PLL output and pin EXCLK. 0: I2S clock source is EXCLK	R

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		1: I2S clock source is PLL output divided by I2SDIV If EXCLK is 12M, please don't change the bit.	
30	I2PCS	0: select PLL0 clock output; 1: select PLL1 clock output.	
29:9	Reserved	Writing has no effect, read as zero.	R
8:0	I2SCDR	Divider for I2S Frequency. Specified the I2S device clock division ratio, which varies from 1 to 512 (division ratio = I2SCDR + 1). When EXCLK is 12M, don't care the bit.	RW

11.2.4.3 USB clock divider Register

USB clock divider Register (USBCDR) is a 32-bit read/write register that specifies the divider of OTG PHY clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on USBCDR.

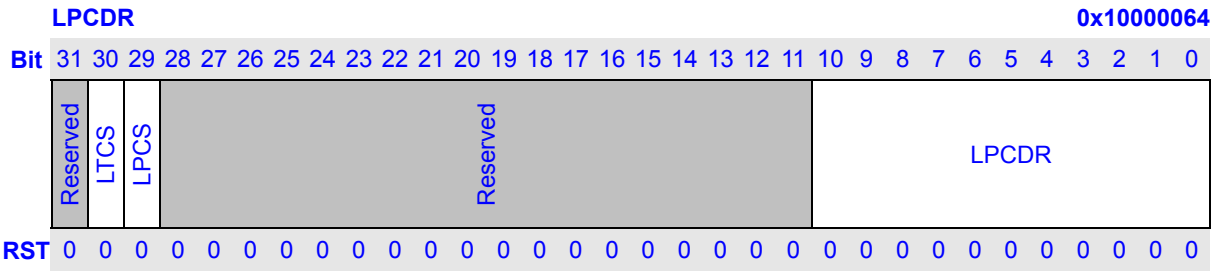


Bits	Name	Description	RW
31	UCS	OTG PHY Clock Source Selection. Selects the OTG PHY clock source between PLL output and pin EXCLK. 0: OTG clock source is pin EXCLK 1: OTG clock source is PLL output If EXCLK is 12M, please don't change the bit.	RW
30	UPCS	0: select PLL0 clock output 1: select PLL1 clock output	
29:9	Reserved	Writing has no effect, read as zero.	R
7:0	USBCDR	Divider for OTG PHY Clock Frequency. When OTG PHY clock source is PLL (UCS bit is 1), this field specified the OTG PHY clock division ratio, which varies from 1 to 256 (division ratio = USBCDR + 1).	RW

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11.2.4.4 LCD pix clock divider Register

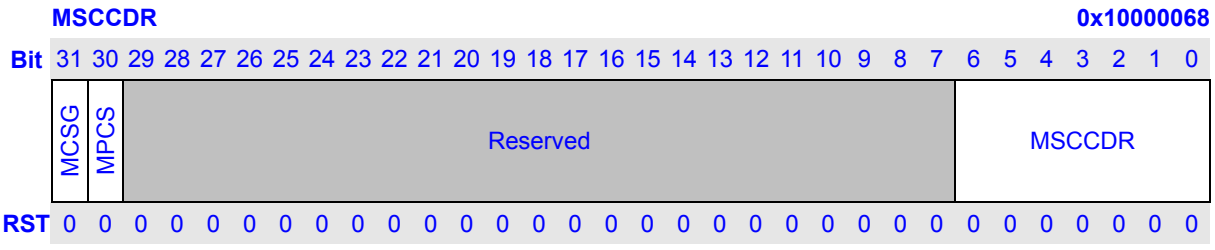
LCD pix clock divider Register (LPCDR) is a 32-bit read/write register that specifies the divider of LCD pixel clock (LPCLK). This register is initialized to 0x00000000 only by any reset. Only word access can be used on LPCDR.



Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	LTCS	LCD TV Encoder or Panel pix clock Selection. 0: pix clock is used as LCD PANEL 1: pix clock is used as TV ENCODER	RW
29	LPCS	0: select PLL0 clock output 1: select PLL1 clock output	RW
29:11	Reserved	Writing has no effect, read as zero.	R
10:0	LPCDR	Divider for Pixel Frequency. Specified the LCD pixel clock (LPCLK) division ratio, which varies from 1 to 2048 (division ratio = LPCDR + 1).	RW

11.2.4.5 MSC0 device clock divider Register

MSC0 device clock divider Register (MSC0CDR) is a 32-bit read/write register that specifies the divider of MSC device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MSC0CDR.



Bits	Name	Description	RW
31	MCSG	MSC Clock Source Gate. Whether gate MSC clock divider. 0: clock divider is on, clock is running 1:clock divider is off , clock is stopped	RW
30	MPCS	0: select PLL0 clock output 1: select PLL1clock output	RW

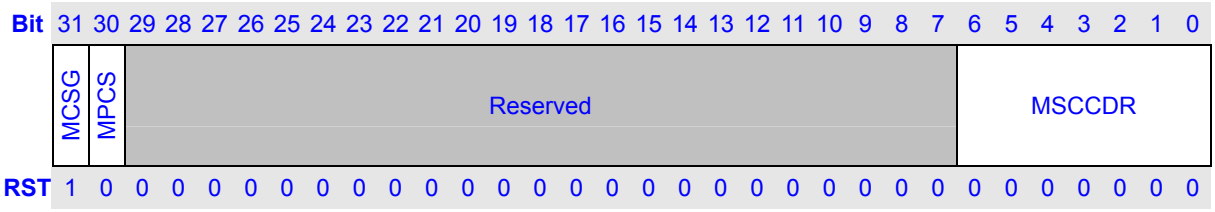
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29:7	Reserved	Writing has no effect, read as zero.	R
6:0	MSCCDR	Divider for MSC Frequency. Specified the MSC device clock division ratio, which varies from 1 to 128 (division ratio = MSCCDR + 1).	RW

11.2.4.6 MSC1 device clock divider Register

MSC1 device clock divider Register (MSC1CDR) is a 32-bit read/write register that specifies the divider of MSC device clock . This register is initialized to 0x80000000 only by any reset. Only word access can be used on MSC1CDR.

MSCCDR **0x100000A4**

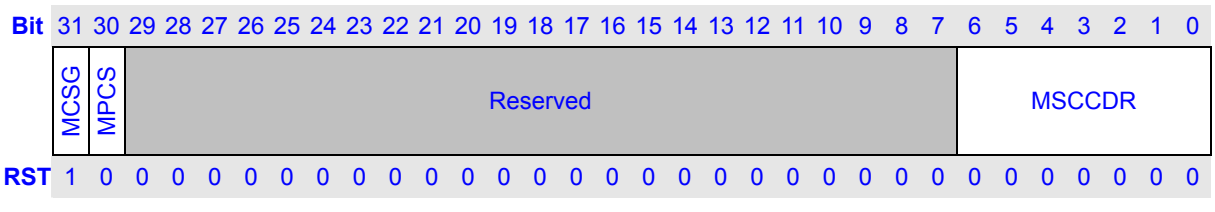


Bits	Name	Description	RW
31	MCSG	MSC Clock Source Gate. Whether gate MSC clock divider. 0: clock divider is on, clock is running 1:clock divider is off , clock is stopped	RW
30	MPCS	0: select PLL0 clock output 1: select PLL1clock output	RW
29:7	Reserved	Writing has no effect, read as zero.	R
6:0	MSCCDR	Divider for MSC Frequency. Specified the MSC device clock division ratio, which varies from 1 to 128 (division ratio = MSCCDR + 1).	RW

11.2.4.7 MSC2 device clock divider Register

MSC2 device clock divider Register (MSC2CDR) is a 32-bit read/write register that specifies the divider of MSC device clock . This register is initialized to 0x80000000 only by any reset. Only word access can be used on MSC2CDR.

MSCCDR **0x100000A8**



Bits	Name	Description	RW
31	MCSG	MSC Clock Source Gate. Whether gate MSC clock divider. 0: clock divider is on, clock is running	RW

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		1:clock divider is off , clock is stopped	
30	MPCS	0: select PLL0 clock output 1: select PLL1clock output	RW
29:7	Reserved	Writing has no effect, read as zero.	R
6:0	MSCCDR	Divider for MSC Frequency. Specified the MSC device clock division ratio, which varies from 1 to 128 (division ratio = MSCCDR + 1).	RW

11.2.4.8 UHC device clock divider Register

UHC device clock divider Register (UHCCDR) is a 32-bit read/write register that specifies the divider of UHC 48M device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on UHCCDR.

UHCCDR **0x1000006C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UHCS		UPCS	Reserved																						UHCCDR						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	UHCS	00: UHC clock source is PLL divider output 01: UHC clock source is PLL divider output 10: UHC clock source is OTG_PHY 11: UHC clock source is external PIN	RW
29	UHPCS	0: select PLL0 clock output 1: select PLL1 clock output	RW
30:6	Reserved	Writing has no effect, read as zero.	R
3:0	UHCCDR	Divider for UHC Frequency. Specified the UHC 48M device clock division ratio, which varies from 1 to 64 (division ratio = UHCCDR + 1).	RW

11.2.4.9 SSI device clock divider Register

SSI device clock divider Register (SSICDR) is a 32-bit read/write register that specifies the divider of SSI device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SSICDR.

SSICDR **0x10000074**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCS		SPCS	Reserved																						SSICDR						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31	SCS	SSI Clock Source Selection. Selects the SSI clock source between PLL output and pin EXCLK. 0: SSI clock source is EXCLK 1: SSI clock source is PLL output divided by SSICDR.	R
30	SPCS	0: select PLL0 clock output 1: select PLL1 clock output	RW
29:7	Reserved	Writing has no effect, read as zero.	R
6:0	SSICDR	Divider for SSI Frequency. Specified the SSI device clock division ratio, which varies from 1 to 128 (division ratio = SSICDR + 1).	RW

11.2.4.10 CIM MCLK clock divider Register

CIM mclk clock divider Register (CIMCDR) is a 32-bit read/write register that specifies the divider of CIM mclk clock (CIM_MCLK). This register is initialized to 0x00000000 only by any reset. Only word access can be used on CIMCDR.

CIMCDR 0x1000007C

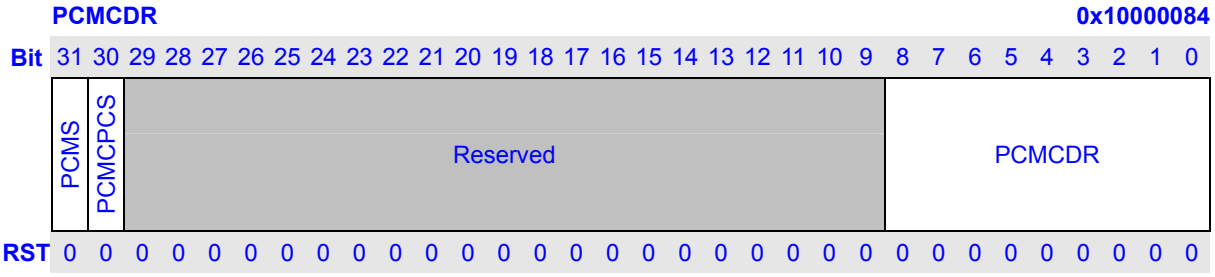
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIMPCS	Reserved																							CIMCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31	CIMPCS	0: select PLL0 clock output 1: select PLL1 clock output	RW
30:8	Reserved	Writing has no effect, read as zero.	R
7:0	CIMCDR	Divider for CIM MCLK Frequency. Specified the CIM MCLK clock (CIM_MCLK) division ratio, which varies from 1 to 256 (division ratio = CIMCDR + 1).	RW

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11.2.4.11 PCM device clock divider Register

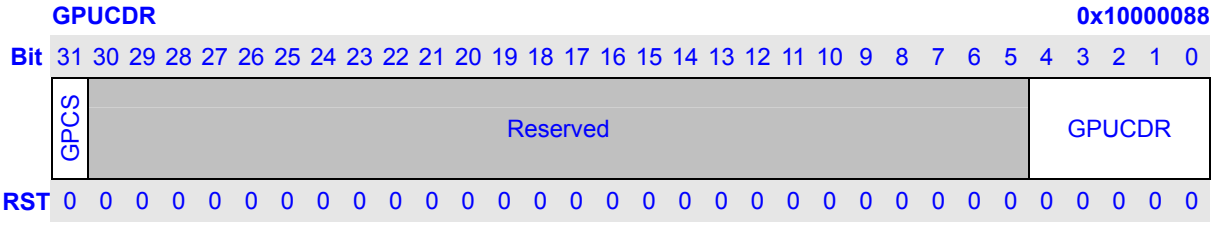
PCM device clock divider Register (PCMCDR) is a 32-bit read/write register that specifies the divider of PCM device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on PCMCDR.



Bits	Name	Description	RW
31	PCMS	PCM source clock Selection. 0: PCM source clock is pin EXCLK 1: PCM source clock is PLL divider output	RW
30	PCMPCS	0: select PLL0 divider output 1: select PLL1 divider output	
30:9	Reserved	Writing has no effect, read as zero.	R
8:0	PCMCDR	Divider for PCM Frequency. Specified the PCM device clock division ratio, which varies from 1 to 512 (division ratio = PCMCDR + 1).	RW

11.2.4.12 GPU clock divider Register

GPU clock divider Register (GPUCDR) is a 32-bit read/write register that specifies the divider of GPU clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on GPUCDR.



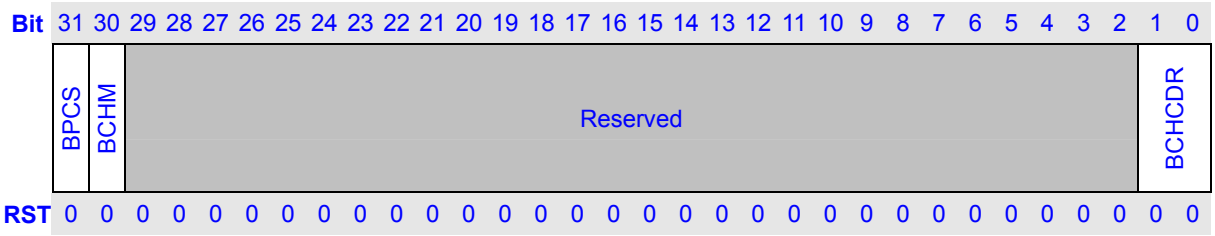
Bits	Name	Description	RW
31	GPCS	0: select PLL0 divider output 1: select PLL1 divider output	RW
30:3	Reserved	Writing has no effect, read as zero.	R
4:0	GPUCDR	Divider for GPU Frequency. Specified the GPU clock division ratio, which varies from 1 to 32 (division ratio = GPUCDR + 1).	RW

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11.2.4.13 BCH clock divider Register

BCH clock divider Register (BCHCDR) is a 32-bit read/write register that specifies the divider of BCH clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on BCHCDR.

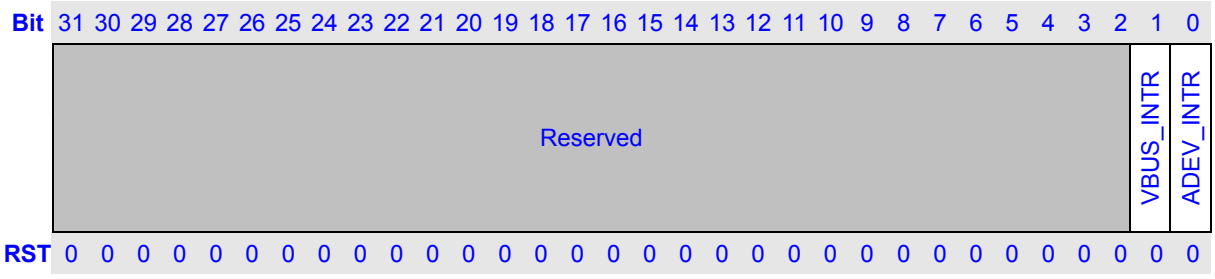
GPUCDR 0x100000AC



Bits	Name	Description	RW
31	BPCS	0: select PLL0 divider output 1: select PLL1 divider output	RW
30	BCHM	0: hardware frequency change 1: software frequency change	RW
30:3	Reserved	Writing has no effect, read as zero.	R
1:0	BCHCDR	Divider for BCH Frequency. Specified the BCH clock division ratio, which varies from 1 to 4 (division ratio = BCHCDR + 1).	RW

11.2.4.14 CPM interrupt Register

CPM_INTR 0x100000B0



Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTR	B device insert interrupt.	R
0	ADEV_INTR	A device insert interrupt.	R

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11.2.4.15 CPM interrupt enable Register

CPM_INTRE 0x100000B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTRE	ADEV_INTRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTRE	B device insert interrupt enable.	RW
0	ADEV_INTRE	A device insert interrupt enable.	RW

11.2.4.16 CPM Scratch Pad Protected Register

The Scratch Pad Protected Register is reset to 0x0000a5a5. When CPSPPR value equals to 0x00005a5a, software can write the CPSPR.

CPSPPR 0x10000038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPSPPR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CPSPPR	The value is only = 0x00005a5a, software can write the CPSPR.	RW

11.2.4.17 CPM Scratch Pad Register

The Scratch Pad Register is a 32-bit read/write register that allows software to preserve some critical data . It is not initialized by poweron and WDT reset.

CPPSR 0x10000034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPPSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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11.2.4.18 USB Parameter Control Register

The USBPCR is a 32-bit read/write register that allows software to control OTG PHY some functions. It is initialized to 0x429919b8.

USBPCR **0x1000003C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USB_MODE	AVLD_REG	IDPULLUP_MASK		INCR_MASK	CLK12_EN	COMONONN	VBUSVLDEXT	VBUSVLDEXTSEL	POR	SIDDQ	OTGDISABLE	COMPDISTUNE			OTGTUNE			SQRXTUNE			TXFSLSTUNE				TXPREMTUNE		TXHSXVTUNE			TXVREFTUNE			
RST	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	0	0	0

Bits	Name	Description	RW
31	USB_MODE	0: work as USB device 1: work as OTG	RW
30	AVLD_REG	This bit is used to set “avalid”(VBUS above A-device session threshold) signal.	RW
29:28	IDPULLUP_MASK	These 2 bits control “idpullup” signal in otg mode. 2’b1x: “idpullup” always active 2’b01: “idpullup” always active when usb suspend 2’b00: use “idpullup” from otg controller	RW
27	INCR_MASK	This bit controls whether the ahb interface enhancement for “incr transfer” takes effect. Set this bit to 0 will active the enhancement.	RW
26	CLK12_EN	OTG PHY reference clock enable.	RW
25	COMMONONN	This bit is the OTG PHY common block power down control signal. 0: The common blocks remain powered in suspend mode 1: The common blocks are powered down in suspend mode	RW
24	VBUSVLDEXT	This bit controls OTG PHY VBUSVLDEXT signal.	RW
23	VBUSVLDEXTSEL	This bit controls OTG PHY VBUSVLDEXTSEL signal.	RW
22	POR	This bit controls OTG PHY power on reset.	RW
21	SIDDQ	This bit is the OTG PHY analog blocks power down signal.	RW
20	OTG_DISABLE	This bit is the power control for otg block in OTG PHY.	RW
19:17	COMPDISTUNE	These bits control disconnect threshold adjustment.	RW

3’b111	+4.5%
3’b110	+3%
3’b101	+1.5%
3’b100	Default
3’b011	-1.5%

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		3’b010	-3%		
		3’b001	-4.5%		
		3’b000	-6%		
16:14	OTGTUNE	These bits control VBUS valid threshold adjustment.		RW	
		3’b111	+4.5%		
		3’b110	+3%		
		3’b101	+1.5%		
		3’b100	Default		
		3’b011	-1.5%		
		3’b010	-3%		
		3’b001	-4.5%		
		3’b000	-6%		
13:11	SQRXTUNE	These bits control squelch threshold adjustment.		RW	
		3’b111	-20%		
		3’b110	-15%		
		3’b101	-10%		
		3’b100	-5%		
		3’b011	default		
		3’b010	+5%		
		3’b001	+10%		
		3’b000	+15%		
10:7	TXFSLSTUNE	These bits control FS/LS source impedance adjustment.		RW	
		4’b1111	-5%		
		4’b0111	-2.5%		
		4’b0011	Default		
		4’b0001	+2.5%		
		4’b0000	+5%		
6	TXPREEMPHTUNE	This bit controls HS transmitter Pre-emphasis enable. 1: enable 0: disable		RW	
5:4	TXHSXVTUNE	These bits adjust the voltage at which dp and dm signals cross while transmitting in HS mode.		RW	
		2’b11	Default		
		2’b10	+15mv		
		2’b01	-15mv		
		2’b00	reserved		
3:0	TXVREFTUNE	These bits control HS DC voltage level adjustment.		RW	
		4’b1111	+12.5%		
		4’b1110	+11.25%		
		4’b1101	+10%		
		4’b1100	+8.75%		

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		4'b1011	+7.5%		
		4'b1010	+6.255		
		4'b1001	+5%		
		4'b1000	+3.75%		
		4'b0111	+2.5%		
		4'b0110	+1.25%		
		4'b0101	Default		
		4'b0100	-1.25%		
		4'b0011	-2.5%		
		4'b0010	-3.75%		
		4'b0001	-5%		
		4'b0000	-6.25%		

11.2.4.19 USB Reset Detect Timer Register

USBRDT **0x10000040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					HB_MASK	VBFIL_LD_EN	IDDIG_EN	IDDIG_REG	USBRDT																						
RST	?	?	?	?	?	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26	HB_MASK	Halfword/Byte transfer support mask. 0: enable 1: mask	RW
25	VBFIL_LD_EN	VBUS filter data load enable.	RW
24	IDDIG_EN	This bit indicates using IDDIG_REG to control "iddig" signal.	RW
23	IDDIG_REG	This bit controls "iddig" when IDDIG_REG_EN = 1'b1.	RW
22:0	USBRDT	These bits control USB reset detect time.	RW

11.2.4.20 USB VBUS Jitter Filter Register

USBVBFIL **0x10000044**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDDIGFIL																USBVBFIL															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	IDDIGFIL	These bits controls iddig jitter filter time.	RW
15:0	USBVBFIL	These bits controls VBUS jitter filter time.	RW

11.2.4.21 USB Parameter Control Register1

The USBPCR1 is a 32-bit read/write register that allows software to control OTG PHY some functions. It is initialized to 0x00000004.

USBPCR1 **0x10000048**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									TXRISETUNE	UHC_pdbar	UHC_ibspot			UHC_xp	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	1	0	0

Bits	Name	Description	RW
6	TXRISETUNE	These bit adjust the rise/fall times of the HS waveform. 1'b0: default 1'b1: -8%	RW
5	UHC_pdbar	Power down Mode. Enables power down state. 0: power down 1: power on	RW
4:2	UHC_ibspot	Current option. 3'b000: 6u 3'b001: 5u (default) 3'b010: 4u	RW
1:0	UHC_xp	Cross-point control of DP, DM. 2'b0x: default cross-point: $V_{DD}/2$ 2'b11: cross-point up: $V_{DD}/2$ + 400mV 2'b10: cross-point down: $V_{DD}/2$ - 400mV	RW

11.2.4.22 PLL Control Register0

The PLL Control Register (CPPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x????0020 only by any reset. Only word access can be used on CPPCR.

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CPPCR 0x10000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BS	PLLM							Reserved	PLLN					PLLOD		LOCK0	Reserved				PLLS	PLLBP	PLLEN	PLLST							
RST	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31	BS	0: low band; 1: high band.	RW
30:24	PLLM	the PLL feedback 7-bit divider.	RW
23	Reserved	Writing has no effect, read as zero.	R
22:18	PLLN	the PLL input 5-bit divider.	RW
17:16	PLLOD	00: divide by 1 01: divide by 2 10: divide by 4 11: divide by 8	RW
15	LOCK0	0: the PLL output is stable 1: the PLL output is not stable Software should clear this bit to 0, when this bit equal to 1, it indicates that PLL hadn't stable previously , it is only used to debug.	RW
14:11	Reserved	Writing has no effect, read as zero.	R
10	PLLS	PLL Stabilize Flag. 0: PLL is off or not stable 1: PLL is on and stable	R
9	PLLBP	PLL Bypass. If PLLEN is 1, set this bit to1 will bypass PLL. The PLL is still running background but the source of associated dividers is switched to 12-M. If PLLEN is 0, set this bit to 1 has no effect. If PLLEN is 1, clear this bit to 0 will switch the source of associated dividers to PLL output.	RW
8	PLLEN	PLL Enable. When PLLEN is set to 1, PLL starts to lock phase. After PLL stabilizes, PLLS bit is set. If PLLBP is 0, the source of associated dividers, is switched to PLL output. When PLLEN is clear to 0, PLL is shut off and the source of associated dividers is switched to 12-MHz in spite of PLLBP bit.	RW
7:0	PLLST	PLL Stabilize Time. Specifies the PLL stabilize time by unit of RTCCLK (approximate 32kHz) cycles. It is used when change PLL multiplier or change PLL from off to on. It is initialized to H'20.	RW

11.2.4.23 PLL Control Register1

The PLL Control Register (CPPCR1) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x????0002 only by any reset. Only word access can be used on CPPCR1.

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CPPCR1 0x10000030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BS	PLL1M							Reserved	PLL1N					PLL1OD		P1SCS	Reserved		P1SDIV					PLL1EN	PLL1S	Reserved			LOCK1	PLL1OFF	PLL1ON
RST	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31	BS	0: low band 1: low band	RW
30:24	PLL1M	the PLL1 feedback 7-bit divider.	RW
23	Reserved	Writing has no effect, read as zero.	R
22:18	PLL1N	the PLL1 input 5-bit divider.	RW
17:16	PLL1OD	00: divide by 1 01: divide by 2 10: divide by 4 11: divide by 8	RW
15	P1SCS	0: select EXCLK as PLL1 input clock 1: select PLL0 divided clock as PLL1 input clock	RW
12:8	P1SDIV	PLL0 clock dividers as PLL1 input clock.	RW
8	Reserved	Writing has no effect, read as zero.	R
7	PLL1EN	PLL1 Enable. When PLL1EN is set to 1, PLL1 starts to lock phase. After PLL1 stabilizes, PLL1S bit is set. When PLL1EN is clear to 0, PLL1 is shut off.	RW
6	PLL1S	PLL1 Stabilize Flag. 0: PLL1 is off or not stable 1: PLL 1is on and stable	R
5:3	Reserved	Writing has no effect, read as zero.	R
2	LOCK1	0: the PLL output is stable 1: the PLL output is not stable Software should clear this bit to 0, when this bit equal to 1, it indicates that PLL hadn't stable previously , it is only used to debug.	RW
1	PLLOFF	0 : PLL1 doesn't enter shut off state 1: PLL1 is in shut off state	R
0	PLLON	0: PLL1 doesn't enter on state 1: PLL1 is in on state	R

11.2.4.24 PLL Switch and Status Register

The PLL Switch and Status Register (CPPSR) is a 32-bit read/write register, which controls the clock switch ,frequency change mode and reflect the PLL and clock switch Status .It is initialized to 0x80000000 by any reset. Only word access can be used on CPPSR.

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CPPSR **0x10000014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PLLOFF	PLLBP	PLLON	PS	FS	CS	Reserved																							SM	PM	FM
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PLLOFF	0 : PLL doesn't enter shut off state 1: PLL is in shut off state	R
30	PLLBP	0: PLL doesn't enter by pass state 1: PLL is in by pass state	R
29	PLLON	0: PLL doesn't enter on state 1: PLL is in on state	R
28	PS	0: disable PLL or no change PLL parameters 1: enable PLL or change PLL parameters have finished The bit is asserted to 1 auto by hardware . when software concerns this bit, at first software write 0 to the bit, then read the status bit until to 1.	RW
27	FS	Indicate the change frequency has finished . the bit only reflect CDIV, C1DIV, H0DIV, H1DIV, PDIV , H2DIV change. 0: no change 1: change clock parameters have finished when software concerns this bit, at first software write 0 to the bit, then read the status bit until to 1.	RW
26	CS	Indicate the clock switch has finished, the bit reflects when PLL switch to EXCLK or EXCLK to PLL. 0: no clock switch 1: clock switch has finished. when software concerns this bit, at first software write 0 to the bit, then read the status bit until to 1.	RW
25:3	Reserved	Writing has no effect, read as zero.	R
2	SM	0: hardware control 1: when frequency changes, above clocks are all stopped	RW
1	PM	Clock switch mode. When PLL switch to EXCLK or EXCLK switch to PLL. 0: slow mode 1: fast mode	RW
0	FM	Clock frequency change mode. Only to CDIV, C1DIV. 0: slow mode 1: fast mode	RW

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11.2.5 PLL Operation

The PLL developed as a macro cell for clock generator. It can generate a stable high-speed clock from a slower clock signal. The output frequency is adjustable and can be up to 1500MHz. The PLL integrates a phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and other associated support circuitry. All fundamental building blocks as well as fully programmable dividers are integrated on the core. It is useful for clock multiplication of stable crystal oscillator sources and for de-skew clock signals.

The PLL block diagram is shown in following figure:

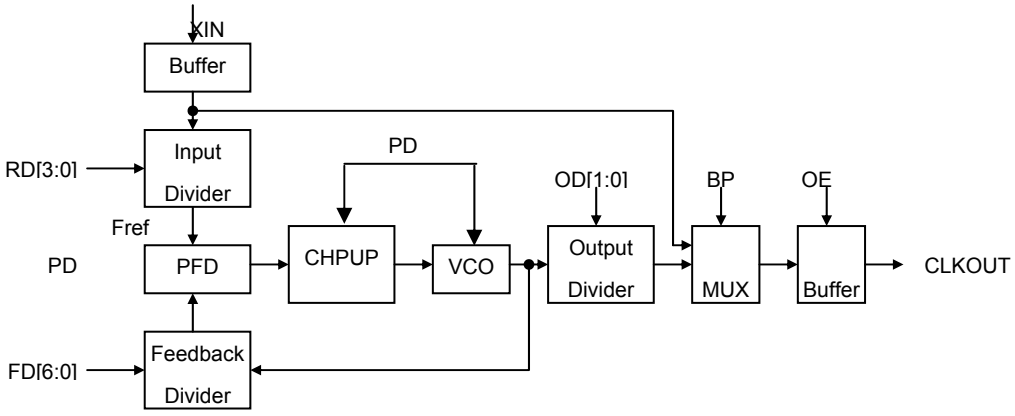


Figure 11-1 Block Diagram of PLL

11.2.5.1 PLL Configuration

PLL Divider Value Setting

There are 3 divider values (N, M and NO) to set the PLL output clock frequency CLKOUT:

1 Input Divider Value N.

N = PLLN of CPPCR

2 Feedback Divider Value M.

M = PLLM of CPPCR

3 Output Divider Value NO.

Output Divider Setting (OD)	Output Divider Value (NO)
0	1
1	2
2	4
3	8

4 The PLL output frequency, FOUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency FOUT is calculated from the

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following equations:

NF = 1+ M0 + M1*2 + M2*4 + M3*8 + M4*16 + M5*32 + M6*64

NR = 1+ N0*1 + N1*2 + N2*4 + N3*8 + N4*16

NO = 2od0+2od1

FREF = FIN / NR

FVCO = FOUT * NO

FOUT = FIN * NF / (NR*NO), where FREF is the comparison frequency for the PFD.

For proper operation in normal mode, the following constraints must be satisfied:

For high-band,

10 MHz ≤ FREF ≤ 50 MHz

500 MHz ≤ FVCO ≤ 1000 MHz

62.5 MHz ≤ FOUT ≤ 1000 MHz

For low-band:

10 MHz ≤ FREF ≤ 50 MHz

300 MHz ≤ FVCO ≤ 600 MHz

37.5 MHz ≤ FOUT ≤ 600 MHz

Electrical Characteristics

Junction Temperature = -40 - 125°C, Operating Voltage = typical ± 10% (unless specified otherwise)

PARAMETER	SYM	CONDITION		MIN	TYP	MAX	UNIT
Comparison Frequency	F_{REF}	$F_{REF} = F_{IN} / NR$ [1]		10	--	50	MHz
Input Clock Frequency [2]	F_{IN}	$F_{IN} = NR * F_{REF}$		10	--	400	MHz
Output Clock Frequency	F_{OUT}	$F_{OUT} = F_{VCO} / NO$ [1]	High-band	62.5	--	1000	MHz
			Low-band	37.5		600	
VCO Operating Range	F_{VCO}	$F_{VCO} = F_{REF} * NF$ [1]	High-band	500	--	1000	MHz
			Low-band	300		600	

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PARAMETER	SYM	CONDITION			MIN	TYP	MAX	UNIT
Period Jitter (pk-pk) [3, 4]	--	Clean Power	High-band	OD=0	--	--	3.50	% UI
				OD=1			2.00	
				OD=2			1.35	
				OD=3			0.75	
			Low-band	OD=0	--	--	2.35	% UI
				OD=1			1.50	
				OD=2			1.00	
				OD=3			0.65	
Cycle-to-Cycle Jitter (max) [3, 4]	--	Clean Power	High-band	OD=0	--	--	3.20	% UI
				OD=1			2.00	
				OD=2			1.30	
				OD=3			0.65	
			Low -band	OD=0	--	--	2.10	% UI
				OD=1			1.40	
				OD=2			1.00	
				OD=3			0.55	
Long-term Jitter (pk-pk) [3, 4]	--	Clean Power / 1024-cycle Delay	High-band	OD=0	--	--	490	ps
				OD=1			525	
				OD=2			560	
				OD=3			565	
			Low -band	OD=0	--	--	615	
				OD=1			600	
				OD=2			710	
				OD=3			770	
TIE (Time Interval Error) Jitter (rms) [3, 4]	--	Clean Power	High-band	OD=0	--	--	3.00	% UI
				OD=1			1.41	
				OD=2			0.70	
				OD=3			0.36	
			Low -band	OD=0	--	--	2.10	
				OD=1			1.03	
				OD=2			0.52	
				OD=3			0.26	

11.2.6 Implementing the Dividers

In Normal Mode, in order for the PLL to function properly, it is necessary to set suitable integer values for the dividers (NR for the input divider, NF for the feedback divider and NO for the output divider). The divider values are set using digital binary inputs of R[4:0], F[6:0] and OD[1:0].

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1 Input Divider Value (**NR**).
NR = 16*R4 + 8*R3 + 4*R2 + 2*R1+ R0 + 1 = R[4:0] + 1

2 Feedback Divider Value (**NF**).
NF = 64*F6 + 32*F5 + 16*F4 + 8*F3+ 4*F2 + 2*F1 + F0 + 1 = F[6:0] + 1

3 Output Divider Value (**NO**).

OD[1:0]	0	1	2	3
NO	1	2	4	8

11.2.7 Programming the Output Clock Frequency

FREF = FIN / NR
FVCO = FOUT * NO
FOUT = FIN * NF / (NR*NO), where FREF is the comparison frequency for the PFD.

For proper operation in normal mode, the following constraints must be satisfied:

For high-band,
10 MHz ≤ FREF ≤ 50 MHz
500 MHz ≤ FVCO ≤ 1000 MHz
62.5 MHz ≤ FOUT ≤ 1000 MHz

For low-band:
10 MHz ≤ FREF ≤ 50 MHz
300 MHz ≤ FVCO ≤ 600 MHz
37.5 MHz ≤ FOUT ≤ 600 MHz

Example I: To synthesize a 800 MHz output clock in high-band with an input frequency FIN = 100 MHz.

1 Set normal mode operation in high-band.
PD = 0, BP = 0, BS = 1.

2 Set NR to obtain FREF within the PFD comparison frequency range.
Let FREF = 25 MHz;
Since FREF = FIN / NR,
NR = FIN / FREF = 100 MHz / 25 MHz = 4;
R[4:0] = NR – 1 = 3 = 000112.

3 Set NO and ensure FVCO within the VCO operating range.
Set NO = 1;
FVCO = FOUT * NO;
FVCO = 800 MHz * 1 -> within the VCO operating range in high-band;
-> OD[1:0] = 0 = 002.

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4 Set NF to obtain the FOUT frequency.
NF = FOUT * NR * NO / FIN;
NF = 800 MHz * 4 * 1 / 100 MHz = 32;
-> F[6:0] = NF – 1 = 31 = 00111112.

Example II: To synthesize a 500 MHz output clock withan input frequency FIN = 100 MHz. Choose low-band for a better jitter performance.

1 Set normal mode operation in low-band.
PD = 0, BP = 0, BS = 0.

2 Set NR to obtain FREF within the PFD comparison frequency range.
Let FREF = 25 MHz;
Since FREF = FIN / NR,
NR = FIN / FREF = 100 MHz / 25 MHz = 4;
-> R[4:0] = NR – 1 = 3 = 000112.

3 Set NO and ensure FVCO within the VCO operating range.
Set NO = 1;
FVCO = FOUT * NO;
FVCO = 500 MHz * 1 □ within the VCO operating range in low-band;
-> OD[1:0] = 0 = 002.

4 Set NF to obtain the FOUT frequency.
NF = FOUT * NR * NO / FIN;
NF = 500 MHz * 4 *1 / 100 MHz = 20;
-> F[6:0] = NF – 1 = 19 = 00100112.

11.2.8 Main Clock Division Change Sequence

Main clock (CCLK, AUX_CLK, H0CLK, PCLK, H1CLK, H2CLK) frequencies can be changed separately or simultaneously by changing division ratio. Following conditions must be obeyed:

1 CCLK must be integral multiple of H0CLK, H1CLK, H2CLK.
2 AUX_CCLK must be CCLK/2 or equal to H1CLK.
3 H0CLK must be equal to H2CLK or twice of H2CLK.
4 H2CLK must be equal to PCLK or twice of PCLK.
5 H1CLK must be equal to H0CLK or twice of H0CLK.

Don’t violate this limitation, otherwise unpredictable error may occur.

In normal mode, if CE bit of CPCCR is 1, changing CDIV, C1DIV, H0DIV, H2DIV, PDIV ,H1DIV, BCHCDR(BCHM=0) will start a Division Change Sequence immediately. If CE bit of CPCCR is 0, changing above all will not start Division Change Sequence.

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11.2.9 Change Other Clock Frequencies

The divider of LCD pixel clock (LPCLK), I2S device clock, SSI device clock, MSC device clock ,USB clock, UHC clock, PCM clock, GPS , BCH and GPU clock can be changed by programming LPCDR , I2SCDR, SSICDR, MSCCDR , USBCDR, UHCCDR, PCMCDR, GPSCDR, BCHCDR(BCHM=1) and GPUCDR respectively.

Change LPCDR I2SCDR SSICDR MSCCDR , USBCDR, UHCCDR, PCMCDR, GPSCDR, BCHCDR(BCHM=1), GPUCDR as following steps:

1 Stop related devices with clock-gate function. Clock supplies to the devices are stopped.
2 Change LPCDR, I2SCDR, SSICDR, MSCCDR, USBCDR, UHCCDR, PCMCDR, GPSCDR, BCHCDR, GPUCDR . If CE is 1, clock frequencies are changed immediately. If CE is 0, clock frequencies are not changed until PLL Multiplier Change Sequence is started.
3 Cancel above clock-gate function.

11.2.10 Change Clock Source Selection

USB, I2S device clocks, PCM device clock, LCD pix clock , MSC clock and SSI clock can be selected from two sources. Before change clock source, corresponding devices should be stopped using clock-gate function.

1 When USB clock source is changed (UCS bit of USBCDR), USB clock should be stopped.
2 When UHC clock source is changed (UHPCS, UHCS bit of UHCCDR), UHC should be stopped.
3 When I2S clock source is changed (I2CS bit of CPCCR), AIC should be stopped.
4 When LCD pix clock source is changed (LSCS LTCS bit of LPCDR), LCD should be stopped.
5 When MSC clock source is changed (MPCS of MSCCDR), MSC should be stopped.
6 When SSI clock source is changed (SCS ,SPCS of SSICDR), SSI should be stopped.
7 When BCH clock source is changed (BPCS of BCHCDR), BCH should be stopped.

When UCS, I2CS , LSCS, LTCS, MCS, SCS, BPCS(BCHM=1) bit is changed, clock source is changed immediately.

When PCS of CPPCR is changed, the corresponding module clock should be stopped.

When P1SCS of CPPCR1 or P1SDIV is changed, the corresponding module should be stopped.

11.2.11 Two PLL Source Selection

USB, I2S, PCM, GPS, GPU, LCD, UHC, MSC, SSI, BCH, CIM source clock can be selected from PLL0 or PLL1. Before change clock source, corresponding devices should be stooped using clock-gate function.

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11.2.12 EXCLK Oscillator

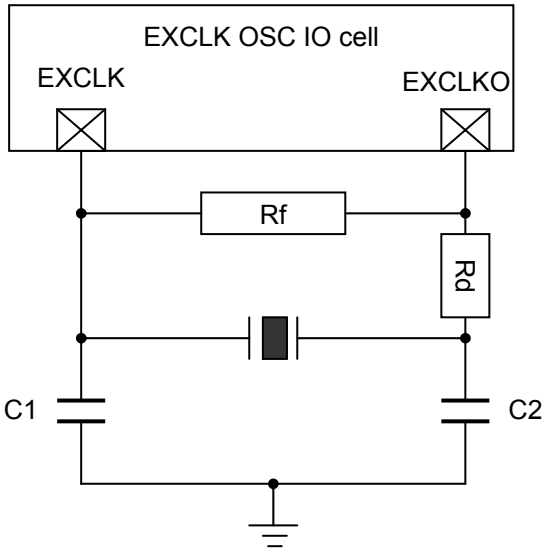


Figure 11-2 Oscillating circuit for fundamental mode

To turn on the oscillator, the oscillating circuit must provide the negative resistance (-Re) at least five times the equivalent series resistance (ESR) of the crystal sample. For larger -Re value, faster turn on the crystal. Higher gm provides larger -Re therefore can start-up the crystal with higher ESR for the same load capacitance (CL). However, it's required higher power consumption.

There are two key parameters to turn on oscillator. Which are CL and the maximum ESR at the target frequency? By reducing the CL, the -Re can be increased thus; shorter turn on time can be achieved. However, if CL is too small, the deviation from the target frequency will increase because of the capacitance variation. So, a trade-off relationship between short turn on time and small frequency deviation in deciding CL value. The smaller ESR of the crystal sample will reduce turn on time but the price is higher. The typical CL and ESR values for difference target frequencies are listed in Table 11-2.

Table 11-2 Typical CL and the corresponding maximum ESR

Target Frequency (Hz)	2M ~ 3M	3M ~ 6M	6M ~ 10M	10M ~ 20M
CL (pf)	25	20	16	12
Maximum ESR (ohm)	1K	400	100	80

Figure 11-2 shows the oscillating circuit is connected with the oscillator I/O cell. Components feedback resistor (Rf), damping resistor (Rd), C1 and C2 are used to adjust the turn on time, keep stability and accurate of the oscillator.

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Rf is used to bias the inverter in the high gain region. It cannot be too low or the loop may not oscillate. For mega Hertz range applications, Rf of 1Mohm is applied.
Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Re of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.

C1 and C2 are deciding regard to the crystal or resonator CL specification. In the steady state of oscillating, CL is defined as (C1*C2)/(C1+C2). Actually, the I/O ports, bond pad, and package pin all contribute the parasitic capacitance to C1 and C2. Thus, CL can be rewrite to (C1'*C2')/(C1'+C2'), where C1'=(C1+Cin,stray) and C2'=(C2+Cout,stray). In this case, the required C1 and C2 will be reduced.

Notice, this oscillating circuit is for parallel resonate but not series resonate. Because C1, C2, Rd and Rf are varying with the crystal specifications; therefore there is no single magic number of all the applications.

11.3 Power Manager

In the Low-Power mode, part or whole processor is halted. This will reduce power consumption. The Power Management Controller contains low-power mode control and reset sequence control.

11.3.1 Low-Power Modes and Function

The processor supports six low-power modes and function:

- NORMAL mode
  In Normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate completely. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

- DOZE mode
  DOZE mode is entered by setting DOZE bit of LCR to 1. In DOZE mode, clock is burst to CPU core and the clock duty is set by DUTY field of LCR. DOZE mode is canceled by reset, interrupt or clearing DOZE bit to 0. Continuous clock is supplied immediately after DOZE mode is canceled. The other Clocks except CCLK run continuously in DOZE mode.

- IDLE mode
  In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, the any interrupts should be activated.

- SLEEP mode
  In SLEEP mode, all clocks except RTC clock are disabled. PLL is disabled also. SLEEP

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mode is canceled by reset or interrupt. When SLEEP mode is canceled, PLL is restarted , the PLL needs clock stabilization time (PLL lock time). This PLL stabilization time is automatically inserted by the internal logic with lock time count register. and all clocks start operating after PLL stability time.

- CLOCK GATE function
  CLOCK GATE function is used to gate specified on-chip module when it is not used. Set specified CLKG0~40 bits in CLKGR will enter specified CLK gate function. CLOCK gate function is canceled by reset or clearing specified CLKGR0~40 to 0.

- Power down Mode
  In order to reduce power leakage, software may shut down power supply for AHB1 and GPS module. When system enters into SLEEP mode, the software may shut down power for J1 according to OPCR.PD bit.

11.3.2 Register Description

All PMC register 32bit access address is physical address.

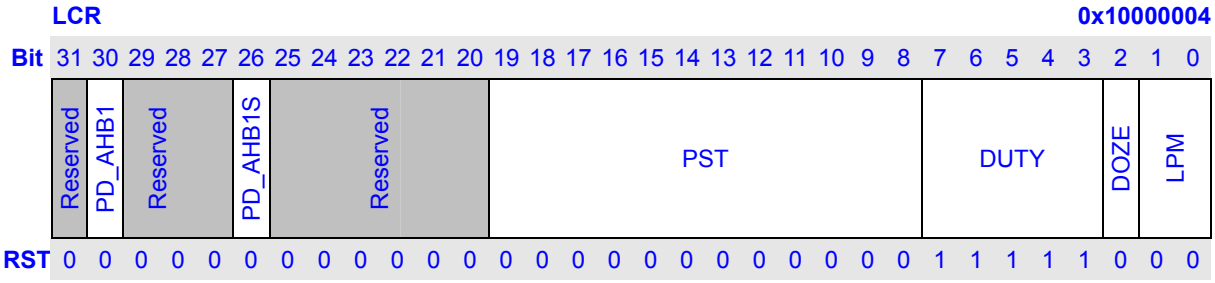
Table 11-3 Power/Reset Management Controller Registers Configuration

Name	description	RW	Initial Value	Address	Access Size
LCR	Low Power Control Register	RW	0x000000F8	0x10000004	32
PSWC0ST	Power Switch Chain0 Start Time	RW	0x00000000	0x10000090	32
PSWC1ST	Power Switch Chain1 Start Time	RW	0x00000000	0x10000094	32
PSWC2ST	Power Switch Chain2 Start Time	RW	0x00000000	0x10000098	32
PSWC3ST	Power Switch Chain3 Start Time	RW	0x00000000	0x1000009c	32
CLKGR0	Clock Gate Register0	RW	0x3FFFFFE0	0x10000020	32
OPCR	Oscillator and Power Control Register	RW	0x00001570	0x10000024	32
CLKGR1	Clock Gate Register1	RW	0x0000017F	0x10000028	32

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11.3.2.1 Low Power Control Register

The Low Power Control Register (LCR) is a 32-bit read/write register that controls low-power mode status. It is initialized to 0x000000F8 by any reset.



Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	PD_AHB1	Power Down Module AHB1. 0: not shut down power supply to AHB1 1: shut down power supply to AHB1	RW
29:27	Reserved	Writing has no effect, read as zero.	R
26	PD_AHB1S	AHB1 power down status. 0: AHB1 module not shut down 1: AHB1 module has entered shut down mode	R
25:20	Reserved	Writing has no effect, read as zero.	R
19:8	PST	Power stability Time. Specifies the Power stabilize time by unit of RTCCLK (approximate 32kHz) cycles.	RW
7:3	DUTY	CPU Clock Duty. Control the CPU clock duty in doze mode. When the DUTY field is 0x1F, the clock is always on and when it is zero, the clock is always off. Set the DUTY field to 0 when the CPU will be disabled for an extended amount of time. 00000: 0/31 duty-cycle 00001: 1/31 duty-cycle 00010: 2/31 duty-cycle … 11111: 31/31 duty-cycle	RW
2	DOZE	Doze Mode. Control the doze mode. When doze mode is canceled, this bit is cleared to 0 automatically. 0: Doze mode is off; 1: Doze mode is on.	RW
1:0	LPM	Low Power Mode. Specifies which low-power mode will be entered when SLEEP instruction is executed. Bit 1~0: **00**: IDLE mode will be entered when SLEEP instruction is executed **01**: SLEEP mode will be entered when SLEEP instruction is executed	RW

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		10: Reserved **11**: Reserved	

11.3.2.2 Power Switch Chain0 Start Time Register

PSWC0ST **0x10000090**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC0ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.3.2.3 Power Switch Chain1 Start Time Register

PSWC1ST **0x10000094**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC1ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.3.2.4 Power Switch Chain2 Start Time Register

PSWC2ST **0x10000098**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC2ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.3.2.5 Power Switch Chain3 Start Time Register

PSWC3ST **0x1000009C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC3ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The Start Time by the unit of PCLK cycles.

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11.3.2.6 Clock Gate Register0

The Clock Gate Register (CLKGR0) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x2FFFFFE0.

CLKGR																														0x10000020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKGR0																															
RST	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:0	CLKGR0	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also.	RW

Bit	Module	Description
31	AHB_MON	After reset period, the clock is not stopped.
30	DDR	After reset period, the clock is not stopped.
29	IPU	After reset period, the clock is stopped.
28	LCD	After reset period, the clock is not stopped.
27	TVE	After reset period, the clock is stopped.
26	CIM	After reset period, the clock is stopped.
25	MDMA	After reset period, the clock is stopped.
24	UHC	After reset period, the clock is stopped.
23	MAC	After reset period, the clock is stopped.
22	GPS	After reset period, the clock is stopped.
21	DMAC	After reset period, the clock is stopped.
20	SSI2	After reset period, the clock is stopped.
19	SSI1	After reset period, the clock is stopped.
18	UART3	After reset period, the clock is stopped.
17	UART2	After reset period, the clock is stopped.
16	UART1	After reset period, the clock is stopped.
15	UART0	After reset period, the clock is stopped.
14	SADC	After reset period, the clock is stopped.
13	KBC	After reset period, the clock is stopped.
12	MSC2	After reset period, the clock is stopped.
11	MSC1	After reset period, the clock is stopped.
10	OWI	After reset period, the clock is stopped.
9	TSSI	After reset period, the clock is stopped.
8	AIC	After reset period, the clock is stopped.
7	SCC	After reset period, the clock is stopped.
6	I2C1	After reset period, the clock is stopped.
5	I2C0	After reset period, the clock is stopped.

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		4	SSI0	After reset period, the clock is not stopped.	
		3	MSC0	After reset period, the clock is not stopped.	
		2	OTG	After reset period, the clock is not stopped.	
		1	BCH	After reset period, the clock is not stopped.	
		0	NEMC	After reset period, the clock is not stopped.	

11.3.2.7 Clock Gate Regiater1

The Clock Gate Register (CLKGR1) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x00000FFFF.

CLKGR1 **0x10000028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CLKGR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

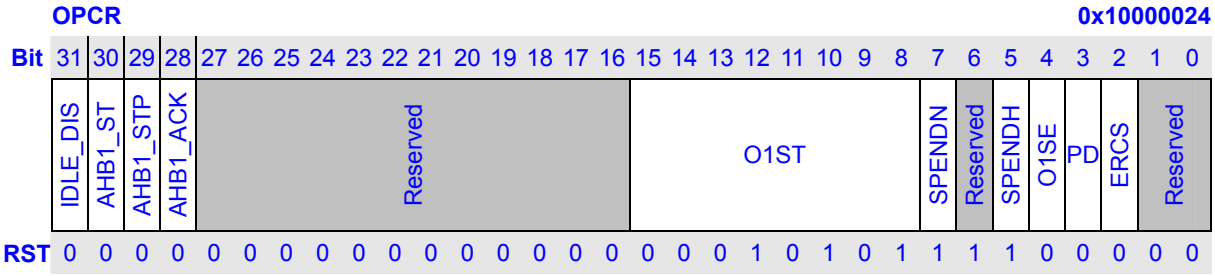
Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
8:0	CLKGR1	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also.	

Bit	Module	Description
15	I2C2	After reset period, the clock is stopped.
14	AUX	After reset period, the clock is stopped.
13	I2S2CH	After reset period, the clock is stopped.
12	OSD	After reset period, the clock is stopped.
11	UART4	After reset period, the clock is stopped.
10	PCM1	After reset period, the clock is stopped.
9	GPU	After reset period, the clock is stopped.
8	PCM0	After reset period, the clock is stopped.
7	VPU	After reset period, the clock is stopped.
6	CABAC	After reset period, the clock is stopped.
5	SRAM	After reset period, the clock is stopped.
4	DCT	After reset period, the clock is stopped.
3	ME	After reset period, the clock is stopped.
2	DBLK	After reset period, the clock is stopped.
1	MC	After reset period, the clock is stopped.
0	BDMA	After reset period, the clock is stopped.

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11.3.2.8 Oscillator and Power Control Register (OPCR)

The Oscillator and Power Control Register is a 32-bit read/write register that specifies some special controls to oscillator and analog block. It is initialized to 0x00001570 by reset.



Bits	Name	Description	RW
31	IDLE_DIS	0: when CPU enters idle mode, CPUI clock is stopped 1: When CPU enters idle mode, CPUI clock is not stopped	RW
30	AHB1_ST	0: AHB1 does not enter soft reset mode 1: AHB1 enters soft reset mode	RW
29	AHB1_STP	Request for AHB1 to Stop bus transfer.	RW
28	AHB1_ACK	AHB1 Stop Ack.	R
27:16	Reserved	Writing has no effect, read as zero.	R
15:8	O1ST	EXCLK Oscillator Stabilize Time. This filed specifies the EXCLKoscillator stabilize time by unit of 16 RTCCLK periods (oscillator stable time O1ST × 16 / 32768) cycles. It is initialized to H'15.	RW
7	SPENDN	force OTG phy to enter suspend mode. 0: OTG phy has forced to entered SUSPEND mode 1: OTG phy hasn't forced to entered SUSPEND mode	R
6	Reserved	Writing has no effect, read as zero.	R
5	SPENDH	Force UHC phy to enter suspend mode. 0: UHC phy hasn't forced to entered SUSPEND mode 1: UHC phy has forced to entered SUSPEND mode	RW
4	O1SE	EXCLK Oscillator Sleep Mode Enable. This filed controls the state of the EXCLK oscillator in Sleep mode. 0: EXCLK oscillator is disabled in Sleep mode 1: EXCLK oscillator is enabled in Sleep mode	RW
3	PD	The fief controls the state P0 in Sleep mode. 0: The P0 not power down in Sleep mode 1: The P0 power down in Sleep mode	RW
2	ERCS	EXCLK/512 clock and RTCLK clock selection. 0: select EXCLK/512 division ration clock 1: select RTCLK clock the clock only output to CPM INTC SSI TCU etc.	RW
1:0	Reserved	Writing has no effect, read as zero.	R

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11.3.3 Doze Mode

Firstly, software should set the DUTY bits of LCR. Then set DOZE bit of LCR to 1 to enter doze mode. When slot controller of PMC indicates that the CPU clock's time-slot has expired, CPU is halted but its register contents are retained. During doze mode, program can modify clock duty-cycle according to core resource requirement. Clock control is in increments of approximately 3% (1/31).

Doze is exited by software, interrupt, reset or SLEEP instruction.

11.3.4 IDLE Mode

In normal mode, when LPM bits in LCR are 0 and SLEEP instruction is executed, the processor enters idle mode. CPU is halted but its register contents are retained All critical application must be finished and peripherals must be configured to generate interrupts when they need CPU attention.

The procedure of entering sleep mode is shown blow:

1 Set LPM bits in LCR to 0.
2 Executes SLEEP instruction.
3 When current operation of CPU core has finished and CPU core is idle, CCLK supply to CPU core is stopped.

IDLE mode is exited by an interrupt (IRQ or on-chip devices) or a reset.

11.3.5 SLEEP Mode

In normal mode, when LPM bits in LCR is 1 and SLEEP instruction is executed, the processor enter SLEEP mode. CPU and on-chip devices are halted, except some wakeup-logic. PLL is shut off. Clock output from CKO pin is also stopped. SDRAM content is preserved by driving into self-refresh state. CPU registers and on-chip devices registers contents are retained.

Before enter SLEEP mode, software should ensure that all peripherals are not running. The procedure of entering SLEEP mode is shown blow:

1 Set LPM bit in LCR to 1.
2 Execute a SLEEP instruction.
3 When current access on system bus complete, the arbiter will not grant any following request. EMC will drive SDRAM from auto-refresh mode to self-refresh mode.
4 When system bus is idle state and SDRAM is self-refresh mode, internal clock supplies are stopped.
5 SLEEP mode can be exited by an interrupt (IRQ or on-chip devices), WDT reset or a poweron reset via the RESETP pin.

11.3.6 Power Down Mode

When PD_AHB1/PD_GPS bit in LCR is 1 , the processor enters shut down AHB1/GPS module power sequence.

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When PD_AHB1S/PD_GPSS bit in LCR is 1, it indicates that the AHB1/GPS module has been shut off. The leakage current of AHB1/GPS is reduced almost to 0.

When enter sleep mode, when PD bits in OPCR is 1, the J1 power supply would be shut off. The leakage current of J1 is reduced almost to 0.

The procedure of entering Power Down mode is shown blow:

1 set proper values for PSWC0ST, PSWC1ST, PSWC2ST, PSWC3ST.
2 set PD_AHB1/PD_GPS bit in LCR to 1.
3 wait until PD_AHB1S/PD_GPSS = 1.
4 When need for supply power for AHB1/GPS, set PD_AHB1/PD_GPS in LCR to 0.
5 wait until PD_AHB1S/PD_GPSS = 0.
6 the hardware auto generate RESET signal to the module, the software must again config the module as the same to POWER ON Reset.

11.4 Reset Control Module

11.4.1 Register Description

All RCM register 32bit access address is physical address.

Name	description	RW	Initial Value	Address	Access Size
RSR	Reset Status Register	RW	0x????????	0x10000008	32

11.4.1.1 Reset Status Register (RSR)

The Reset Status Register (RSR) is a 32-bit read/write register which records last cause of reset. Each RSR bit is set by a different source of reset. Please refer to Reset Sequence Control for reset sources description.

RSR 0x10000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													P0R	WR	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
2	P0R	P0 power up Reset. It indicates that P0 has been shut down, now it has been power up. When P0 reset is detected, P0R is set and remains set until software clears it or another reset occurs. This bit can only be written	RW

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		with 0. Write with 1 will be ignored. 0: P0 reset has not occurred since the last time the software clears this bit 1: P0 reset has occurred since the last time the software clears this bit	
1	WR	WDT Reset. When a WDT reset is detected, WR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: WDT reset has not occurred since the last time the software clears this bit 1: WDT reset has occurred since the last time the software clears this bit	RW
0	PR	Power On Reset. When a poweron reset via PRESET pin is detected, PR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored. 0: Power on reset has not occurred since the last time the software clears this bit 1: Power on reset has occurred since the last time the software clears this bit	RW

11.4.2 Power On Reset

Power on reset is generated when PRESET pin is driven to low. Internal reset is asserted immediately. All pins return to their reset states. The Power on reset is extended to 40MS.

PRESET pin must be held low until power stabilizes and the EXCLK oscillator stabilize. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state. All internal modules are initialized to their predefined reset states.

11.4.3 WDT Reset

WDT reset is generated when WDT overflow. Internal reset is asserted within two RTCCLK cycles. All pins return to their reset states.

Then WDT reset source is cleared because of internal reset. The internal reset is asserted for about 10 milliseconds. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state.

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12 Real Time Clock

12.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, the real time and alarm logic, and the power down and wakeup control logic.

12.1.1 Features

RTC module has following features:

- Embedded 32768Hz oscillator for 32k clock generation with an external 32k crystal
- RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- Alarm wakeup
- External pin wakeup with up to 2s glitch filter

12.1.2 Signal Descriptions

RTC has 5 signal IO pins and 1 power pin. They are listed and described in.

Pin Names	Pin Loc	IO	IO Cell Char.	Pin Description	Power
RTCLK		AI	32768Hz	RTCLK: 32768 clock input or OSC input	VDD_{RTC}
RTCLKO		AO		RTCLKO: OSC output	VDD_{RTC}
PWRON		AO	~2mA, Open-Draw	PWRON: Power on/off control of main power	VDD_{RTC}
WKUP_		AI	Schmitt	WKUP_: Wake signal after main power down	VDD_{RTC}
PPRST_		AI	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC		P		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

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RTCLK/RTCLKO pins. We have an embedded oscillator for 32768Hz crystal. These two pins are the crystal XTALI and XTALO connection pins. If an input clock is used instead, please input it to RTCLK pin.

If do not use any clock, hibernate mode will be NOT available any more, and the time will lose if power down.

PWRON pin: this pin is used to control the main power on/off. Output high voltage means on and 0 means off.

WKUP_ pin: hibernating mode wakeup input. (Default low active)

PPRST_ pin: This pin should be set to low voltage only in two cases.

- When RTC power is turned on. (so that whole chip is power on)
- A RESET-KEY is pressed.

12.2 Register Description

Table 12-1 Registers for real time clock

Name	Description	RW	Reset Value	Address	Access Size
RTCCR	RTC Control Register	RW	0x00000081*1*2	0x10003000	32
RTCSR	RTC Second Register	RW	0x????????	0x10003004	32
RTCSAR	RTC Second Alarm Register	RW	0x????????	0x10003008	32
RTCGR	RTC Regulator Register	RW	0x0???????	0x1000300C	32

NOTES:

1 *1: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

2 *2: The reset value can be either of 0x00000081, 0x00000091, 0x00000089, 0x00000099.

Table 12-2 Registers for hibernating mode

Name	Description	RW	Reset Value	Address	Access Size
HCR	Hibernate Control Register	RW	0x00000000*1	0x10003020	32
HWFCR	Wakeup filter counter Register in Hibernate mode	RW	0x0000???0	0x10003024	32
HRCR	Hibernate reset counter Register in Hibernate mode	RW	0x00000??0	0x10003028	32
HWCR	Wakeup control Register in Hibernate mode	RW	0x00000008*1	0x1000302C	32
HWRSR	Wakeup Status Register in Hibernate mode	RW	0x00000000*1	0x10003030	32
HSPR	Scratch pattern register	RW	0x????????	0x10003034	32

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WENR	Write enable pattern register	RW	0x00000000	0x1000303C	32
CKPCR	Write enable pattern register	RW	0x00000010	0x10003040	32
PMCR	Write enable pattern register	RW	0x00000000	0x10003044	32

NOTE:

*[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

All these registers, include those for real time clock and for hibernating mode control, except otherwise stated, are implemented in RTCLK clock domain. When write to these registers, it needs about 1 ~ 2 RTCLK cycles to actually change the register's value and needs another RTCLK cycle to allow the next write access. A bit RTCCR.WRDY is used to indicate it. When RCR.WRDY is 1, it means the previous write is finished, a right value can be read from the target register, and a new write access can be issued. So before any write access, please make sure RCR.WRDY = 1.

12.2.1 RTC Control Register (RTCCR)

RTCCR contains bits to configure the real time clock features. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

RTCCR **0x10003000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WRDY	1HZ	1HZIE	AF	AIE	AE	SELEXC	RTCE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1*[1]	0	0*[1]	?	0	?	0*[1]	1

NOTE:

*[1]: These bits are reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
7	WRDY	Write ready flag. It is 0 when a write is currently processing and the value has not been written to the writing target register. No write to any RTC registers can be issued in this case, or the result is undefined. The read value from the target register is also undefined. The reading is meaningful and another write can be issued when it is 1. Please reference to descriptions in 12.2 for some more details. This bit is read only and write to it is ignored.	R
6	1HZ	1Hz flag. This bit is set by hardware once every 1 second through the 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored.	RW
5	1HZIE	1Hz interrupt enable. Writing to this bit takes effect immediately without	RW

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<table>
<tr><td></td><td></td><td>delay.<table><tr><th>1HZIE</th><th>Description</th></tr><tr><td>0</td><td>1Hz interrupt is disabled.</td></tr><tr><td>1</td><td>1Hz interrupt is enabled. RTC issues interrupt when 1HZ bit is set.</td></tr></table></td><td></td></tr>
<tr><td>4</td><td>AF</td><td>Alarm flag. This bit is set by hardware when alarm match (RTCSR = RTCSAR) is found and alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect immediately.</td><td>RW</td></tr>
<tr><td>3</td><td>AIE</td><td>Alarm interrupt enable.<table><tr><th>AIE</th><th>Description</th></tr><tr><td>0</td><td>Alarm interrupt is disabled.</td></tr><tr><td>1</td><td>Alarm interrupt is enabled. RTC issues interrupt when AF is set.</td></tr></table></td><td>RW</td></tr>
<tr><td>2</td><td>AE</td><td>Alarm enable.<table><tr><th>AE</th><th>Description</th></tr><tr><td>0</td><td>Alarm function is disabled.</td></tr><tr><td>1</td><td>Alarm function is enabled.</td></tr></table></td><td>RW</td></tr>
<tr><td>1</td><td>SELEXC</td><td>The divided EXCLK is selected as RTCLK in rtc-hiber module.<table><tr><th>SELEXC</th><th>Description</th></tr><tr><td>0</td><td>OSC32K or RTCLK input clock is selected as RTCLK in rtc-hiber module.</td></tr><tr><td>1</td><td>The divided EXCLK is selected as RTCLK in rtc-hiber module.</td></tr></table>NOTE: If do not use any 32Khz clock (either input clock or using crystal), hibernate mode will be NOT available any more, and the time will lose if power down.
CPM.OPCR.ERCS must be 0, when using SELEXC = 1.
When the main chip power down, SELEXC will be 0 in internal circuit, in this time, RTCLK will use OSC32K clock.</td><td>RW</td></tr>
<tr><td>0</td><td>RTCE</td><td>Real time clock enable.<table><tr><th>RTCE</th><th>Description</th></tr><tr><td>0</td><td>Real time clock function is disabled.</td></tr><tr><td>1</td><td>Real time clock function is enabled.</td></tr></table></td><td>RW</td></tr>
</table>

12.2.2 RTC Second Register (RTCSR)

RTCSR is a 32-bit width second counter. It can be read and write by software. It is increased by 1 at every 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). When read, it should be read continued more than once and take the value if the adjacent results are the same. RTCSR is not initialized by any reset.

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RTCSR																															0x10003004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

12.2.3 RTC Second Alarm Register (RTCSAR)

RTCSAR serves as a second alarm register. Alarm flag (RTCCR.AF) is set to 1 when the RTCSR equals the RTCSAR in the condition of alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). RTCSAR can be read and write by software and is not initialized by any reset.

RTCSAR																															0x10003008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSAR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

12.2.4 RTC Regulator Register (RTCGR)

RTCGR is serves as the real time clock regulator, which is used to adjust the interval of the 1Hz pulse.

RTCGR																															0x1000300C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK	Reserved					ADJC										NC1HZ															
RST	0*[1]	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

NOTE:

*[1]: This bit is reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31	LOCK	Lock bit. This bit is used to safeguard the validity of the data written into the RTCGR register. Once it is set, write to RTCGR is ignored. This bit can only be set by software and cleared by (any type of) resets. LOCK: 0 — Write to RTCGR is allowed. LOCK: 1 — Write to RTCGR is forbidden.	RW
30:26	Reserved	Writing has no effect, read as zero.	R
25:16	ADJC	This field specifies how many times it needs to add one 32kHz cycle for	RW

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		the 1Hz pulse interval in every 1024 1Hz pulses. In other word, among every 1024 1Hz pulses, ADJC number of them are trigged in every (NC1HZ + 2) 32kHz clock cycles, (1024 – ADJC) number of them are trigged in every (NC1HZ + 1) 32kHz clock cycles.	
15:0	NC1HZ	This field specifies the number plus 1 of the working 32kHz clock cycles are contained in the 1Hz pulse interval. In other word, 1Hz pulse is trigged every (NC1HZ + 1) 32kHz clock cycles, if RTCGR.ADJC = 0.	RW

12.2.5 Hibernate Control Register (HCR)

HCR contains the bit to control the main chip power on/off.

HCR **0x10003020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															PD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	PD	Power down or power on bit. Besides writing by CPU, this bit will be set to 1 if an unknown reason main power supply off is detected. This bit controls the PWRON pin level. When co-working with some external components, this bit is used for power management of this chip. It is supposed when 1 is written to this bit, the main power supply of the chip, except RTC power, will be shut down immediately. After this bit is set to 1, all registers in RTC module, except RTCCR.1HZ and RTCCR.1HZIE, cannot be changed by write access. This bit is cleared by reset pin reset and hibernating reset. The later one is asserted by wakeup procedure.	RW

PD	PWRON	Description
0	VDDRTC	No power down, keep power on.
1	0 V	Power down enable, turn power off.

12.2.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR)

The HIBERNATE mode Wakeup Filter Counter Register (HWFCR) is a 32-bit read/write register .It filter the glitch generated by a dedicated wakeup pin. The HWFCR is not initialized by any reset.

HWFCR **0x10003024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HWFCR												Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:5	HWFCR	Wakeup pin effective minimum time in number of 32 RTCLK cycles, used as glitch filter logic. Maximum of 2 seconds if the RTCLK is 32768Hz If this value is configured to 0, and the pin keeps low longer than 15 RTCLK periods, it wakes up RTC from Hibernate.	RW
4:0	Reserved	Writing has no effect, read as zero.	R

12.2.7 Hibernate Reset Counter Register (HRCR)

The Hibernate Reset Counter Register is a 32-bit read/write register that specifies hibernate reset assertion time. The HRCR is initialized by PPRST_ .

HRCR **0x10003028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				HRCR								Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:5	HRCR	HIBERNATE Reset waiting time. Number of 32 RTCLK cycles. Maximum 125 ms if the RTCLK is 32768Hz. If this value is configured to 0, it will generate 31 RTCLK HIBERNATE Reset.	RW
4:0	Reserved	Writing has no effect, read as zero.	R

12.2.8 HIBERNATE Wakeup Control Register (HWCR)

The HIBERNATE Wakeup Control Register is a 32-bit read/write register that controls real time clock alarm wake up enable. The reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

HWCR **0x1000302C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												EPDET	WKUPVL	Reserved	EALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R

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3	EPDET	Power detect enable. 0: disable 1: enable (default)	RW
2	WKUPVL	RTC Alarm wakeup pin valid level. 0: Low level sensitive (default) 1: High sensitive	RW
1	Reserved	Writing has no effect, read as zero.	R
0	EALM	RTC Alarm wakeup enable. 0: disable 1: enable	RW

12.2.9 HIBERNATE Wakeup Status Register (HWRSR)

The HIBERNATE Wakeup Status Register is a 32-bit read/write register that reflects wakeup status bits.

HWRSR **0x10003030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							APD	Reserved		HR	PPR	Reserved		PIN	ALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	1*2	1*1	0	0	?	?

NOTES:

1 *1: This reset value only for PPRST_. It is undefined in case of other resets.

2 *2: This reset value only for HRST_. It is undefined in case of other resets.

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zero.	R
8	APD	Accident power down. When the software has not set to HIBERNATE state, the core power is down, then an accident power down is detected. APD is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored. **HR** / **Description** 0: Accident power down has not occurred since the last time the software clears this bit. 1: Accident power down has occurred since the last time the software clears this bit.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5	HR	Hibernate Reset. When a Hibernate reset detected, HR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored.	RW

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		HR: 0 — Hibernate reset has not occurred since the last time the software clears this bit. HR: 1 — Hibernate reset has occurred since the last time the software clears this bit.	
4	PPR	PAD PIN Reset. When a PPRST_ is detected, PPR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored. PPR: 0 — PPRST_ reset has not occurred since last time the software clears this bit. PPR: 1 — PPRST_ reset has occurred since last time the software clears this bit.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	PIN	Wakeup Pin Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by wakeup pin. This bit can only be written with 0. Write with 1 is ignored.	RW
0	ALM	RTC Alarm Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by alarm. This bit can only be written with 0. Write with 1 is ignored.	RW

12.2.10 Hibernate Scratch Pattern Register (HSPR)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

HSPR 0x10003034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	PAT	The pattern.	RW

12.2.11 Write Enable Pattern Register (WENR)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

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WENR **0x1000303C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WEN	Reserved															WENPAT															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31	WEN	The write enable flag. If the WENPAT is 0xA55A then this bit will be 1. When the WEN changes to 1, the RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers could be changed. But RTCCR.SELEXC, RTCCR.HZIE, RTCCR.WRDY may change in any time. This bit is read only and write to it is ignored. There is an exception, when system does NOT have RTC 32Khz crystal. MUST write 1 to RTCCR.SELEXC before write to any value to any other registers.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	WENPAT	The write enable pattern. Before writing any value to RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers, write 0xA55A to WENPAT to set these register writable. If this value is ok, WEN will change to 1. But RTCCR.SELEXC and RTCCR.HZIE are writable in any time. These bits are write-only, always read as 0.	W

WEN	Description
0	Other RTC registers is locked, write these registers will be ignored.
1	Other RTC registers can be changed.

12.2.12 CLK32K Pin control register (CKPCR)

This is a CLK32K pin control register used to configure the CLK32K pin value. The CKPCR is initialized by PPRST_ .

CKPCR **0x10003040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CK32RD	CK32PULL	Reserved	CK32CTL		CK32D
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	1	0	0	0	0

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Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
5	CK32RD	Read this bit will return CLK32K pin status.	R
4	CK32PULL	Pull up configures. **CK32PULL** / **Description** 0 — Pull Up is enabled. 1 — Pull Up is disabled.	RW
3	Reserved	Writing has no effect, read as zero.	R
2:1	CK32CTL	Output RTCLK to CLK32K pin. **CK32CTL** / **Description** 00 — CLK32K pin is set to general input. The pin value can be read by CK32RD bit or GPIO PD14 bit. The input pin should not be left floating, if pull up (CK32PULL) is disabled. The CLK32K pin is only set as input in HIBERNATE mode. 01 — CLK32K pin is set to general output. The pin output value is set by CK32D bit. 10 — GPIO PD14 controls CLK32K pin. The pin output is set by GPIO PD14 bit. The CLK32K pin is output CK32D bit in HIBERNATE mode. 11 — Output RTCLK to CLK32K pin. If this set, CLK32K pin will always output 32K clock, even in HIBERNATE mode.	RW
0	CK32D	When CK32CTL is configured to general output or input (HIBERNATE), Write to this pin will output to CLK32K pin, if configured.	RW

12.2.13 PMCR Power Monitor register (PMCR)

This is a register used to identify the RTC battery has been removed. The software can check the register to know whether RTC battery has ever been down and whether it is needed to setup the real time clock. The PMCR is not initialized by any reset.

PMCR **0x10003044**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															NBF
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R

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0	NBF	No RTC battery flag. Write 1 to this register will update this flag. Write 0 to this register will be clear this flag.	RW

12.3 Time Regulation

Because of the inherent inaccuracy of crystal and other variables, the time counter may be inaccurate. This requires a slight adjustment. The application processor, through the RTCGR, lets you adjust the 1Hz time base to an error of less than 1ppm. Such that if the Hz clock were set to be 1Hz, there would be an error of less than 5 seconds per month.

To determine the value programmed into the RTCGR, you must first measure the output frequency at the oscillator multiplex (approximately 32 kHz) using an accurate time base, such as a frequency counter. This clock is externally visible by selecting the alternate function of GPIO.
To gain access to the clock, program this pin as an output and then switch to the alternate function. To trim the clock, divide the output of the oscillator by an integer value and fractional adjust it by periodically deleting clocks from the stream driving this integer divider.

After the true frequency of the oscillator is known, it must be split into integer and fractional portions. The integer portion of the value (minus one) is loaded into the NC1HZ field of the RTCGR.

The fractional part of the adjustment is done by periodically deleting clocks from the clock stream driving the Hz divider. The trim interval period is hardwired to be 1024 1Hz clock cycles (approximately 17 minutes). The number of clocks (represented by ADJC field of RTCGR) are deleted from the input clock stream per trim interval. If ADJC is programmed to be zero, then no trim operations occur and the RTC is clocked with the raw 32 kHz clock. The relationship between the Hz clock frequency and the nominal 32 kHz clock (f1 and f32K, respectively) is shown in the following equation.

$$f1 = \frac{2^{10} \times (NC1HZ + 1)}{2^{10} \times (NC1HZ + 1) + ADJC} \times \frac{f32k}{NC1HZ + 1}$$

f1 = actual frequency of 1Hz clock
f32k = frequency of either 32.768KHz crystal output or 3.6864MHz crystal output further divided down to 32.914KHz

12.3.1 HIBERNATE Mode

First make sure RTCCR.SELEXC is 0.
When Software writes 1 to PD bit of HCR, the system at once enters HIBERNATE mode. The powers of CORE and IO are disconnected by PWRON pin, no power consumption to core and IO. When a wakeup event occurs, the core enters through a hibernate reset. Only CPM wake up logic and RTC is operating in HIBERNATE mode.

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12.3.1.1 Procedure to Enter HIBERNATE mode

Before enter HIBERNATE mode, software must complete following steps:

1 Finish the current operation and preserve all data to flash.
2 Configure the wake-up sources properly by configure HWCR.
3 Set HIBERNATE MODE. (Set PD bit in HCR to 1)

12.3.1.2 Procedure to Wake-up from HIBERNATE mode

1 The internal hibernate reset signal will be asserted if one of the wake-up sources is issued.
2 Check RSR to determine what caused the reset.
3 Check PIN/ALM bits of HWRSR in order to know whether or not the power-up is caused by which wake-up from HIBERNATE mode.
4 Configure the SDRAM memory controller.
5 Recover the data from flash.

12.4 Clock select

There could be two clock input to RTC internal clock called rtclk. One is OSC32k clock; the other is EXCLK/512.

The software MUST make sure the RTC run in valid clock configuration.

Table 12-3 Clock select registers

RTCCR.SELEXC	CPM.ERCS	Description	Valid
0	0	RTC use OSC32K clock.	OK
0	1		OK
1	0	RTC use EXCLK/512 clock.	OK
1	1	RTC will lost clock. (Not Valid)	NO

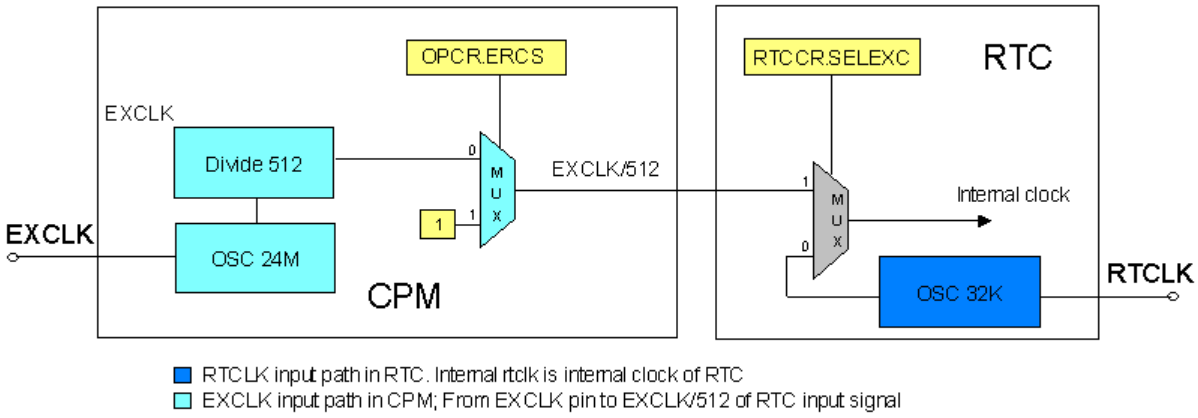


Figure 12-1 RTC clock selection path

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Changing RTCLK sequence:

1 There are both 32KHz crystal and 24Mhz EXCLK crystal connected, so RTCLK input path has 32Khz clock.

In this case, there is no need to change internal clock, so do NOT change SELEXC all the time.

2 There is no 32KHz crystal connected but only 24Mhz EXCLK crystal connected, so RTCLK input path has no clock.

In this case, should flow the sequence below to change internal clock:

a Set OPCR.ERCS of CPM to 1; close EXCLK/512 to RTC.
b Set CLKGR.RTC of CPM to 1; close PCLK to RTC.
c Set RTCCR.SELEXC to 1; change internal clock to EXCLK/512.
d Wait two clock period of clock.
e Clear OPCR.ERCS of CPM to 0; open EXCLK/512 to RTC.
f Clear CLKGR.RTC of CPM to 0; open PCLK to RTC.
g Configure all RTC registers but RTCCR.SELEXC.
h Check RTCCR.SELEXC == 1.
i IF YES, finish this sequence; IF NO, do step (1) again.

NOTE: If using HIBERNATE mode, MUST have both 32KHz crystal (or input 32Khz clock) and 24Mhz EXCLK crystal connected, or RTC time will be insignificant.

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13 Interrupt Controller

13.1 Overview

This chapter describes the interrupt controller included in the XBurst Processor, explains its modes of operation, and defines its registers. The interrupt controller controls the interrupt sources available to the processor and contains the location of the interrupt source to allow software to determine source of all interrupts. It also determines whether the interrupts cause an IRQ to occur and masks the interrupts.

Features:

- Total 64 interrupt sources
- Each interrupt source can be independently enabled
- Priority mechanism to indicate highest priority interrupt
- All the registers are accessed by CPU
- Unmasked interrupts can wake up the chip in sleep mode

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13.2 Register Description

Table 13-1 lists the registers of Interrupt Controller. All of these registers are 32bit, and each bit of the register represents or controls one interrupt source that list in Table 13-1.

All INTC register 32bit access address is physical address.

Table 13-1 INTC Register

Name	Description	RW	Reset Value	Address	Access Size
ICSR0	Interrupt controller Source Register	R	0x00000000	0x10001000	32
ICMR0	Interrupt controller Mask Register	RW	0xFFFFFFFF	0x10001004	32
ICMSR0	Interrupt controller Mask Set Register	W	0x????????	0x10001008	32
ICMCR0	Interrupt controller Mask Clear Register	W	0x????????	0x1000100C	32
ICPR0	Interrupt controller Pending Register	R	0x00000000	0x10001010	32
ICSR1	Interrupt controller Source Register	R	0x00000000	0x10001020	32
ICMR1	Interrupt controller Mask Register	RW	0xFFFFFFFF	0x10001024	32
ICMSR1	Interrupt controller Mask Set Register	W	0x????????	0x10001028	32
ICMCR1	Interrupt controller Mask Clear Register	W	0x????????	0x1000102C	32
ICPR1	Interrupt controller Pending Register	R	0x00000000	0x10001030	32

13.2.1 Interrupt Controller Source Register (ICSR0)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

ICSR0 **0x10001000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	IPU	GPS	TCU0	TCU1	TCU2	DMA0	DMA1	I2C2	OTG	UHC	ETH	SADC	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	KBC	BDMA	TSSI	SSI0	SSI1	GPU	UART0	UART1	UART2	UART3	I2C0	I2C1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICSR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

13.2.2 Interrupt Controller Source Register (ICSR1)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

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ICSR1 **0x10001020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPM	Reserved	I2S2CH	ARB2	AOSD	UART4	PCM1	PCM0	BCH	SCC	MSC0	MSC1	MSC2	AIC	OWI	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICSR1	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

13.2.3 Interrupt Controller Mask Register (ICMR0)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

ICMR0 **0x10001004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	IPU	GPS	TCU0	TCU1	TCU2	DMA0	DMA1	I2C2	OTG	UHC	ETH	SADC	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	KBC	BDMA	TSSI	SSI0	SSI1	GPU	UART0	UART1	UART2	UART3	I2C0	I2C1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMR0	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

13.2.4 Interrupt Controller Mask Register (ICMR1)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

ICMR1 **0x10001024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPM	Reserved	I2S2CH	ARB2	AOSD	UART4	PCM1	PCM0	BCH	SCC	MSC0	MSC1	MSC2	AIC	OWI	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits Of ICMR1	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

13.2.5 Interrupt Controller Mask Set Register (ICMSR0)

This register is used to set bits in the interrupt mask register. This register is write only.

ICMSR0 **0x10001008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	IPU	GPS	TCU0	TCU1	TCU2	DMA0	DMA1	I2C2	OTG	UHC	ETH	SADC	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	KBC	BDMA	TSSI	SSI0	SSI1	GPU	UART0	UART1	UART2	UART3	I2C0	I2C1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMSR0	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

13.2.6 Interrupt Controller Mask Set Register (ICMSR1)

This register is used to set bits in the interrupt mask register. This register is write only.

ICMSR1 **0x10001028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPM	Reserved	I2S2CH	ARB2	AOSD	UART4	PCM1	PCM0	BCH	SCC	MSC0	MSC1	MSC2	AIC	OWI	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMSR1	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

13.2.7 Interrupt Controller Mask Clear Register (ICMCR0)

This register is used to clear bits in the interrupt mask register. This register is write only.

ICMCR0 **0x1000100C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	IPU	GPS	TCU0	TCU1	TCU2	DMA0	DMA1	I2C2	OTG	UHC	ETH	SADC	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	KBC	BDMA	TSSI	SSI0	SSI1	GPU	UART0	UART1	UART2	UART3	I2C0	I2C1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits Of ICMCR0	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

13.2.8 Interrupt Controller Mask Clear Register (ICMCR1)

This register is used to clear bits in the interrupt mask register. This register is write only.

ICMCR1 **0x1000102C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPM	Reserved	I2S2CH	ARB2	AOSD	UART4	PCM1	PCM0	BCH	SCC	MSC0	MSC1	MSC2	AIC	OWI	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMCR1	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

13.2.9 Interrupt Controller Pending Register (ICPR0)

This register contains the status of the interrupt sources after masking. This register is read only.

ICPR0 **0x10001010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	IPU	GPS	TCU0	TCU1	TCU2	DMA0	DMA1	I2C2	OTG	UHC	ETH	SADC	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	KBC	BDMA	TSSI	SSI0	SSI1	GPU	UART0	UART1	UART2	UART3	I2C0	I2C1
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

NOTES:

1 Reserved bits in ICMR0, ICMSR0 and ICMCR0 are normal bits to be written into and read out.

2 Reserved bits in ICSR and ICPR are read-only and always 0.

13.2.10 Interrupt Controller Pending Register (ICPR1)

This register contains the status of the interrupt sources after masking. This register is read only.

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ICPR1 0x10001030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPM	Reserved	I2S2CH	ARB2	AOSD	UART4	PCM1	PCM0	BCH	SCC	MSC0	MSC1	MSC2	AIC	OWI	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR1	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

NOTES:

1 Reserved bits in ICMR1, ICMSR1 and ICMCR1 are normal bits to be written into and read out.

2 Reserved bits in ICSR1 and ICPR1 are read-only and always 0.

13.3 Software Considerations

The interrupt controller is reflecting the status of interrupts sources in the peripheral .

Software should perform the task - determine the interrupt source from in ICPRx. In this chip, pending interrupts have two levels in structure. Interrupting module in the system that contains more than one interrupt sources need software to determine how to service it by reading interrupt status registers within it.

In the interrupt handler, the serviced interrupt source needs to be cleared in the interrupting device. In order to make certain the cleared source request status has been reflected at the corresponding ICPRx bit, software should wait enough time before exiting interrupt state.

The procedure is described following:

1 Interrupt generated.

2 CPU query interrupt sources, saves the current environment and then goes to interrupt common service routine.

3 Get ICPRx.

4 Find the highest priority interrupt and vector it. (The software decides which one has the highest priority)

5 Mask the chosen interrupt by writing the register ICMSRx.

6 Enable the system interrupt to allow the interrupt nesting. (software decided)

7 Execute the interrupt handler and unmask it by writing the register ICMCRx when exit the handler.

8 CPU restores the saved environment and exits the interrupt state.

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14 Timer/Counter Unit

14.1 Overview

The TCU (Timer/Counter with PWM output) contains 8 channels of 16-bit programmable timers (timers 0 to 5). They can be used as Timer or PWM.

TCU has the following features:

- There are two modes of TCU for the eight channels
  - TCU1: Channel 0, 3,4, 5, 6,and 7
  - TCU2: Channel 1,2
- Six independent channels, each consisting of
  - Counter
  - Data register (FULL and HALF)
  - Control register
- Independent clock for each counter, selectable by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- FULL interrupt and HALF interrupt can be generated for each channel using the compare data registers
  - Timer 0-7 can be used as PWM (Set the initial signal level)
  - Timer 0,3-7 can be used as a counter to count external signal (like trackball)
  - Timer 5 has separated interrupt
  - Timer 0-4 and timer 6-7 has one interrupt in common
  - OST uses interrupt 0, Timer 0 uses interrupt 1, and Timer 1-7 uses interrupt 2
- The difference between TCU1 and TCU2
  - TCU1: It cannot work in sleep mode, but operated easily
  - TCU2: It can work in sleep mode, but operated more complicated than TCU1

14.2 Pin Description

Table 14-1 PWM Pins Description

Name	I/O	Description
PWM [7:0]	Output	PWM channel output signals.

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14.3 Register Description

In this section, we will describe the registers in timer. Following table lists all the registers definition. All timer register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
TSTR	Timer Status Register	R	0x00000000	0x100020F0	32
TSTSR	Timer Status Set Register	W	0x????????	0x100020F4	32
TSTCR	Timer Status Clear Register	W	0x????????	0x100020F8	32
TSR	Timer STOP Register	R	0x00000000	0x1000201C	32
TSSR	Timer STOP Set Register	W	0x00000000	0x1000202C	32
TSCR	Timer STOP Clear Register	W	0x0000	0x1000203C	32
TER	Timer Counter Enable Register	R	0x0000	0x10002010	16
TESR	Timer Counter Enable Set Register	W	0x????	0x10002014	16
TECR	Timer Counter Enable Clear Register	W	0x????	0x10002018	16
TFR	Timer Flag Register	R	0x003F003F	0x10002020	32
TFSR	Timer Flag Set Register	W	0x????????	0x10002024	32
TFCR	Timer Flag Clear Register	W	0x????????	0x10002028	32
TMR	Timer Mask Register	R	0x00000000	0x10002030	32
TMSR	Timer Mask Set Register	W	0x????????	0x10002034	32
TMCR	Timer Mask Clear Register	W	0x????????	0x10002038	32
TDFR0	Timer Data FULL Register 0	RW	0x????	0x10002040	16
TDHR0	Timer Data HALF Register 0	RW	0x????	0x10002044	16
TCNT0	Timer Counter 0	RW	0x????	0x10002048	16
TCSR0	Timer Control Register 0	RW	0x0000	0x1000204C	16
TDFR1	Timer Data FULL Register 1	RW	0x????	0x10002050	16
TDHR1	Timer Data HALF Register 1	RW	0x????	0x10002054	16
TCNT1	Timer Counter 1	RW	0x????	0x10002058	16
TCSR1	Timer Control Register 1	RW	0x0000	0x1000205C	16
TDFR2	Timer Data FULL Register 2	RW	0x????	0x10002060	16
TDHR2	Timer Data HALF Register 2	RW	0x????	0x10002064	16
TCNT2	Timer Counter 2	RW	0x????	0x10002068	16
TCSR2	Timer Control Register 2	RW	0x0000	0x1000206C	16
TDFR3	Timer Data FULL Register 3	RW	0x????	0x10002070	16
TDHR3	Timer Data HALF Register 3	RW	0x????	0x10002074	16
TCNT3	Timer Counter 3	RW	0x????	0x10002078	16
TCSR3	Timer Control Register 3	RW	0x0000	0x1000207C	16
TDFR4	Timer Data FULL Register 4	RW	0x????	0x10002080	16
TDHR4	Timer Data HALF Register 4	RW	0x????	0x10002084	16
TCNT4	Timer Counter 4	RW	0x????	0x10002088	16

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TCSR4	Timer Control Register 4	RW	0x0000	0x1000208C	16
TDFR5	Timer Data FULL Register 5	RW	0x????	0x10002090	16
TDHR5	Timer Data HALF Register 5	RW	0x????	0x10002094	16
TCNT5	Timer Counter 5	RW	0x????	0x10002098	16
TCSR5	Timer Control Register 5	RW	0x0000	0x1000209C	16
TDFR6	Timer Data FULL Register 6	RW	0x????	0x100020A0	16
TDHR6	Timer Data HALF Register 6	RW	0x????	0x100020A4	16
TCNT6	Timer Counter 6	RW	0x????	0x100020A8	16
TCSR6	Timer Control Register 6	RW	0x0000	0x100020AC	16
TDFR7	Timer Data FULL Register 7	RW	0x????	0x100020B0	16
TDHR7	Timer Data HALF Register 7	RW	0x????	0x100020B4	16
TCNT7	Timer Counter 7	RW	0x????	0x100020B8	16
TCSR7	Timer Control Register 7	RW	0x0000	0x100020BC	16

14.3.1 Timer Control Register (TCSR)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

TCSR0, TCSR1, TCSR2, TCSR3, TCSR4, TCSR5 TCSR6, TCSR7

0x1000204C, 0x1000205C, 0x1000206C, 0x1000207C, 0x1000208C, 0x1000209C, 0x100020AC, 0x100020BC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				BYPASS	CLRZ	SD	INITL	PWM_EN	PWM_IN_EN	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:11	Reserved	Writing has no effect, read as zero.	R
11	BYPASS	PWM bypass mode. 1: If PCK_EN = 1, this channel output PIXCLK; If RTC_EN = 1, this channel output RTCCLK; If EXT_EN = 1, this channel output EXTAL; Only one of those XXX_EN is permit available during one time. 0: This BYPASS function disable. *Only when you want to let this PWM channel output some special clock (PIXCLK, RTCLK and EXTAL clock), you can set this register to 1. Otherwise keep it to 0. When you want to use BYPASS function, not forget offer clock supplies of relate channel (relate to register TSR, TSSR, TSCR).	RW

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<table>
<tr><td>10</td><td>CLRZ</td><td>Clear counter to 0. It is only used in TCU2 mode.
Writing 1 to this bit will clear the counter to 0. When the counter is finished setting to 0, it will be cleared by hardware.
Writing 0 to this bit will be ignored.</td><td>RW</td></tr>
<tr><td>9</td><td>SD</td><td>Shut Down (SD) the PWM output. It is only used in TCU1 mode.
0: Graceful shutdown
1: Abrupt shutdown
Graceful shutdown: The output level for PWM output will keep the level after the comparison match of FULL.
Abrupt shutdown: The output level for PWM output will keep the level.</td><td>RW</td></tr>
<tr><td>8</td><td>INITL</td><td>Selects an initial output level for PWM output.
1: High
0: Low</td><td>RW</td></tr>
<tr><td>7</td><td>PWM_EN</td><td>PWM output pin control bit.
1: PWM pin output enable
0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL</td><td>RW</td></tr>
<tr><td>6</td><td>PWM_IN_EN</td><td>PWM input mode enable.
Set to 1 to enable this function.
In this function, PWM pin need to set as input in GPIO to receive external signal, EXT_EN, RTC_EN, PCK_EN need to set 0.
And TCNT became a counter to count this signal’s both edges. (This bit in TCSR1, 2 are reserved).</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
1: Enable
0: Disable</td><td>RW</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
1: Enable
0: Disable</td><td>RW</td></tr>
<tr><td>0</td><td>PCK_EN</td><td>Select PCLK as the timer clock input.
1: Enable
0: Disable</td><td>RW</td></tr>
</table>

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NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

14.3.2 Timer Data FULL Register (TDFR)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

TDFR0, TDFR1, TDFR2, TDFR3, TDFR4, TDFR5, TDFR6, TDFR7 — **0x10002040, 0x10002050, 0x10002060, 0x10002070, 0x10002080, 0x10002090, 0x100020A0, 0x100020B0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDFR															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

14.3.3 Timer Data HALF Register (TDHR)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate) But it is not suggested changing when counter is working in TCU2 mode.

TDHR0, TDHR1, TDHR2, TDHR3, TDHR4, TDHR5, TDHR6, TDHR7 — **0x10002044, 0x10002054, 0x10002064, 0x10002074, 0x10002084, 0x10002094, 0x100020A4, 0x100020B4**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDHR															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

14.3.4 Timer Counter (TCNT)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up

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using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up.

TCU1: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

TCU2: The counter data can be read out at any time, but you should read TSTR.REALn to check whether the data is real data or not. The data can only be written before counter is started, and the counter clock is pclk. But it can be cleared to 0 by setting TCSR.CLRZ to 1, and if the counter is really cleared, TCSR.CLRZ will be set to 0 by hardware.

TCNT0, TCNT1, TCNT2, TCNT3, TCNT4, TCNT5, TCNT6, TCNT7 — **0x10002048, 0x10002058, 0x10002068, 0x10002078, 0x10002088, 0x10002098, 0x100020A8, 0x100020B8**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

14.3.5 Timer Counter Enable Register (TER)

The TER is a 16-bit read-only register. It contains the counter enable control bits for each channel. It is initialized to 0x0000 by any reset. It can only be set by register TESR and TECR. Since the timer enable control bits are located in the same addresses, two or more timers can be started at the same time.

TER — **0x10002010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTEN	Reserved							TCEN 7	TCEN 6	TCEN 5	TCEN 4	TCEN 3	TCEN 2	TCEN 1	TCEN 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	OSTEN	Enable the counter in OST. 1: Begin counting up 0: Stop counting up	
14:8	Reserved	Writing has no effect, read as zero.	R
7	TCEN 7	Enable the counter in timer 7. 1: Begin counting up 0: Stop counting up	R

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6	TCEN 6	Enable the counter in timer 6. 1: Begin counting up 0: Stop counting up	R
5	TCEN 5	Enable the counter in timer 5. 1: Begin counting up 0: Stop counting up	R
4	TCEN 4	Enable the counter in timer 4. 1: Begin counting up 0: Stop counting up	R
3	TCEN 3	Enable the counter in timer 3. 1: Begin counting up 0: Stop counting up	R
2	TCEN 2	Enable the counter in timer 2. 1: Begin counting up 0: Stop counting up	R
1	TCEN 1	Enable the counter in timer 1. 1: Begin counting up 0: Stop counting up	R
0	TCEN 0	Enable the counter in timer 0. 1: Begin counting up 0: Stop counting up	R

14.3.6 Timer Counter Enable Set Register (TESR)

The TCCSR is a 32-bit write-only register. It contains the counter enable set bits for each channel. Since the timer enable control set bits are located in the same addresses, two or more timers can be started at the same time.

TESR **0x10002014**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTST	Reserved							TCST 7	TCST 6	TCST 5	TCST 4	TCST 3	TCST 2	TCST 1	TCST 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTST	Set OSTEN bit of TER. 1: Set OSTEN bit to 1 0: Ignore	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	TCST 7	Set TCEN 7 bit of TER. 1: Set TCEN 5 bit to 1	W

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		0: Ignore	
6	TCST 6	Set TCEN 6 bit of TER. 1: Set TCEN 5 bit to 1 0: Ignore	W
5	TCST 5	Set TCEN 5 bit of TER. 1: Set TCEN 5 bit to 1 0: Ignore	W
4	TCST 4	Set TCEN 4 bit of TER. 1: Set TCEN 4 bit to 1 0: Ignore	W
3	TCST 3	Set TCEN 3 bit of TER. 1: Set TCEN 3 bit to 1 0: Ignore	W
2	TCST 2	Set TCEN 2 bit of TER. 1: Set TCEN 2 bit to 1 0: Ignore	W
1	TCST 1	Set TCEN 1 bit of TER. 1: Set TCEN 1 bit to 1 0: Ignore	W
0	TCST 0	Set TCEN 0 bit of TER. 1: Set TCEN 0 bit to 1 0: Ignore	W

14.3.7 Timer Counter Enable Clear Register (TECR)

The TECR is a 32-bit write-only register. It contains the counter enable clear bits for each channel. Since the timer enable clear bits are located in the same addresses, two or more timers can be stop at the same time.

TECR **0x10002018**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCL	Reserved							TCCL 7	TCCL 6	TCCL 5	TCCL 4	TCCL 3	TCCL 2	TCCL 1	TCCL 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTCL	Set OSTEN bit of TER. 1: Set OSTEN 5 bit to 0 0: Ignore	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	TCCL 7	Set TCEN 7 bit of TER. 1: Set TCEN 6 bit to 0	W

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		0: Ignore	
6	TCCL 6	Set TCEN 7 bit of TER. 1: Set TCEN 6 bit to 0 0: Ignore	W
5	TCCL 5	Set TCEN 5 bit of TER. 1: Set TCEN 5 bit to 0 0: Ignore	W
4	TCCL 4	Set TCEN 4 bit of TER. 1: Set TCEN 4 bit to 0 0: Ignore	W
3	TCCL 3	Set TCEN 3 bit of TER. 1: Set TCEN 3 bit to 0 0: Ignore	W
2	TCCL 2	Set TCEN 2 bit of TER. 1: Set TCEN 2 bit to 0 0: Ignore	W
1	TCCL 1	Set TCEN 1 bit of TER. 1: Set TCEN 1 bit to 0 0: Ignore	W
0	TCCL 0	Set TCEN 0 bit of TER. 1: Set TCEN 0 bit to 0 0: Ignore	W

14.3.8 Timer Flag Register (TFR)

The TFR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It can also be set by register TFSR and TFCR. It is initialized to 0x00000000 by any reset.

TFR **0x10002020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFLAG 7	HFLAG 6	HFLAG 5	HFLAG 4	HFLAG 3	HFLAG 2	HFLAG 1	HFLAG 0	OSTFLAG	Reserved							FFLAG 7	FFLAG 6	FFLAG 5	FFLAG 4	FFLAG 3	FFLAG 2	FFLAG 1	FFLAG 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFLAG 7~0	HALF comparison match flag. (TCNT = TDHR) 1: Comparison match 0: Comparison not match	R
15	OSTFLAG	OST comparison match flag. (OSTCNT = OSTDR) 1: Comparison match	R

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		0: Comparison not match	
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFLAG 7~0	FULL comparison match flag. (TCNT = TDFR) 1: Comparison match 0: Comparison not match	R

14.3.9 Timer Flag Set Register (TFSR)

The TFSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

TFSR **0x10002024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFST 7	HFST 6	HFST 5	HFST 4	HFST 3	HFST 2	HFST 1	HFST 0	OSTFST	Reserved							FFST 7	FFST 6	FFST 5	FFST 4	FFST 3	FFST 2	FFST 1	FFST 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFST 7~0	Set HFLAG n bit of TFR. 1: Set HFLAG n bit to 1 0: Ignore	W
15	OSTFST	Set OSTFLAG n bit of TFR. 1: Set OSTFLAG n bit to 1 0: Ignore	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFST 7~0	Set FFLAG n bit of TFR. 1: Set FFLAG n bit to 1 0: Ignore	W

14.3.10 Timer Flag Clear Register (TFCR)

The TFCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

TFCR **0x10002028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFCL 7	HFCL 6	HFCL 5	HFCL 4	HFCL 3	HFCL 2	HFCL 1	HFCL 0	OSTFCL	Reserved							FFCL 7	FFCL 6	FFCL 5	FFCL 4	FFCL 3	FFCL 2	FFCL 1	FFCL 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFCL 7~0	Set HFLAG n bit of TFR. 1: Set FFLAG n bit to 0 0: Ignore	W
15	OSTFCL	Set OSTFLAG n bit of TFR. 1: Set OSTFLAG n bit to 0 0: Ignore	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFCL 7~0	Set FFLAG n bit of TFR. 1: Set FFLAG n bit to 0 0: Ignore	W

14.3.11 Timer Mast Register (TMR)

The TMR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It is initialized to 0x003F003F by any reset. It can only be set by register TMSR and TMCR.

TMR **0x10002030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMASK 7	HMASK 6	HMASK 5	HMASK 4	HMASK 3	HMASK 2	HMASK 1	HMASK 0	OSTMASK	Reserved							FMASK 7	FMASK 6	FMASK 5	FMASK 4	FMASK 3	FMASK 2	FMASK 1	FMASK 0
RST	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HMASK 7~0	HALF comparison match interrupt mask. 1: Comparison match interrupt mask 0: Comparison match interrupt not mask	R
15	OSTMASK	OST comparison match interrupt mask. 1: Comparison match interrupt mask 0: Comparison match interrupt not mask	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMASK 7~0	FULL comparison match interrupt mask. 1: Comparison match interrupt mask 0: Comparison match interrupt not mask	R

14.3.12 Timer Mask Set Register (TMSR)

The TMSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

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TMSR 0x10002034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMST 7	HMST 6	HMST 5	HMST 4	HMST 3	HMST 2	HMST 1	HMST 0	OSTMST	Reserved							FMST 7	FMST 6	FMST 5	FMST 4	FMST 3	FMST 2	FMST 1	FMST 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HMST 7~0	Set HMASK n bit of TMR. 0: Ignore; 1: Set HMASK n bit to 1.	W
15	OSTMST	Set OSTMASK n bit of TMR. 0: Ignore; 1: Set OSTMASK n bit to 1.	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMST 7~0	Set FMASK n bit of TMR. 0: Ignore; 1: Set FMASK n bit to 1.	W

14.3.13 Timer Mask Clear Register (TMCR)

The TMCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

TMCR 0x10002038

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMCL 7	HMCL 6	HMCL 5	HMCL 4	HMCL 3	HMCL 2	HMCL 1	HMCL 0	OSTMCL	Reserved							FMCL 7	FMCL 6	FMCL 5	FMCL 4	FMCL 3	FMCL 2	FMCL 1	FMCL 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
23:16	HMCL 7~0	Set HMASK n bit of TMR. 0: Ignore; 1: Set HMASK n bit to 0.	W
15	OSTMCL	Set OSTMASK n bit of TMR. 0: Ignore; 1: Set OSTMASK n bit to 0.	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMCL 7~0	Set FMASK n bit of TMR. 0: Ignore; 1: Set FMASK n bit to 0.	W

14.3.14 Timer Stop Register (TSR)

The TSR is a 32-bit read-only register. It contains the timer stop control bits for each channel, WDT

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and OST. It is initialized to 0x00000000 by any reset. It can only be set by register TSSR and TSCR. If set, clock supplies to timer n / WDT / OST is stopped, and registers of the timer / WDT / OST cannot be accessed also.

TSR **0x1000201C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTS	OSTS	Reserved							STOP 7	STOP 6	STOP 5	STOP 4	STOP 3	STOP 2	STOP 1	STOP 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTS	1: The clock supplies to WDT is stopped 0: The clock supplies to WDT is supplied	R
15	OSTS	1: The clock supplies to OST is stopped 0: The clock supplies to OST is supplied	R
14:8	Reserved	Writing has no effect, read as zero.	R
7	STOP 7	1: The clock supplies to timer 7 is stopped 0: The clock supplies to timer 7 is supplied	R
6	STOP 6	1: The clock supplies to timer 6 is stopped 0: The clock supplies to timer 6 is supplied	R
5	STOP 5	1: The clock supplies to timer 5 is stopped 0: The clock supplies to timer 5 is supplied	R
4	STOP 4	1: The clock supplies to timer 4 is stopped 0: The clock supplies to timer 4 is supplied	R
3	STOP 3	1: The clock supplies to timer 3 is stopped 0: The clock supplies to timer 3 is supplied	R
2	STOP 2	1: The clock supplies to timer 2 is stopped 0: The clock supplies to timer 2 is supplied	R
1	STOP 1	1: The clock supplies to timer 1 is stopped 0: The clock supplies to timer 1 is supplied	R
0	STOP 0	1: The clock supplies to timer 0 is stopped 0: The clock supplies to timer 0 is supplied	R

14.3.15 Timer Stop Set Register (TSSR)

The TCSR is an 32-bit write-only register. It contains the timer stop set bits for each channel, WDT and OST. Since the timer stop control set bits are located in the same addresses, two or more timers can be started at the same time.

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TSSR 0x1000202C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSS	OSTSS	Reserved							STPS 7	STPS 6	STPS 5	STPS 4	STPS 3	STPS 2	STPS 1	STPS 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSS	Set WDTS bit of TSR. 0: Ignore; 1: Set WDTS bit to 1.	W
15	OSTSS	Set OSTS bit of TSR. 0: Ignore; 1: Set OSTS bit to 1.	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	STPS 7	Set STOP 7 bit of TSR. 0: Ignore; 1: Set STOP 7 bit to 1.	W
6	STPS 6	Set STOP 6 bit of TSR. 0: Ignore; 1: Set STOP 6 bit to 1.	W
5	STPS 5	Set STOP 5 bit of TSR. 0: Ignore; 1: Set STOP 5 bit to 1.	W
4	STPS 4	Set STOP 4 bit of TSR. 0: Ignore; 1: Set STOP 4 bit to 1.	W
3	STPS 3	Set STOP 3 bit of TSR. 0: Ignore; 1: Set STOP 3 bit to 1.	W
2	STPS 2	Set STOP 2 bit of TSR. 0: Ignore; 1: Set STOP 2 bit to 1.	W
1	STPS 1	Set STOP 1 bit of SR. 0: Ignore; 1: Set STOP 1 bit to 1.	W
0	STPS 0	Set STOP 0 bit of TSR. 0: Ignore; 1: Set STOP 0 bit to 1.	W

14.3.16 Timer Stop Clear Register (TSCR)

The TSCR is an 32-bit write-only register. It contains the timer stop clear bits for each channel, WDT and OST. Since the timer stop clear bits are located in the same addresses, two or more timers can be stop at the same time.

TSCR 0x1000203C

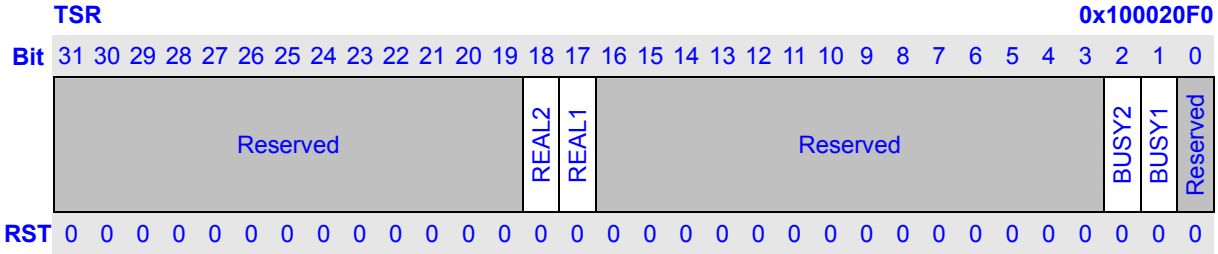
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSC	OSTSC	Reserved							STPC 7	STPC 6	STPC 5	STPC 4	STPC 3	STPC 2	STPC 1	STPC 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSC	Set WDTS bit of TSR. 0: Ignore; 1: Set WDTS bit to 0.	W
15	OSTSC	Set OSTS bit of TSR. 0: Ignore; 1: Set OSTS bit to 0.	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	STPC 7	Set STOP 7 bit of TSR. 0: Ignore; 1: Set STOP 7 bit to 0.	W
6	STPC 6	Set STOP 6 bit of TSR. 0: Ignore; 1: Set STOP 6 bit to 0.	W
5	STPC 5	Set STOP 5 bit of TSR. 0: Ignore; 1: Set STOP 5 bit to 0.	W
4	STPC 4	Set STOP 4 bit of TSR. 0: Ignore; 1: Set STOP 4 bit to 0.	W
3	STPC 3	Set STOP 3 bit of TSR. 0: Ignore; 1: Set STOP 3 bit to 0.	W
2	STPC 2	Set STOP 2 bit of TSR. 0: Ignore; 1: Set STOP 2 bit to 0.	W
1	STPC 1	Set STOP 1 bit of TSR. 0: Ignore; 1: Set STOP 1 bit to 0.	W
0	STPC 0	Set STOP 0 bit of TSR. 0: Ignore; 1: Set STOP 0 bit to 0.	W

14.3.17 Timer Status Register (TSTR)

The TSTR is a 32-bit read-only register. It contains the status of channel in TCU2 mode. The register can be written by setting register TSTSR and TSTCR.



Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REAL 2	0: The value read from counter 2 is a false value 1: The value read from counter 2 is a real value	R
17	REAL1	0: The value read from counter 1 is a false value 1: The value read from counter 1 is a real value	R

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16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSY 2	0: The counter 2 is ready now 1: The counter 2 is busy now	R
1	BUSY1	0: The counter 1 is ready now 1: The counter 1 is busy now	R
0	Reserved	Writing has no effect, read as zero.	R

14.3.18 Timer Status Set Register (TSTSR)

The TSTSR is a 32-bit write-only register. It contains the timer status set bits for each channel.

TSTSR **0x100020F4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													REALS 2	REALS 1	Reserved														BUSYS 2	BUSYS 1	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REALS 2	Set REAL 2 bit of TSTR. 0: Ignore; 1: Set REAL 2 bit to 1.	R
17	REALS 1	Set REAL 1 bit of TSTR. 0: Ignore; 1: Set REAL 1 bit to 1.	R
16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSYS 2	Set BUSY 2 bit of TSTR. 0: Ignore; 1: Set BUSY 2 bit to 1.	R
1	BUSYS 1	Set BUSY 1 bit of TSTR. 0: Ignore; 1: Set BUSY 1 bit to 1.	R
0	Reserved	Writing has no effect, read as zero.	R

14.3.19 Timer Status Clear Register (TSTCR)

The TSTCR is a 32-bit write-only register. It contains the timer status clear bits for each channel.

TSTCR **0x100020F8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													REALC 2	REALC 1	Reserved														BUSYC 2	BUSYC 1	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	REALC 2	Clear REAL 2 bit of TSTR. 0: Ignore; 1: Clear REAL 2 bit to 1.	R
17	REALC 1	Clear REAL 1 bit of TSTR. 0: Ignore; 1: Clear REAL 1 bit to 1.	R
16:3	Reserved	Writing has no effect, read as zero.	R
2	BUSYC 2	Clear BUSY 2 bit of TSTR. 0: Ignore; 1: Clear BUSY 2 bit to 1.	R
1	BUSYC 1	Clear BUSY 1 bit of TSTR. 0: Ignore; 1: Clear BUSY 1 bit to 1.	R
0	Reserved	Writing has no effect, read as zero.	R

14.4 Operation

14.4.1 Basic Operation in TCU1 Mode

The value of TDFR should be bigger than TDHR, and the minimum settings are TDHR = 0 and TDFR = 1. In this case, the timer output clock cycle is the input clock × 1/2. If TDHR > TDFR, no comparison TFHR signal is generated.

Before the timer counter begin to count up, we need to do as follows:

If you want to use PWM you should set TCSR.PWM_EN to be 0 before you initial TCU.

1 Initial the configuration.
   a Writing TCSR.INITL to initialize PWM output level.
   b Writing TCSR.SD to setting the shutdown mode (Abrupt shutdown or Graceful shutdown).
   c Writing TCSR.PRESCALE to set TCNT count clock frequency.
   d Setting TCNT, TDHR and TDFR.

2 Enable the clock.
   a Writing TCSR.PWM_EN to set whether enable PWM or disable PWM.
   b Writing TCSR.EXT_EN, TCSR.RTC_EN or TCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN can be set to 1.

After initialize the register of timer, we should start the counter as follows:

3 Enable the counter.
   Setting the TESR.TCST bit to 1 to enable the TCNT.

NOTE: The input clock and PCLK should follow the rules advanced before.

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14.4.2 Disable and Shutdown Operation in TCU1 Mode

1 Setting the TECR.TCCL bit to 1 to disable the TCNT.

14.4.3 Basic Operation in TCU2 Mode

The value of TDFR should be bigger than TDHR, and the minimum settings are TDHR = 0 and TDFR = 1. In this case, the timer output clock cycle is the input clock × 1/2. If TDHR > TDFR, no comparison TFHR signal is generated.

Initial state is that TCSR.PRESCALE=0, TCSR.PWM_EN=0 and TCENR=0.

1 Reset the TCU.
   a Writing TCSR.PCK_EN to 1 to select pclk as the input clock.
   b Set TCSR.CLRZ to 1 to clear TCNT or set TCNT to an initial value.
   c Writing TCSR.PCK_EN to 0 to close the input clock.
2 Initial the configuration.
   a Setting TDHR and TDFR.
   b Writing TCSR.INITL to initialize PWM output level (if used PWM).
   c Writing TCSR.PRESCALE to set TCNT count clock frequency.
   d Writing TCSR.EXT_EN, TCSR.RTC_EN or TCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN can be set to 1.
   e Writing TCSR.PWM_EN to set whether enable PWM or disable PWM.

After initialize the register of timer, we should start the counter as follows:

3 Setting the TESR.TCST bit to 1 to enable the TCNT.

NOTES:

1 You can clear the counter when counter is working.
   a Set TCSR.CLRZ to 1 to clear TCNT.
   b Wait till TSTR.BUSY = 0, that is the counter have been cleared.
2 You can enable PWM or disable PWM the counter when counter is working.
   a Set TCSR.PWM_EN to 1 to enable PWM.
   b Set TCSR.PWM_EN to 0 to disable PWM.

14.4.4 Disable and Shutdown Operation in TCU2 Mode

1 Writing TCSR.PWM_EN to 0 to disable PWM.
2 Setting the TECR.TCCL bit to 1 to disable the TCNT.
3 Wait till TSTR.BUSY = 0, that is the reset of counter is finished.

14.4.5 Read Counter in TCU2 Mode

If you want to read the data from register TCNT when the TCU is working, you can check TSTR.REAL

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whether it is good or not. It is suggested that:

1 If TSTR.REAL==1, the data read is available.
2 If TSTR.REAL==0, reread the counter till TSTR.REAL==1, the data read is available.
3 If TSTR.REAL is always 0, you can read some data, and lose some data that is quick different from the others. Then choose a data from them as the available data.

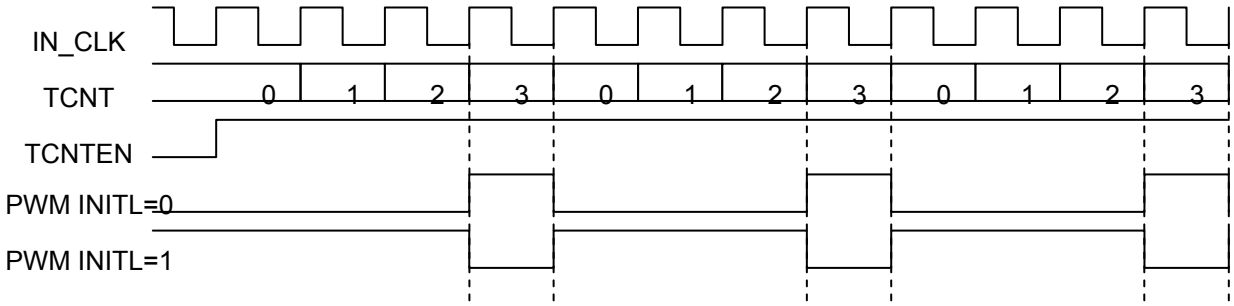
NOTES:

1 It suggested that (1), (2) is often used when the counter clock is very slow.
2 It suggested that (3) is often used when the counter clock is very fast.

14.4.6 Pulse Width Modulator (PWM)

Timer 0~7 can be used as Pulse Width Modulator (PWM). The PWM can be used to control the back light inverter or adjust bright or contrast of LCD panel.

FULL comparison match signal and HALF comparison match signal can determine an attribute of the PWM_OUT waveform. FULL comparison match signal specifies the clock cycle for the PWM module clock. HALF comparison match signal specifies the duty ratio for the PWM module clock.



14.4.7 Trackball Input Waveform Detect

Timer 0, 3~7 can be used as a waveform edge counter to count both positive edge and negative edge of an external input waveform. For example, a trackball device's input. 4 timers will need to count all four directions (up, down, left, right). You need configure relate GPIO (set relate 4 PWM IO as input) and set relate TCSR.PWM_IN_EN to 1. Both relate TDFR and TDHR need to set to 0xFFFF, unless you need a special interrupt when the counter hit TDFR or TDHR. The counter will clear to 0 when hit TDFR.

Before the timer counter begin to count up, we need to do as follows:

1 Initial the configuration.
  a Writing TCSR.SD to setting the shutdown mode (Abrupt shutdown or Graceful shutdown).
  b Writing TCSR.PRESCALE to set to 0.
  c Setting TCNT, TDHR and TDFR.
2 Enable the clock.
  a Writing TCSR.PWM_EN to disable PWM.
  b Writing TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN to 0, TCSR.PWM_IN_EN

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to 1 to select the input clock and enable the input clock.

After initialize the register of timer, we should start the counter as follows:

3 Enable the counter.

Setting the TESR.TCST bit to 1 to enable the TCNT.

NOTE: The input clock and PCLK should follow the rules advanced before.

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15 Operating System Timer

15.1 Overview

The OST (Operating System Timer) contains one 64-bit programmable timer. It can be used as operating system timer.

OST has the following features:

- OST includes:
  - 64-bit Counter
  - 32-bit Compare Data Register
  - Control Register
- Independent clock for each counter, selectable by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Match interrupt can be generated for OST using the compare data registers
  - Interrupt flag and interrupt mask is same with TCU in TCU spec

15.2 Register Description

In this section, we will describe the registers in OST. Following table lists all the registers definition. All OST register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
OSTDR	Operating System Timer Data Register	RW	0x????????	0x100020e0	32
OSTCNTL	Operating System Timer Counter Lower 32 Bits	RW	0x????????	0x100020e4	32
OSTCNTH	Operating System Timer Counter Higher 32 Bits	RW	0x????????	0x100020e8	32
OSTCSR	Operating System Timer Control Register	RW	0x0000	0x100020ec	16
OSTCNTH BUF	Operating System Timer Counter Higher 32 Bits Buffer	R	0x????????	0x100020fc	32

15.2.1 Operating System Control Register (OSTCSR)

The TCSR is a 16-bit read/write register. It contains the control bits for OST. It is initialized to 0x00 by any reset.

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OSTCSR **0x100020ec**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNT_MD	Reserved					SD	Reserved			PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	CNT_MD	Counter mode choose bit. 0: When the value counter is equal to compare value, the counter will be cleared, and increase from 0. 1: When the value counter is equal to compare value, the counter will go on increasing till overflow, and then increase from 0.	
14:6	Reserved	Writing has no effect, read as zero.	R
9	SD	Shut Down (SD) the PWM output. It is only used in TCU1 mode. 0: Graceful shutdown (only used when CNT_MD = 0) 1: Abrupt shutdown	RW
5:3	PRESCALE	These bits select the TCNT count clock frequency.	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

2	EXT_EN	Select EXTAL as the timer clock input. 1: Enable 0: Disable	RW
1	RTC_EN	Select RTCCLK as the timer clock input. 1: Enable 0: Disable	RW
0	PCK_EN	Select PCLK as the timer clock input. 1: Enable 0: Disable	RW

NOTE: The input clock of timer and the PCLK should keep to the rules as follows.

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**

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PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

15.2.2 Operating System Timer Data Register (OSTDR)

The operating system timer data register OSTDR is used to store the data to be compared with the content of the operating system timer up-counter OSTCNT. This register can be directly read and written. (Default: indeterminate)

OSTDR **0x100020e0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTDR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

15.2.3 Operating System Timer Counter (OSTCNTH, OSTCNTL)

The operating system timer counter (OSTCNT) is a 64-bit read/write counter. The up-counter OSTCNT can be set by software and counts up using the prescaler output clock. The data can be read out at any time. The counter data can be written at any time. (Default: indeterminate)

OSTCNTH **0x100020e8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTH																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

OSTCNTL **0x100020e4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTL																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

15.2.4 Operating System Timer Counter high 32 bits buffer (OSTCNTHBUF)

The operating system timer counter high 32 bits buffer OSTCNTHBUF is used to store the high 32 bits of OSTCNT when its lower 32 bits are read by software. This register can be directly read. (Default: indeterminate)

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OSTCNTHBUF																														0x100020fc
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTHBUF																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

15.3 Operation

15.3.1 Basic Operation

Before the timer counter begin to count up, we need to do as follows:

1 Initial the configuration.

a Writing TCSR.SD to setting the shutdown mode (Abrupt shutdown or Graceful shutdown).

b Writing OSTCSR.PRESCALE to set OSTCNT count clock frequency.

c Setting OSTCNTL/H and OSTDR.

2 Enable the clock.

Writing OSTCSR.EXT_EN, OSTCSR.RTC_EN or OSTCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of OSTCSR.EXT_EN, OSTCSR.RTC_EN and OSTCSR.PCK_EN can be set to 1.

After initialize the register of timer, we should start the counter as follows:

3 Enable the counter.

Setting the TESR.OSTCST bit to 1 to enable the OSTCNT.

NOTE: The input clock and PCLK should follow the rules advanced before.

15.3.2 Disable and Shutdown Operation

1 Setting the TECR.OSTCCL bit to 1 to disable the OSTCNT.

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16 Watchdog Timer

16.1 Overview

The watchdog timer is used to resume the processor whenever it is disturbed by malfunctions such as noise and system errors. The watchdog timer can generate the reset signal.

Features:

- Generates WDT reset
- A 16-bit Data register and a 16-bit counter
- Counter clock uses the input clock selected by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

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16.2 Register Description

In this section, we will describe the registers in WDT. Following table lists all the registers definition. All WDT register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
TDR	Watchdog Timer Data Register	RW	0x????	0x10002000	16
TCER	Watchdog Counter Enable Register	RW	0x00	0x10002004	8
TCNT	Watchdog Timer Counter	RW	0x????	0x10002008	16
TCSR	Watchdog Timer Control Register	RW	0x0000	0x1000200C	16

16.2.1 Watchdog Control Register (TCSR)

The TCSR is a 16-bit read/write register. It contains the control bits for WDT. It is initialized to 0x00 by any reset.

TCSR 0x1000200C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:6	Reserved	Writing has no effect, read as zero.	R
5:3	PRESCALE	These bits select the TCNT count clock frequency.	RW
2	EXT_EN	Select EXTAL as the timer clock input. 1: Enable 0: Disable	RW
1	RTC_EN	Select RTCCLK as the timer clock input. 1: Enable	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

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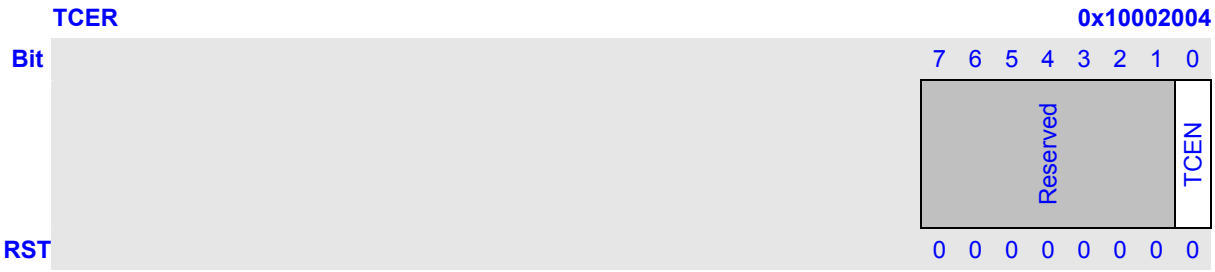
		0: Disable	
0	PCK_EN	Select PCLK as the timer clock input. 1: Enable 0: Disable	RW

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

16.2.2 Watchdog Enable Register (TCER)

The TCER is an 8-bit read/write register. It contains the counter enable control bits for watchdog. It is initialized to 0x00 by any reset.



Bits	Name	Description	RW
7:1	Reserved	Writing has no effect, read as zero.	R
0	TCEN	Counter enable control. 0: Timer stop 1: Timer running	RW

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16.2.3 Watchdog Timer Data Register (TDR)

The watchdog timer data register TDR is used to store the data to be compared with the content of the watchdog timer up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

TDR																0x10002000
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDR															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

16.2.4 Watchdog Timer Counter (TCNT)

The watchdog timer counter (TCNT) is a 16-bit read/write counter. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDR, the comparison match signal will be generated and a WDT reset is generated. The data can be read out at any time. The counter data can be written at any time. (Default: indeterminate)

TCNT																0x10002008
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

16.3 Watchdog Timer Function

The following describes steps of using WDT:

1 Setting the PRESCALE of input clock in register TCSR.
2 Set register TDR and TCNT.
3 Select the input clock and enable the input clock in register TCSR.

After initialize the register of timer, we should start the counter as follows:

4 Set TCEN bit in TCER to 1. The counter TCNT begins to count.
5 If TCNT = TDR, a WDT reset will be generated.

NOTES:

1 The input clock and PCLK should follow the rules advanced before.
2 The clock of WDT can be stopped by setting register TSR, and register TSR can only be set by register TSSR or TSCR. The content of register TSR, TSSR and TSCR can be found in TCU spec.

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17 LCD Controller

17.1 Overview

The JZ integrated LCD controller has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller. Temporal dithering (frame rate modulation) is supported for STN LCD panels. And OSD is also supported for LCD controller.

Features:

- Basic Features
  - Support PAL/NTSC TV out. 3-components (YUV) TV out (refer TVE spec). VGA
  - Support CCIR601/656 data format
  - Single and Dual panel displays in STN mode
  - Single panel displays in TFT mode
  - Display size up to 1280x720@60Hz(BPP24)
  - Internal palette RAM 256x16 bits

- Colors Supports
  - Encoded pixel data of 1, 2, 4, 8 or 16 BPP in STN mode
  - Support 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - Encoded pixel data of 1, 2, 4, 8, 16, 18 or 24 BPP in TFT mode
  - Support 65,536(65K), 262,144(260K) and up to 16,777,216 (16M) colors in TFT mode

- Panel Supports
  - Support single STN panel and dual STN panel with 1, 2, 4, 8 data output pins
  - Support 16-bit parallel TFT panel
  - Support 18-bit parallel TFT panel
  - Support 24-bit serial TFT panel with 8 data output pins
  - Support 24-bit parallel TFT panel
  - Support Delta RGB panel

- OSD Supports
  - Supports one single color background
  - Supports two foregrounds, and every size can be set for each foreground
  - Supports one transparency for the whole graphic
  - Supports one transparency for each pixel in one graphic
  - Supports color key and mask color key

- Decompressor

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- Support bpp16 compressed data
- Support bpp24 compressed data with alpha
- Support bpp24 compressed data without alpha

17.2 Pin Description

Table 17-1 LCD Controller Pins Description

Name	I/O	Description
Lcd_pclk	Input/Output	Display device pixel clock
Lcd_vsync	Input/Output	Display device vertical synchronize pulse
Lcd_hsync	Input/Output	Display device horizontal synchronize pulse
Lcd_de	Output	Display device is STN: AC BIAS Pin Display device is NOT STN: data enable Pin
Lcd_d[17:0]	Output	Display device data pins
lcd_lo6_o[5:0]	Output	Display device data pins use in 24 bit parallel mode.
Lcd_spl*[1]	Output	Programmable special pin for generating control signals
Lcd_cls*[1]	Output	Programmable special pin for generating control signals
Lcd_ps*[1]	Output	Programmable special pin for generating control signals
Lcd_rev*[1]	Output	Programmable special pin for generating control signals

NOTE: The mode and timing of special pin Lcd_spl, Lcd_cls, Lcd_ps and Lcd_rev can be seen in **part 1.7 LCD Controller Pin Mapping.**

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17.3 Block Diagram

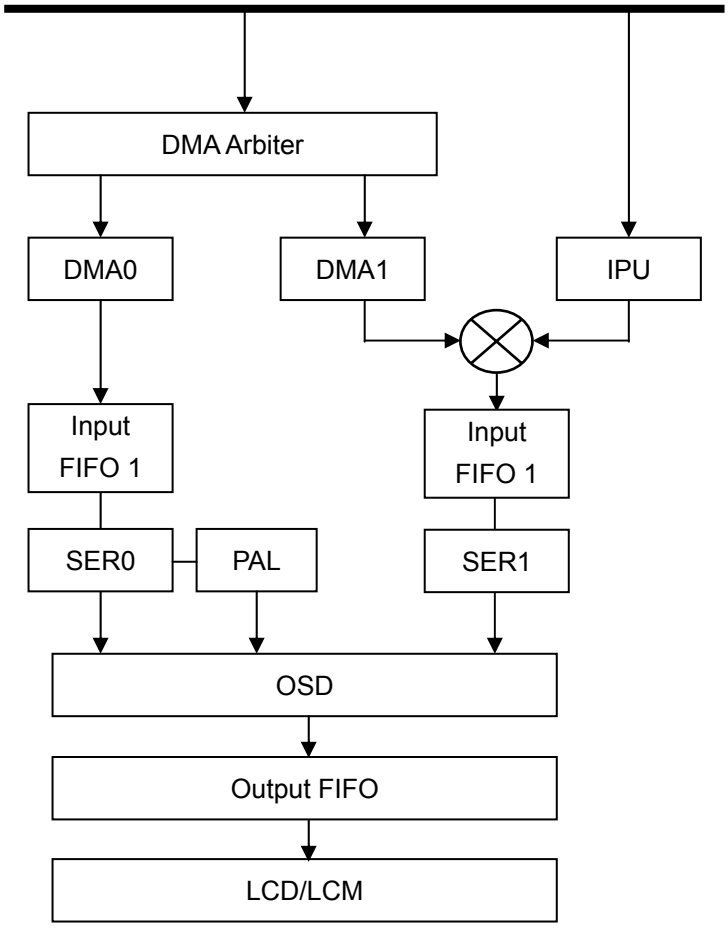


Figure 17-1 Block Diagram when use OSD mode

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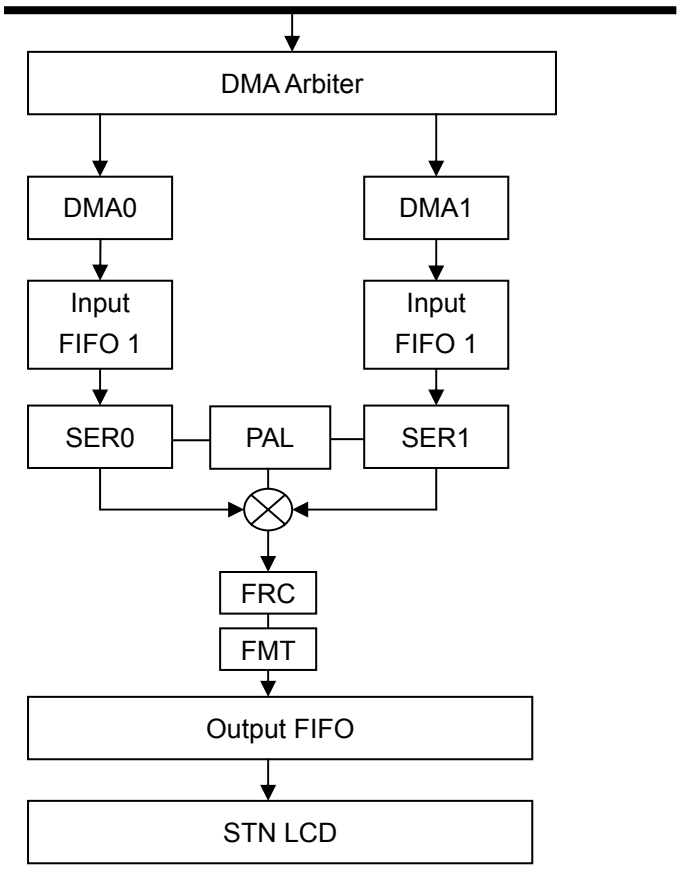


Figure 17-2 Block Diagram of STN mode (not use OSD)

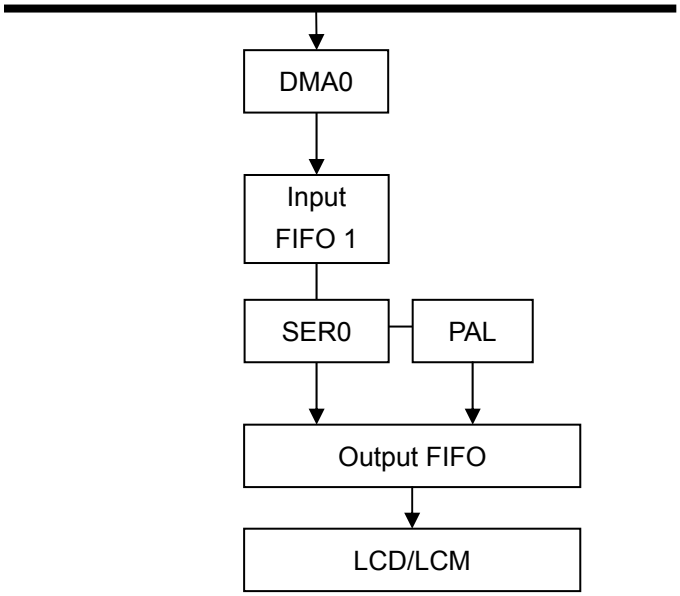


Figure 17-3 Block Diagram of TFT mode (not use OSD)

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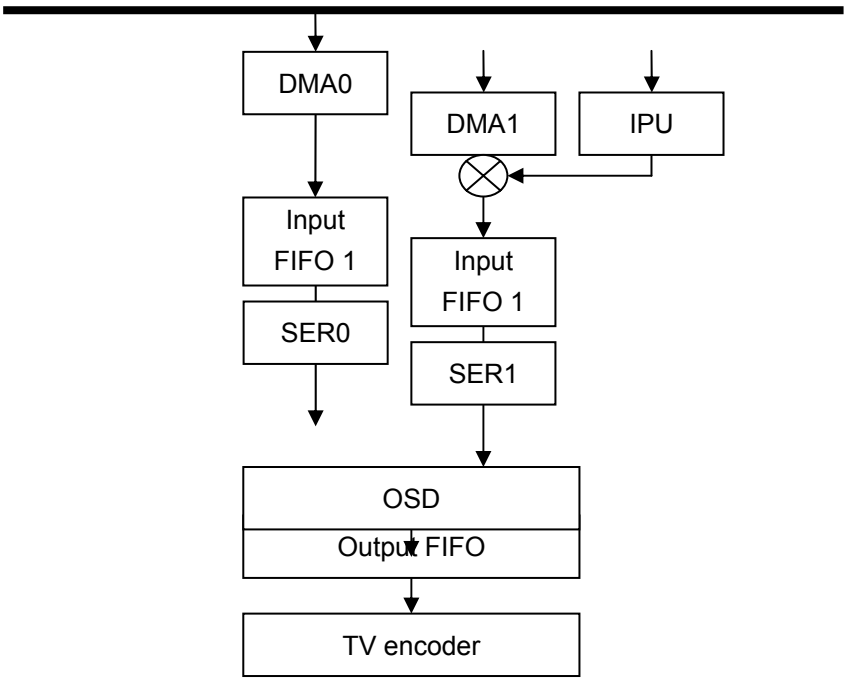


Figure 17-4 Block Diagram of TV interface

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17.4 LCD Display Timing

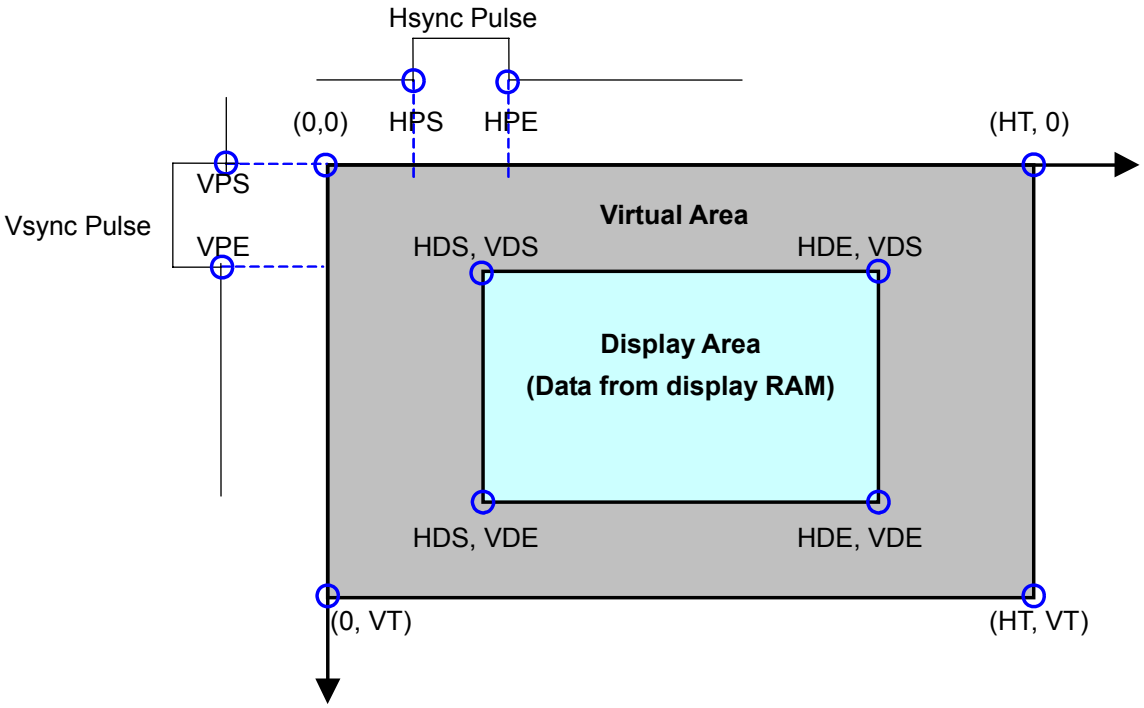


Figure 17-5 Display Parameters

NOTES:

1 VPS === 0
VSYNC pulse always start at point (0,0)

2 H: Horizontal V: Vertical T: Total
D: Display Area P: Pulse
S: Start point E: End point

In the (H, V) Coordinates:

1 The gray rectangle (0, 0) to (HT, VT) is “Virtual Area”.
2 The blue rectangle (HDS, VDS) to (HDE, VDE) is “Display Area”.
3 VPS, VPE defines the VSYNC signal timing. (VPS always be zero)
4 HPS, HPE defines the HSYNC signal timing.

All timing parameters start with “H” is measured in lcd_pclk ticks.
All timing parameters start with “V” is measured in lcd_hsync ticks.

This diagram describes the general LCD panel parameters, these can be set via the registers that describes in next section.

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17.5 TV Encoder Timing

Some of Video Encoders for TV (Tele Vision) require interlaced timing interface.

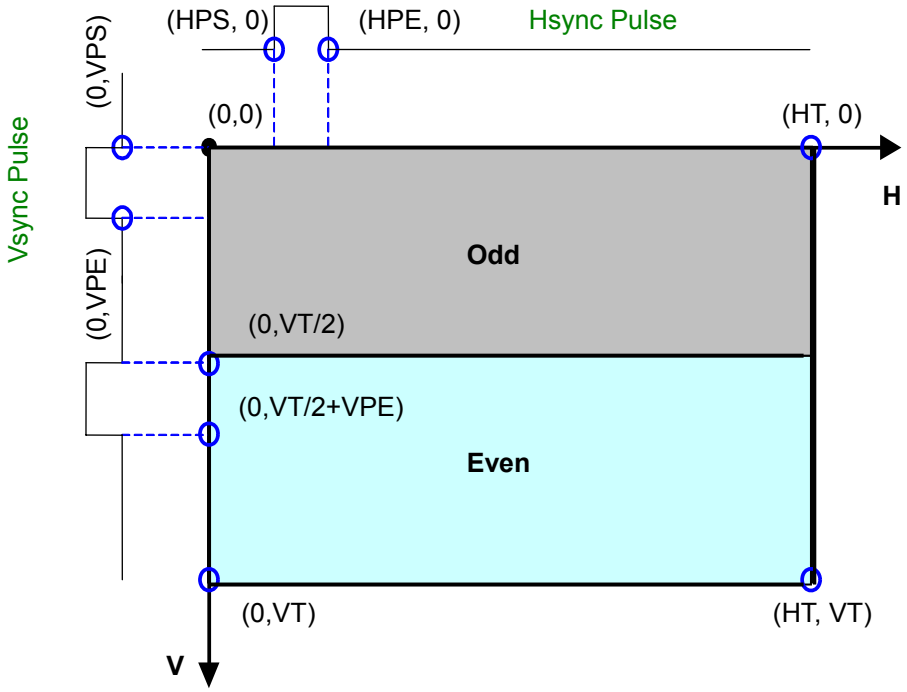


Figure 17-6 TV-Encoder Display Parameters

NOTES:

1 Even Field contains one more blank line.
e.g. For standard PAL timing, Odd filed has 312 lines while even field has 313 lines.

2 Interlace mode generate 2 vsync pulse for each field. The second vsync start at (VT/2), end at (VT/2 + VPE).

3 Display Area & Virtual Area has the same size. VDS=HDS=0, VDE=VT, HDE=HT.

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17.6 OSD Graphic

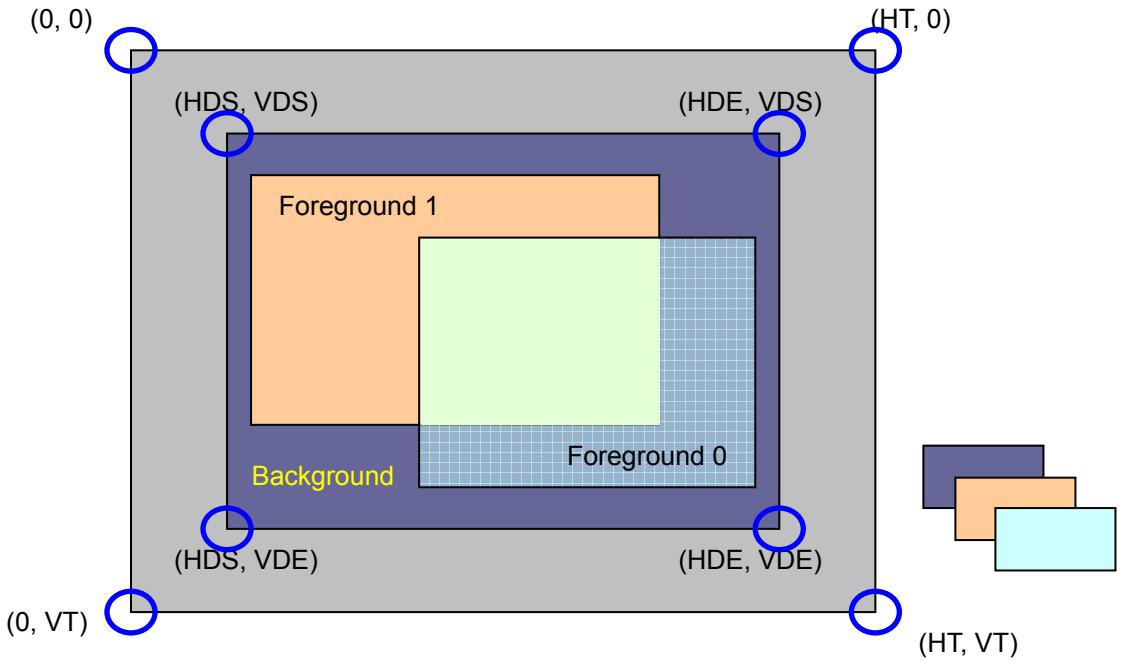


Figure 17-7 OSD Graphic

NOTES:

1 Background is one single color and the size is the full screen.
2 The size of foregrounds can be every size smaller than background.
3 The order of the graphic is as follows:
   a Top layer: Foreground 0.
   b Middle layer: Foreground 1.
   c Bottom layer: Background.

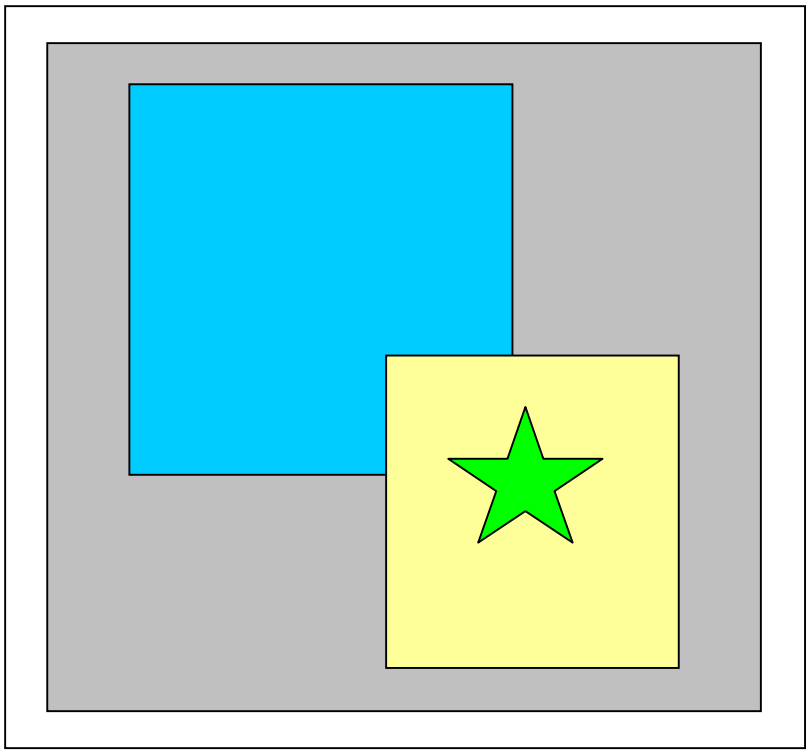
17.6.1 Color Key

This function gives user a method to implement irregular display window. User can make foreground 0 and foreground 1 to different shape. The color key has two implements mode that called color key and mask color key.

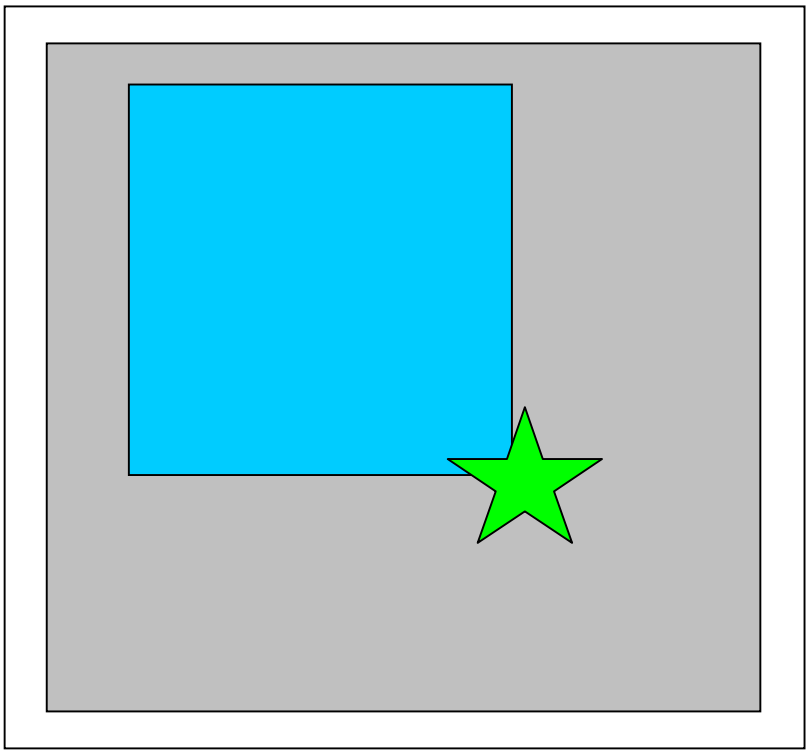
Color Key mode is meant to mask a chosen color and show others.

Mask Color Key mode is meant to only show a chosen color and mask others.

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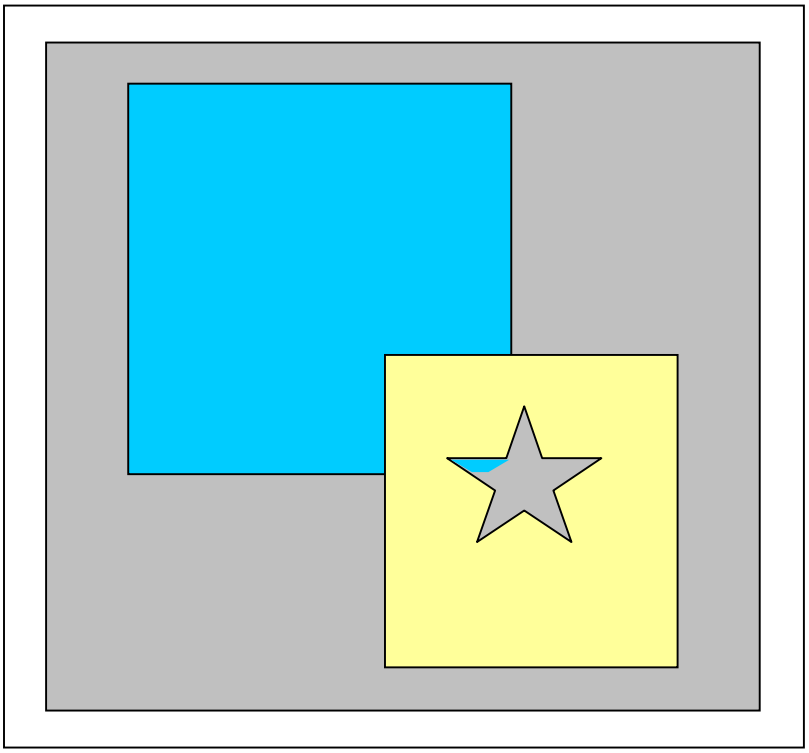


Not use color key function



Color key mode

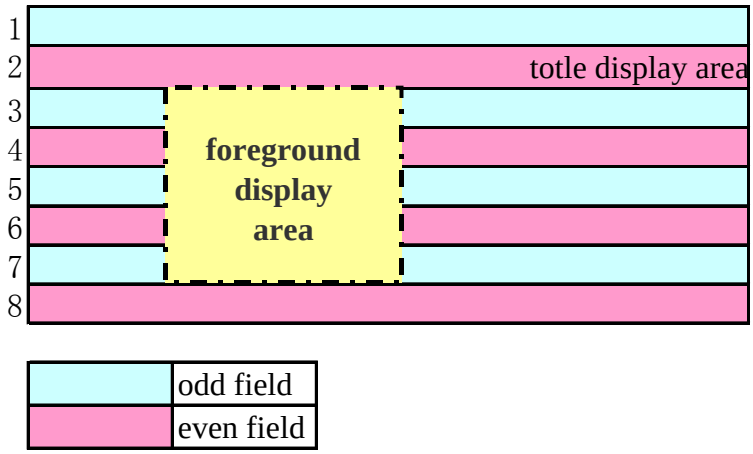
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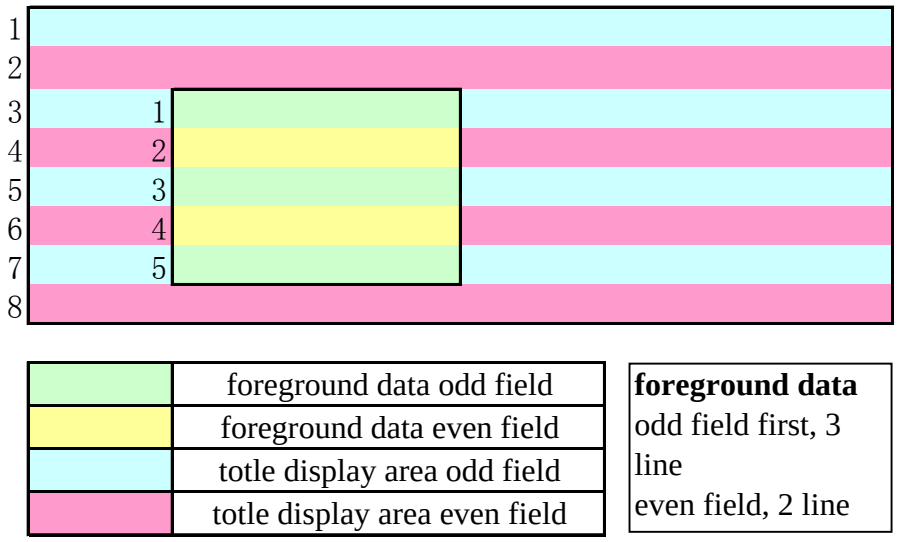
Mask color key mode

17.7 TV Graphic

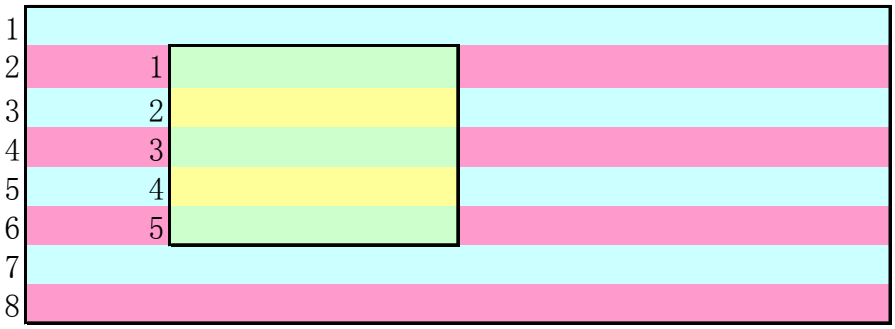
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17.7.1 Different Display Field

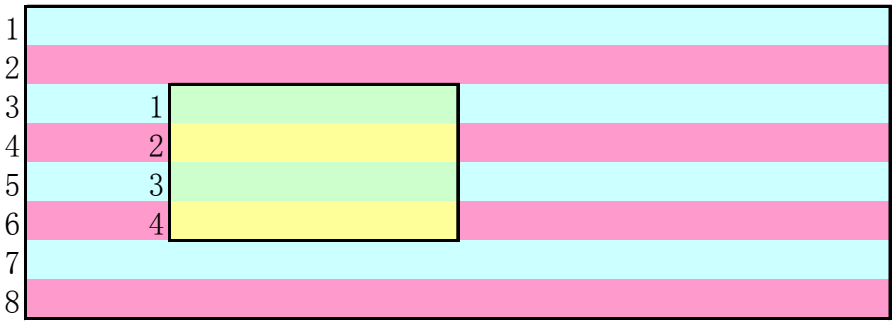


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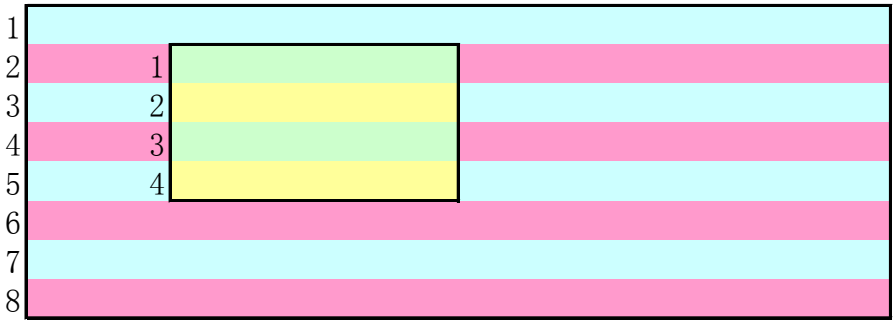
	foreground data odd field
	foreground data even field
	totle display area odd field
	totle display area even field

foreground data
even field first, 2 line
odd field, 3 line



	foreground data odd field
	foreground data even field
	totle display area odd field
	totle display area even field

foreground data
odd field first, 2 line
even field, 2 line



	foreground data odd field
	foreground data even field
	totle display area odd field
	totle display area even field

foreground data
even field first, 2 line
odd field, 2 line

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17.8 Register Description

Table 17-2 LCD Controller Registers Description

Name	RW	Reset Value	Address	Access Size
LCDCFG	RW	0x00000000	0x13050000	32
LCDCTRL	RW	0x00000000	0x13050030	32
LCDSTATE	RW	0x00000000	0x13050034	32
LCDOSDC	RW	0x0000	0x13050100	16
LCDOSDCTRL	RW	0x0000	0x13050104	16
LCDOSDS	RW	0x0000	0x13050108	16
LCDBGC	RW	0x00000000	0x1305010C	32
LCDKEY0	RW	0x00000000	0x13050110	32
LCDKEY1	RW	0x00000000	0x13050114	32
LCDALPHA	RW	0x00	0x13050118	8
LCDIPUR	RW	0x00000000	0x1305011C	32
LCDRGBC	RW	0x0000	0x13050090	16
LCDVAT	RW	0x00000000	0x1305000C	32
LCDDAH	RW	0x00000000	0x13050010	32
LCDDAV	RW	0x00000000	0x13050014	32
LCDXYP0	RW	0x00000000	0x13050120	32
LCDXYP0_PART2	RW	0x00000000	0x130501F0	32
LCDXYP1	RW	0x00000000	0x13050124	32
LCDSIZE0	RW	0x00000000	0x13050128	32
LCDSIZE0_PART2	RW	0x00000000	0x130501F4	32
LCDSIZE1	RW	0x00000000	0x1305012C	32
LCDVSYNC	RW	0x00000000	0x13050004	32
LCDHSYNC	RW	0x00000000	0x13050008	32
LCDPS[*1]	RW	0x00000000	0x13050018	32
LCDCLS[*1]	RW	0x00000000	0x1305001C	32
LCDSPL[*1]	RW	0x00000000	0x13050020	32
LCDREV[*1]	RW	0x00000000	0x13050024	32
LCDIID	R	0x00000000	0x13050038	32
LCDDA0	RW	0x00000000	0x13050040	32
LCDSA0	R	0x00000000	0x13050044	32
LCDFID0	R	0x00000000	0x13050048	32
LCDCMD0	R	0x00000000	0x1305004C	32
LCDOFFS0	R	0x00000000	0x13050060	32
LCDPW0	R	0x00000000	0x13050064	32
LCDCNUM0	R	0x00000000	0x13050068	32
LCDDESSIZE0	R	0x00000000	0x1305006C	32

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LCDDA1[*2]	RW	0x00000000	0x13050050	32
LCDSA1[*2]	R	0x00000000	0x13050054	32
LCDFID1[*2]	R	0x00000000	0x13050058	32
LCDCMD1[*2]	R	0x00000000	0x1305005C	32
LCDOFFS1[*2]	R	0x00000000	0x13050070	32
LCDPW1[*2]	R	0x00000000	0x13050074	32
LCDCNUM1[*2]	R	0x00000000	0x13050078	32
LCDDESSIZE1[*2]	R	0x00000000	0x1305007C	32
LCDDA0_PART2	RW	0x00000000	0x130501C0	32
LCDSA0_PART2	R	0x00000000	0x130501C4	32
LCDFID0_PART2	R	0x00000000	0x130501C8	32
LCDCMD0_PART2	R	0x00000000	0x130501CC	32
LCDOFFS0_PART2	R	0x00000000	0x130501E0	32
LCDPW_PART2	R	0x00000000	0x130501E4	32
LCDCNUM0_PART2	R	0x00000000	0x130501E8	32
LCDDESSIZE0_PART2	R	0x00000000	0x130501EC	32
LCDPCFG	RW	0x00000000	0x130502C0	32

NOTES:

1 *[1]: These registers are only used for SPECIAL TFT panels.

2 *[2]: These registers are only used for Dual Panel STN panels and use DMA channel 1 in OSD mode for TFT panels.

17.8.1 Configure Register (LCDCFG)

LCDCFG **0x13050000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCDPIN	TVEPEH		NEWDES	PALBP	TVEN	RECOVER	DITHER	PSM	CLSM	SPLM	REVM	HSYNM	PCLKM	INVDAT	SYNDIR	PSP	CLSP	SPLP	REVP	HSP	PCP	DEP	VSP	18/16	24	PDW	MODE				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	LCDPIN[*1]	LCD PIN Select bit. It is used to choose the function of LCD PINS or SLCD PINS. The function of pins is as follows. **LCDPIN** / **PIN SELECT** 0 / LCD PIN 1 / SLCD PIN	RW
30	TVEPEH	TVE PAL enable extra_halfline signal.	RW

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29		**KEEP THIS BIT TO 0.**	RW
28	NEWDES	indicate use new 8 words descriptor or not. 0: use old 4 words descriptor 1: use new 8 words descriptor (add LCDOFFSx, LCDPWx, LCDCUNMx, LCDDESSIZEx) OSD mode use 8 word descriptor.	RW
27	PALBP	Indicate bypass pal in BPP8, and in OSD mode, set this bit to 1 is also bypass data format and alpha blending. 0: use PAL; 1: not use PAL.	RW
26	TVEN	Indicate the terminal is LCD panel or TV.	RW
25	RECOVER	Auto recover when output FIFO under run. 0: disable; 1: enable.	RW
24	DITHER	Dither function. (use when 24bpp data output to a 18/16bit panel) 0: disable; 1: enable. Dither function use to make the picture misty, when you show a static picture with few color, strongly recommend you not use it. When you use this function both static and dynamic picture, strongly recommend you to set the static picture with 16/18BPP color.	RW
23	PSM	PS signal mode bit. 0: enabled; 1: disabled.	RW
22	CLSM	CLS signal mode bit. 0: enabled; 1: disabled.	RW
21	SPLM	SPL signal mode bit. 0: enabled; 1: disabled.	RW
20	REVM	REV signal mode bit. 0: enabled; 1: disabled.	RW
19	HSYNM	H-Sync signal polarity choice function. 0: enabled; 1: disabled.	RW
18	PCLKM	Dot clock signal polarity choice function. 0: enabled; 1: disabled.	RW
17	INVDAT	Inverse output data. 0: normal; 1: inverse.	RW
16	SYNDIR	V-Sync and H-Sync direction. 0: output; 1: input.	RW
15	PSP	PS pin reset state.	RW
14	CLSP	CLS pin reset state.	RW
13	SPLP	SPL pin reset state.	RW
12	REVP	REV pin reset state.	RW
11	HSP	H-Sync polarity. 0: active high; 1: active low.	RW
10	PCP	Pix-clock polarity. 0: data translations at rising edge 1: data translations at falling edge	RW
9	DEP	Data Enable polarity. 0: active high; 1: active low.	RW
8	VSP	V-Sync polarity. 0: leading edge is rising edge 1: leading edge is falling edge	RW
7	18/16	18-bit TFT Panel or 16-bit TFT Panel. This bit will be available when MODE [3:2] is equal to 0 and 24[6] is equal to 0. 0: 16-bit TFT Panel 1: 18-bit TFT Panel	RW
6	24	Set this bit to 1 for 24-bit TFT Panel.	RW

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5:4	PDW	STN pins utilization. **Signal Panel** 00 Lcd_d[0] 01 Lcd_d[0:1] 10 Lcd_d[0:3] 11 Lcd_d[0:7] **Dual-Monochrome Panel** 00 Reserved 01 Reserved 10 Upper panel: lcd_d[3:0], lower panel: lcd_d[11:8] 11 Upper panel: lcd_d[7:0], lower panel: lcd_d[15:8]	RW
3:0	MODE	Display Device Mode Select/Output mode. **LCD Panel** 0000 Generic 16-bit/18-bit Parallel TFT Panel 0001 Special TFT Panel Mode1 0010 Special TFT Panel Mode2 0011 Special TFT Panel Mode3 0100 Non-Interlaced TV out 0101 Reserved 0110 Interlaced TV out 0111 Reserved 1000 Single-Color STN Panel 1001 Single-Monochrome STN Panel 1010 Dual-Color STN Panel 1011 Dual-Monochrome STN Panel 1100 8-bit Serial TFT 1101 LCM 1110 Reserved 1111 Reserved	RW

NOTES:

*1:

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1	SLCD CLK	SLCD CS	SLCD RS	--	--	--	--	--	SLCD D [17:0]

1 The direction of PIN25 is set by register LPCDR.LCS in CPM SPEC.

2 The direction of PIN23 and PIN23 are set by register LCDCFG.SYNDIR.

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17.8.2 Control Register (LCDCTRL)

LCDCTRL **0x13050030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINMD	BST			RGB	OFUP	FRC		PDD									DACTE	EOFM	SOFM	OFUM	IFUM0	IFUM1	LDDM	QDM	BEDN	PEDN	DIS	ENA	BPP		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PINMD	This register set Pin distribution in 16-bit parallel mode. 0: 16-bit data correspond with LCD_D[15:0] 1: 16-bit data correspond with LCD_D[17:10], LCD_D[8:1]	RW
30:28	BST	Burst Length Selection. 000: 4 word 001: 8 word 010: 16 word 011: 32 word 101: Contiue16 100: 64 word	RW
27	RGB	Bpp16 RGB mode. 0: RGB565; 1: RGB555. In OSD mode, this bit configure the foreground 0. If use parallel 18 bit，set this bit to 0.	RW
26	OFUP	Output FIFO under run protection. 0: disable; 1: enable.	RW
25:24	FRC	STN FRC Algorithm Selection. 00: 16 grayscale 01: 4 grayscale 10: 2 grayscale 11: Reserved	RW
23:16	PDD	Load Palette Delay Counter.	RW
15		keep this bit to 0.	
14	DACTE	DAC loop back test.	RW
13	EOFM	Mask end of frame interrupt. 0: INT-disabled; 1: INT-enabled.	RW
12	SOFM	Mask start of frame interrupt. 0: INT-disabled; 1: INT-enabled.	RW
11	OFUM	Mask out FIFO under run interrupt. 0: INT-disabled;1: INT-enabled.	RW
10	IFUM0	Mask in FIFO 0 under run interrupt. 0: INT-disabled; 1: INT-enabled.	RW
9	IFUM1	Mask in FIFO 1 under run interrupt. 0: INT-disabled; 1: INT-enabled.	RW
8	LDDM	Mask LCD disable done interrupt. 0: INT-disabled; 1: INT-enabled.	RW
7	QDM	Mask LCD quick disable done interrupt. 0: INT-disabled; 1: INT-enabled.	RW

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6	BEDN	Endian selection. 0: same as system Endian; 1: reverse endian format.	RW
5	PEDN	Endian in byte. 0: msb first; 1: lsb first.	RW
4	DIS	Disable controller indicate bit. 0: enable; 1: in disabling or disabled.	RW
3	ENA	Enable controller. 0: disable; 1: enable.	W
2:0	BPP	Bits Per Pixel. In OSD mode, those bits configure the foreground 0.	RW

	Bits Per Pixel
000	1bpp
001	2bpp
010	4bpp
011	8bpp
100	15/16bpp
101	18bpp/24bpp
110	24bpp compressed
111	30bpp

17.8.3 Status Register (LCDSTATE)

LCDSTATE 0x13050034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								QD	Reserved	EOF	SOF	OUF	IFU0	IFU1	LDD
RST	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	QD	LCD Quick disable. 0: not been quick disabled; 1: quick disabled done.	RW
6	Reserved	Writing has no effect, read as zero.	R
5	EOF	End of Frame indicate bit.	RW
4	SOF	Start of Frame indicate bit.	RW
3	OUF	Out FIFO under run.	RW
2	IFU0	In FIFO 0 under run.	RW
1	IFU1	In FIFO 1 under run.	RW
0	LDD	LCD disable. 0: not been normal disabled; 1: been normal disabled.	RW

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17.8.4 OSD Configure Register (LCDOSDC)

LCDOSDC **0x13050100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOFM1	EOFM1	Reserved	OSDIV	SOFM0	EOFM0	Reserved					F1EN	F0EN	ALPHAEN	ALPHAMD	OSDEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	SOFM1	Start of frame interrupt mask for foreground 1.	RW
14	EOFM1	End of frame interrupt mask for foreground 1.	RW
13	Reserved	Writing has no effect, read as zero.	R
12	OSDIV	Not supported in this release.	RW
11	SOFM0	Start of frame interrupt mask for foreground 0.	RW
10	EOFM0	End of frame interrupt mask for foreground 0.	RW
9:5	Reserved	Writing has no effect, read as zero.	R
4	F1EN	1: Foreground 1 is enabled 0: Foreground 1 is disabled	RW
3	F0EN	1: Foreground 0 is enabled 0: Foreground 0 is disabled. *When use slcd, F0EN must set 1.	RW
2	ALPHAEN	0: Alpha blending is disabled; 1: Alpha blending is enabled.	RW
1	ALPHAMD	Alpha blending mode. 0: One transparency for the whole graphic, and the LCDALPHA register is used for transparency 1: One transparency for each pixel in one graphic, and the alpha value is coming from each pixel data	RW
0	OSDEN	OSD mod enable. 1: enabled. And you can use F0 F1 0: disabled	RW

17.8.5 OSD Control Register (LCDOSDCTRL)

LCDOSDCTRL **0x13050104**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPU	Reserved										RGB	CHANGES	OSDBPP		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
15	IPU	Indicate use IPU or DMA channel 1 to transport data to FIFO 1. This bit is only use in OSD mode. 0: use DMA channel 1 1: use IPU	RW
13:5	Reserved	Writing has no effect, read as zero.	R
4	OSDRGB	Bpp16 RGB mode. 0: RGB565; 1: RGB555. This bit only use in OSD mode to configure foreground 1.	RW
3	CHANGES	Change configure flag, when software need change the foreground0 and foreground1's enable/position/size, it need set this bit to 1. When hardware finishes the change, It will clear this bit to 0. DO NOT set this bit when you needed change size or position. AND make sure the reconfigure value is different to the old one. Only one of these (F0's position, F1's position, F0's size, F1's size) could be change in one time. Refer to 17.8.6.	RW
2:0	OSDBPP	Bits Per Pixel of OSD channel 1.(this channel cannot use palette) 000 Reserved 001 Reserved 010 Reserved 011 Reserved 100 15/16bpp 101 18bpp/24bpp 110 24bpp compressed 111 30bpp Those bits only use in OSD mode to configure display window 1.	RW

17.8.6 OSD State Register (LCDOSDS)

LCDOSDS **0x13050108**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOF1	EOF1	Reserved		SOF0	EOF0	Reserved									READY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	SOF1	Start of frame flag for foreground 1.	RW
14	EOF1	End of frame flag for foreground 1.	RW
13:12	Reserved	Writing has no effect, read as zero.	R
11	SOF0	Start of frame flag for foreground 0.	RW

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10	EOF0	End of frame flag for foreground 0.	RW
9:1	Reserved	Writing has no effect, read as zero.	R
0	READY	Ready for accept the change. When this bit set 1, the software can change the descriptor's LCDDESSIZE0, 1 to change the foreground size. This bit will clear by hardware when the change is finished.	R

17.8.7 Background Color Register (LCDBGC)

LCDBGC **0x1305010C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Red [7:0]								Green [7:0]								Blue [7:0]							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
23:16	Red	Red part or Y part of background.	RW
15:8	Green	Green part or Cb part of background.	RW
7:0	Blue	Blue part or Cr part of background.	RW

17.8.8 Foreground Color Key Register 0 (LCDKEY0)

LCDKEY0 **0x13050110**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEYEN	KEYMD	Reserved						Red [7:0]								Green [7:0]								Blue [7:0]							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	KEYEN	The enable bit of color key for foreground 0.	RW
30	KEYMD	Color key mod. 0: color key; 1: mask color key.	RW
29:27	Reserved	Writing has no effect, read as zero.	R
23:16	Red	Red part of color key for foreground 0.	RW
15:8	Green	Green part of color key for foreground 0.	RW
7:0	Blue	Blue part of color key for foreground 0.	RW

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17.8.9 Foreground Color Key Register 1 (LCDKEY1)

LCDKEY1 **0x13050114**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEYEN	KEYMD	Reserved						Red [7:0]								Green [7:0]								Blue [7:0]							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	KEYEN	The enable bit of color key for foreground 1.	RW
30	KEYMD	Color key mod. 0: color key; 1: mask color key.	RW
29:27	Reserved	Writing has no effect, read as zero.	R
23:16	Red	Red part of color key for foreground 1.	RW
15:8	Green	Green part of color key for foreground 1.	RW
7:0	Blue	Blue part of color key for foreground 1.	RW

17.8.10 ALPHA Register (LCDALPHA)

LCDALPHA **0x13050118**

Bit	7	6	5	4	3	2	1	0
	ALPHA [7:0]							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	ALPHA	The alpha value for one graphic with one transparency.	RW

The formula of alpha blending is as follows:

$$NewPixel = \frac{\left[(256 - Alpha) * (Foreground1\_or\_background) + Alpha * Froeground0 + 128\right]}{256}$$

Note that foreground 1 must be overlay background.

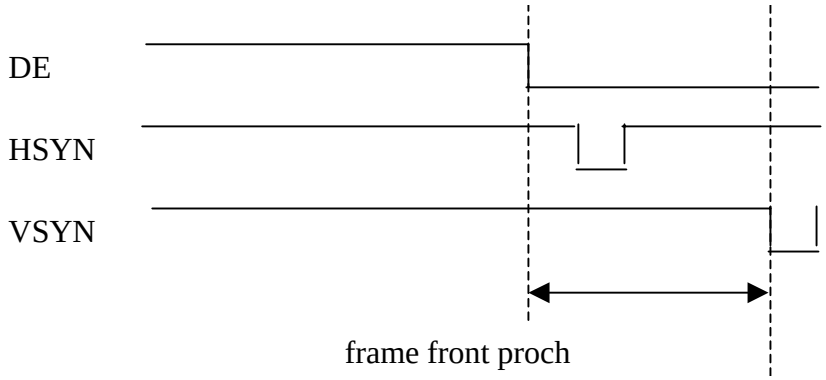
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17.8.11 IPU Restart (LCDIPUR)

LCDIPUR **0x1305011C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPUREN	Reserved							IPUR																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	IPUREN	IPU restart function enable. 0:disable; 1:enable.	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23:0	IPUR	This register is indicating when one frame is end, how long the panel can wait for the next frame data from IPU. In common, set this number larger than frame front porch and near to ((HT-0) X (VPE-VPS))/3. This signal only use when foreground1 work in IPU mode. Trigger IPU transfer the last frame again to avoid output FIFO under run.	RW



17.8.12 RGB Control (LCDRGBC)

LCDRGBC **0x13050090**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RGBDM	DMM	Reserved					YCC	Reserved	OddRGB			Reserved	EvenRGB		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	RGBDM	RGB with dummy data enable. Only useful for RGB serial mode. If this bit set to 1, the one pixel	RW

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<table>
<tr><td></td><td></td><td>include 4 clock periods, that Red, Green, Blue and Dummy data. Dummy is equal to 0.
0: Disable; 1: Enable.</td><td></td></tr>
<tr><td>14</td><td>DMM</td><td>RGB dummy mode.
0: R-G-B-Dummy; 1: Dummy-R-G-B.</td><td></td></tr>
<tr><td>13:9</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>RW</td></tr>
<tr><td>8</td><td>YCC</td><td>Change RGB to YCbCr.
0: not change; 1: change to YUV.
This bit only use in OSD mode. Change RGB data to YCbYCr and sent to TV encoder.
Please notice that the data will be translated as 16 bits parallel. And only half of it will be transfer. (YCb or YCr in one pixel). If you not use OSD mode and TV encoder, please set this bit to 0.
When use this function with IPU transfer data to an interlaced TV, please set IPU output as RGB 888, and OSDBPP to 24. or IPU output data as PACKAGE(YCbYCr) and OSDBPP to 16.</td><td>RW</td></tr>
<tr><td>7</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>RW</td></tr>
<tr><td>6:4</td><td>OddRGB</td><td>Odd line serial RGB data arrangement, useful for RGB serial mode only. *Please notice that you must set 000 when use 16/18parallel mode.
<table>
<tr><th></th><th>RGB mode</th></tr>
<tr><td>000</td><td>RGB</td></tr>
<tr><td>001</td><td>RBG</td></tr>
<tr><td>010</td><td>GRB</td></tr>
<tr><td>011</td><td>GBR</td></tr>
<tr><td>100</td><td>BRG</td></tr>
<tr><td>101</td><td>BGR</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>RW</td></tr>
<tr><td>2:0</td><td>EvenRGB</td><td>Even line serial RGB data arrangement, useful for RGB serial mode only. *Please notice that you must set 000 when use 16/18parallel mode.
<table>
<tr><th></th><th>RGB mode</th></tr>
<tr><td>000</td><td>RGB</td></tr>
<tr><td>001</td><td>RBG</td></tr>
<tr><td>010</td><td>GRB</td></tr>
<tr><td>011</td><td>GBR</td></tr>
<tr><td>100</td><td>BRG</td></tr>
<tr><td>101</td><td>BGR</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
</table>

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17.8.13 Virtual Area Setting (LCDVAT)

LCDVAT **0x1305000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HT												Reserved				VT											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HT	Horizontal Total size. (in dot clock, sum of display area and blank space)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VT	Vertical Total size. (in line clock, sum of display area and blank space)	RW

17.8.14 Display Area Horizontal Start/End Point (LCDDAH)

LCDDAH **0x13050010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HDS												Reserved				HDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HDS	Horizontal display area start. (in dot clock)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HDE	Horizontal display area end. (in dot clock)	RW

17.8.15 Display Area Vertical Start/End Point (LCDDAV)

LCDDAV **0x13050014**

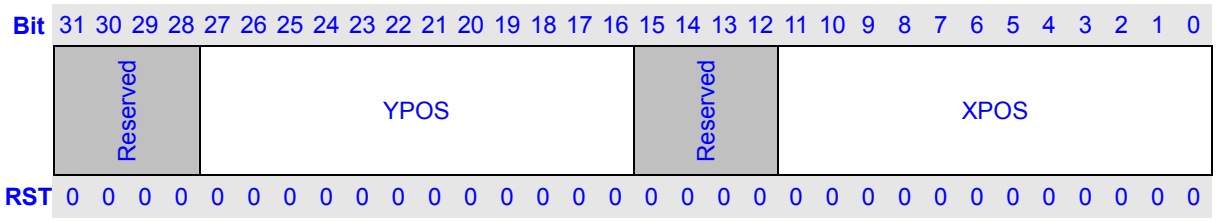
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				VDS												Reserved				VDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VDS	Vertical display area start position. (in line clock)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDE	Vertical display area end position. (in line clock)	RW

17.8.16 Foreground 0 XY Position Register (LCDXYP0)

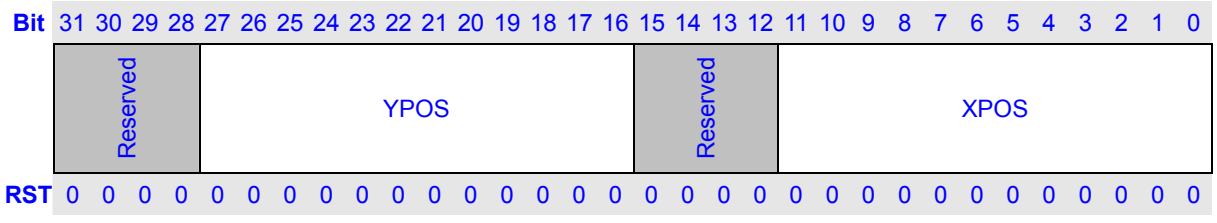
LCDXYP0 **0x13050120**



Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	YPOS	The Y position of top-left part for foreground 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	XPOS	The X position of top-left part for foreground 0.	RW

17.8.17 Foreground 0 PART2 XY Position Register (LCDXYP0_PART2)

LCDXYP0_PART2 **0x130501F0**



Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	YPOS	The Y position of top-left part for foreground 0 PART2.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	XPOS	The X position of top-left part for foreground 0 PART2.	RW

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17.8.18 Foreground 1 XY Position Register (LCDXYP1)

LCDXYP1 **0x13050124**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				YPOS												Reserved				XPOS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	YPOS	The Y position of top-left part for foreground 1.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	XPOS	The X position of top-left part for foreground 1.	RW

17.8.19 Foreground 0 Size Register (LCDSIZE0)

LCDSIZE0 **0x13050128**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Height												Reserved				Width											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	Height	The height of foreground 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	Width	The width of foreground 0.	RW

When use TVE interlaced mode, please set the area of F0 and F1 aligned with BST.

17.8.20 Foreground 0 PART2 Size Register (LCDSIZE0_PART2)

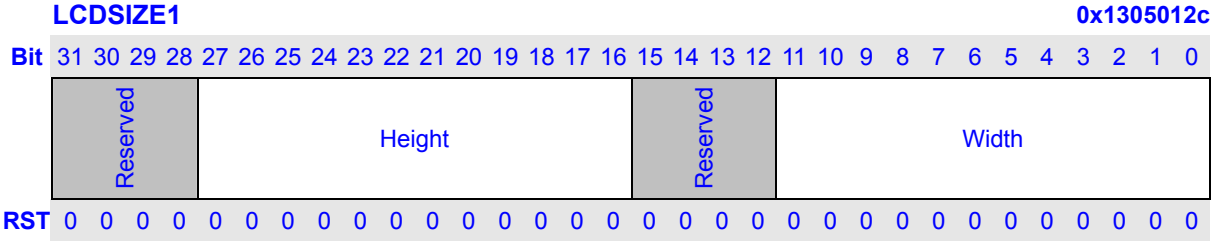
LCDSIZE0_PART2 **0x130501F4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Height												Reserved				Width											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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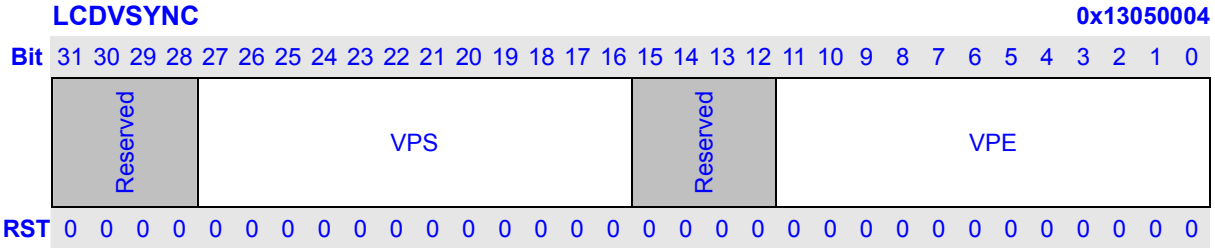
Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	Height	The height of foreground 0 PART2.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	Width	The width of foreground 0 PART2.	RW

17.8.21 Foreground 1 Size Register (LCDSIZE1)



Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	Height	The height of foreground 1.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	Width	The width of foreground 1.	RW

17.8.22 Vertical Synchronize Register (LCDVSYNC)



Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VPS	V-Sync Pulse start position, fixed to 0. (in line clock)	R
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VPE	V-Sync Pulse end position. (in line clock)	RW

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17.8.23 Horizontal Synchronize Register (LCDHSYNC)

LCDHSYNC **0x13050008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HPS												Reserved				HPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HPS	H-Sync pulse start position. (in dot clock)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HPE	H-Sync pulse end position. (in dot clock)	RW

17.8.24 PS Signal Setting (LCDPS)

LCDPS **0x13050018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PSS												Reserved				PSE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PSS	PS signal start position. (in dot clock) In STN mode, PS signal is ignored. But this register is used to define the AC BIAS signal. AC BIAS signal will toggle very N lines per frame. PSS defines the Toggle position.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PSE	PS signal end position. (in dot clock) In STN mode, PSE defines N, which described in PSS.	RW

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17.8.25 CLS Signal Setting (LCDCLS)

LCDCLS **0x1305001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				CLSS												Reserved				CLSE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	CLSS	CLS signal start position. (in dot clock)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	CLSE	CLS signal end position. (in dot clock)	RW

17.8.26 SPL Signal Setting (LCDSPL)

LCDSPL **0x13050020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SPLS												Reserved				SPLE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	SPLS	SPL signal start position. (in dot clock)	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	SPLE	SPL signal end position. (in dot clock)	RW

* In test mode this register use to keep TV encoder module's output data: comp_luma([25:16]) and chroma([9:0]).

17.8.27 REV Signal Setting (LCDREV)

LCDREV **0x13050024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				REVS												Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	REVS	REV signal start position. (in dot clock)	RW
15:0	Reserved	Writing has no effect, read as zero.	R

17.8.28 Interrupt ID Register (LCDIID)

LCDIID is a read-only register that contains a copy of the Frame ID register (LCDFID) from the descriptor currently being processed when a start of frame (SOF) or end of frame (EOF) interrupt is generated. LCDIID is written to only when an unmasked interrupt of the above type is signaled and there are no other unmasked interrupts in the LCD controller pending. As such, the register is considered to be sticky and will be overwritten only when the signaled interrupt is cleared by writing the LCD controller status register. For dual-panel displays, LCDIID is written only when both channels have reached a given state.

LCDIID is written with the last channel to reach that state. (i.e. LCDFID of the last channel to reach SOF would be written in LCDIID if SOF interrupts are enabled). Reserved bits must be written with zeros and reads from them must be ignored.

LCDIID **0x13050038**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	IID	A copy of Frame ID register, which transferred from Descriptor.	RW

17.8.29 Descriptor Address Registers (LCDDAx, LCDDA0_PART2)

A frame descriptor is a 4-word block, aligned on 4-word (16-byte) boundary, in external memory:

WORD [0] contains the physical address for next LCDDAx.
WORD [1] contains the physical address for LCDSAx.
WORD [2] contains the value for LCDFIDx.
WORD [3] contains the value for LCDCMDx.

Software must write the physical address of the first descriptor to LCDDAx before enabling the LCD Controller. Once the LCD Controller is enabled, the first descriptor is read, and all 4 registers are written by the DMAC. The next frame descriptor pointed to by LCDDAx is loaded into the registers for the associated DMA channel after all data for the current descriptor has been transferred.

NOTE: If only one frame buffer is used in external memory, the LCDDAx field (word [0] of the frame descriptor) must point back to itself. That is to say, the value of LCDDAx is the physical address of itself.

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Read/write registers LCDDA0 and LCDDA1, corresponding to DMA channels 0 and 1, contain the physical address of the next descriptor in external memory. The DMAC fetches the descriptor at this location after finishing the current descriptor. On reset, the bits in this register are zero. The target address must be aligned to 16-byte boundary. Bits [3:0] of the address must be zero.

LCDDA0, LCDDA1, LCDDA0_PART2 **0x13050040, 0x13050050, 0x130501C0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA0, 1	Next descriptor physical address. And descriptor structure as following: WORD [0]: next descriptor physical address WORD [1]: the buffer physical address WORD [2]: the buffer ID value (Only for debug) WORD [3]: the buffer property. The value is same as LCDCMD	RW

17.8.30 Source Address Registers (LCDSAx, LCDSA0_PART2)

Registers LCDSA0 and LCDSA1, corresponding to DMA channels 0 and 1, contain the physical address of frame buffer or palette buffer in external memory. The address must be aligned on a 4, 8, or 16 word boundary according to register LCDCTRL.BST. If this descriptor is for palette data, LCDSA0 points to the memory location of the palette buffer. If this descriptor is for frame data, LCDSAx points to the memory location of the frame buffer. This address is incremented by hardware as the DMAC fetches data from memory. If desired, the Frame ID Register can be used to hold the initial frame source address.

LCDSA0, LCDSA1, LCDSA0_PART2 **0x13050044, 0x13050054, 0x130501C4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA0, 1	Buffer start address. (Only for driver debug)	R

17.8.31 Frame ID Registers (LCDFIDx, LCDFID0_PART2)

Registers LCDFID0 and LCDFID1, corresponding to DMA channels 0 and 1, contain an ID field that describes the current frame. The particular use of this field is up to the software. This ID register is copied to the LCD Controller Interrupt ID Register when an interrupt occurs.

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LCDFID0, LCDFID1, LCDFID0_PART2 0x13050048, 0x13050058, 0x130501C8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID0, 1	Frame ID. (Only for debug)	R

17.8.32 DMA Command Registers (LCDCMDx, LCDCMD0_PART2)

LCDCMD0, LCDCMD1, LCDCMD0_PART2 0x1305004C, 0x1305005C, 0x130501CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOFINT	EOFINT	CMD	PAL	Uncomp_en	Uncomp_md	Reserved	LEN																								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SOFINT	Enable start of frame interrupt. When SOFINT =1, the DMAC sets the start of frame bit (LCDSTATE.SOF) when starting a new frame. The SOF bit is set after a new descriptor is loaded from memory and before the palette/frame data is fetched. In dual-panel mode, LCDSTATE.SOF is set only when both channels reach the start of frame and both frame descriptors have SOFINT set. SOFINT must not be set for palette descriptors in dual-panel mode, since only one channel is ever used to load the palette descriptor.	R
30	EOFINT	Enable end of frame interrupt. When EOFINT =1, the DMAC sets the end of frame bit (LCDSTATE.EOF) after fetching the last word in the frame buffer. In dual-panel mode, LCDSTATE.EOF is set only when both channels reach the end of frame and both frame descriptors have EOFINT set. EOFINT must not be set for palette descriptors in dual-panel mode, since only one channel is ever used to load the palette descriptor.	R
29	CMD	It is used to distinguish command and data in lcm mode. And it is only loaded via DMA channel 0. 1: The data is command 0: The data is data	R
28	PAL	The descriptor contains a palette buffer. PAL indicates that data being fetched will be loaded into the palette RAM. If PAL =1, the palette RAM data is loaded via DMA channel 0 as follows:	R

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		In bpp1, 2, 4, 8 mode, software must load the palette at least once after enabling the LCD. In bpp16 mode, PAL must be 0.	
27	Uncomp_en	It indicate this frm is compressed or not. 0: not compressed; 1: compressed.	R
26	Uncomp_md	It indicate this compressed frm is with alpha o without alpha. 0:with alpha; 1:without alpha.	R
25:24	Reserved	Writing has no effect, read as zero.	R
23:0	LEN	The buffer length value. (in WORD) The LEN bit field determines the number of bytes of the buffer size pointed by LCDSAx. LEN = 0 is not valid. DMAC fetch data according to LEN. Each time one or more word(s) been fetched, LEN is decreased automatically. Software can read LEN. *When you use decompressed function, the LEN should be the line number, not word number.	R

17.8.33 DMA OFFSIZE Registers (LCDOFFSx, LCDOFFS0_PART2)

LCDOFFS0, LCDOFFS1, LCDOFFS0_PART2 **0x13050060, 0x13050070, 0x130501E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								OFFSIZE																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
23:0	OFFSIZE0, 1 OFFSIZE0_PART2	OFFSIZE value for DMA 0,1. Indicate the offset in word. *please notice that when you need OFFSIZE function, to set this reg to an un-zero value and also need to set LCDPW0, 1 to indicate how much word in one line of this frame. *When you use decompress function, you must use this to indicate of how many word of a line in the source buffer.	R

17.8.34 DMA Page Width Registers (LCDPWx, LCDPW0_PART2)

LCDPW0, LCDPW1, LCDPW_PART2 **0x13050064, 0x13050074, 0x130501E4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								PAGEWIDTH																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
23:0	PAGEWIDTH0, 1 PAGEWIDTH0_PART2	Page width for DMA 0,1. * When you set LCDOFFS.OFFSIZE0/1 to 0, you need keep the PAGEWIDTH0/1 0. *When you use decompress function, you don't need set this register, dma will get pagewidth of every line automatically.	R

17.8.35 DMA Commend Counter Registers (LCDCNUMx)

When LCDCMD.CMD = 1, **0x13050068, 0x13050078** is use as LCDCNUM0, 1 LCDCNUM0_PART2 are not used now, set it to 0.

LCDCNUM0, LCDCNUM1, LCDCNUM0_PART2 **0x13050068, 0x13050078, 0x130501E8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								CNUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	CNUM0,1	Commands' number in this frame transfer by DMA. (only use in Smart LCD mode)	R

17.8.36 Foreground x Size in Descriptor (LCDDESSIZEx, LCDDESSIZE0_PART2)

When LCDCMD.CMD = 0, **0x1305006C, 0x1305007C** is use as LCDDESSIZE0, 1, to indicator the next frame foreground0, 1's size.

LCDDESSIZE0, 1, LCDDESSIZE0_PART2 **0x1305006C, 0x1305007C, 0x130501EC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Height												Reserved				Width											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	Height	The height of foreground 0.	R
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	Width	The width of foreground 0.	R

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17.8.37 Priority level threshold configure Register (LCDPCFG)

LCDPCFG **0x130502C0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Lcd_pri_md	HP_BST			Reserved	Pcfg2											Pcfg1															
RST	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The 3 thresholds cut the output fifo into 4 space,. When the entries remained triggers one of them, the priority level will be altered by hardware. And the 3 thresholds must follow the order: pcfg2 ≥ pcfg1 ≥ pcfg0.

Priority level

Priority_lv	Space
00	Empty ~ threshold0
01	Threshold0 ~ threshold1
10	Threshold1 ~ threshold2
11	Threshold2 ~ full

Bits	Name	Description	RW
31	Lcd_pri_md	Lcd priority mode. 0: use lcd dynamitic priority level; 1: use arbiter priority level.	RW
30:28	HP_BST	Highest priority Burst Length Selection. 000: 4 word 001: 8 word 010: 16 word 011: 32 word 101: Contiue16 100: 64 word 111: disable	RW
27	Reserved	Writing has no effect, read as zero.	R
26:18	Pcfg2	Threshold2: 0~511.	RW
17:9	Pcfg1	Threshold1: 0~511.	RW
8:0	Pcfg0	Threshold0: 0~511	RW

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17.9 LCD Controller Pin Mapping

There are several mapping schemes for different LCD panels.

17.9.1 TFT and CCIR Pin Mapping

Pin	Generic 8-bit Serial TFT	Generic 18/16-bit Parallel TFT		Special TFT 1 18/16-bit Parallel		Special TFT 2 18/16-bit Parallel		Special TFT 3 18/16-bit Parallel		CCIR656 8-bit	CCIR601 16-bit
Lcd_pclk/ Slcd_clk	CLK	CLK		DCLK		CLK		HCLK		CLK	CLK
Lcd_vsync/ Slcd_cs	VSYNC	VSYNC		SPS		GSRT		STV		VSYNC	VSYNC
Lcd_hsync/ Slcd_rs	HSYNC	HSYNC		LP		GPCK		STH		HSYNC	HSYNC
Lcd_de	DE	DE		-		-		-		-	-
Lcd_ps	-	-		Pulse		Toggle		Toggle		-	-
Lcd_cls	-	-		Pulse		Pulse		Pulse		-	-
Lcd_rev	-	-		Toggle		Toggle		Toggle		-	-
Lcd_spl	-	-		Pulse		Pulse		**Toggle**		-	-
Lcd_dat17	-	R5	-	R5	-	R5	-	R5	-	-	-
Lcd_dat16	-	R4	-	R4	-	R4	-	R4	-	-	-
Lcd_dat15	-	R3	R5	R3	R5	R3	R5	R3	R5	-	D15
Lcd_dat14	-	R2	R4	R2	R4	R2	R4	R2	R4	-	D14
Lcd_dat13	-	R1	R3	R1	R3	R1	R3	R1	R3	-	D13
Lcd_dat12	-	R0	R2	R0	R2	R0	R2	R0	R2	-	D12
Lcd_dat11	-	G5	R1	G5	R1	G5	R1	G5	R1	-	D11
Lcd_dat10	-	G4	G5	G4	G5	G4	G5	G4	G5	-	D10
Lcd_dat9	-	G3	G4	G3	G4	G3	G4	G3	G4	-	D9
Lcd_dat8	-	G2	G3	G2	G3	G2	G3	G2	G3	-	D8
Lcd_dat7	R7/G7/B7	G1	G2	G1	G2	G1	G2	G1	G2	D7	D7
Lcd_dat6	R6/G6/B6	G0	G1	G0	G1	G0	G1	G0	G1	D6	D6
Lcd_dat5	R5/G5/B5	B5	G0	B5	G0	B5	G0	B5	G0	D5	D5
Lcd_dat4	R4/G4/B4	B4	B5	B4	B5	B4	B5	B4	B5	D4	D4
Lcd_dat3	R3/G3/B3	B3	B4	B3	B4	B3	B4	B3	B4	D3	D3
Lcd_dat2	R2/G2/B2	B2	B3	B2	B3	B2	B3	B2	B3	D2	D2
Lcd_dat1	R1/G1/B1	B1	B2	B1	B2	B1	B2	B1	B2	D1	D1
Lcd_dat0	R0/G0/B0	B0	B1	B0	B1	B0	B1	B0	B1	D0	D0

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TFT 24 bit parallel mode/16 bit parallel mode2:

Pin	16 bit Parallel mode2	24 bit Parallel
Lcd_pclk/ Slcd_clk	CLK	CLK
Lcd_vsync/Slcd_cs	VSYNC	VSYNC
Lcd_hsync/Slcd_rs	HSYNC	HSYNC
Lcd_de	DE	DE
Lcd_ps	-	-
Lcd_cls	-	-
Lcd_rev	-	-
Lcd_spl	-	-
Lcd_dat17	R7	R7
Lcd_dat16	R6	R6
Lcd_dat15	R5	R5
Lcd_dat14	R4	R4
Lcd_dat13	R3	R3
Lcd_dat12	G7	R2
Lcd_dat11	G6	G7
Lcd_dat10	G5	G6
Lcd_dat9	0 (NC for panel)	G5
Lcd_dat8	G4	G4
Lcd_dat7	G3	G3
Lcd_dat6	G2	G2
Lcd_dat5	B7	B7
Lcd_dat4	B6	B6
Lcd_dat3	B5	B5
Lcd_dat2	B4	B4
Lcd_dat1	B3	B3
Lcd_dat0	0 (NC for panel)	B2
Lcd_lo6_o[5]	0	R1
Lcd_lo6_o[4]	0	R0
Lcd_lo6_o[3]	0	G1
Lcd_lo6_o[2]	0	G0
Lcd_lo6_o[1]	0	B1
Lcd_lo6_o[0]	0	B0

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17.9.2 Single Panel STN Pin Mapping

Pin	Color STN	Mono STN			
	PDW=3	PDW=0	PDW=1	PDW=2	PDW=3
Lcd_pclk	CLK	CLK	CLK	CLK	CLK
Lcd_vsync	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
Lcd_hsync	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
Lcd_de	BIAS	BIAS	BIAS	BIAS	BIAS
Lcd_ps	-	-	-	-	-
Lcd_cls	-	-	-	-	-
Lcd_rev	-	-	-	-	-
Lcd_spl	-	-	-	-	-
Lcd_dat17	-	-	-	-	-
Lcd_dat16	-	-	-	-	-
Lcd_dat15	-	-	-	-	-
Lcd_dat14	-	-	-	-	-
Lcd_dat13	-	-	-	-	-
Lcd_dat12	-	-	-	-	-
Lcd_dat11	-	-	-	-	-
Lcd_dat10	-	-	-	-	-
Lcd_dat9	-	-	-	-	-
Lcd_dat8	-	-	-	-	-
Lcd_dat7	D7	-	-	-	D7
Lcd_dat6	D6	-	-	-	D6
Lcd_dat5	D5	-	-	-	D5
Lcd_dat4	D4	-	-	-	D4
Lcd_dat3	D3	-	-	D3	D3
Lcd_dat2	D2	-	-	D2	D2
Lcd_dat1	D1	-	D1	D1	D1
Lcd_dat0	D0	D0	D0	D0	D0

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17.9.3 Dual Panel STN Pin Mapping

Pin	Color STN	Mono STN			
	PDW=3	PDW=0	PDW=1	PDW=2	PDW=3
Lcd_pclk	CLK	-	-	CLK	CLK
Lcd_vsync	VSYNC	-	-	VSYNC	VSYNC
Lcd_hsync	HSYNC	-	-	HSYNC	HSYNC
Lcd_de	BIAS	-	-	BIAS	BIAS
Lcd_ps	-	-	-	-	-
Lcd_cls	-	-	-	-	-
Lcd_rev	-	-	-	-	-
Lcd_spl	-	-	-	-	-
Lcd_dat17	-	-	-	-	-
Lcd_dat16	-	-	-	-	-
Lcd_dat15	UD7	-	-	-	UD7
Lcd_dat14	UD6	-	-	-	UD6
Lcd_dat13	UD5	-	-	-	UD5
Lcd_dat12	UD4	-	-	-	UD4
Lcd_dat11	UD3	-	-	UD3	UD3
Lcd_dat10	UD2	-	-	UD2	UD2
Lcd_dat9	UD1	-	-	UD1	UD1
Lcd_dat8	UD0	-	-	UD0	UD0
Lcd_dat7	LD7	-	-	-	LD7
Lcd_dat6	LD6	-	-	-	LD6
Lcd_dat5	LD5	-	-	-	LD5
Lcd_dat4	LD4	-	-	-	LD4
Lcd_dat3	LD3	-	-	LD3	LD3
Lcd_dat2	LD2	-	-	LD2	LD2
Lcd_dat1	LD1	-	-	LD1	LD1
Lcd_dat0	LD0	-	-	LD0	LD0

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17.9.4 Data mapping to GPIO function.

pin name in LCD	mapping to GPIO function
Lcd_dat17/Slcd_dat17	lcd_r7
Lcd_dat16/Slcd_dat16	lcd_r6
Lcd_dat15/Slcd_dat15	lcd_r5
Lcd_dat14/Slcd_dat14	lcd_r4
Lcd_dat13/Slcd_dat13	lcd_r3
Lcd_dat12/Slcd_dat12	lcd_r2
Lcd_dat11/Slcd_dat11	lcd_g7
Lcd_dat10/Slcd_dat10	lcd_g6
Lcd_dat9/Slcd_dat9	lcd_g5
Lcd_dat8/Slcd_dat8	lcd_g4
Lcd_dat7/Slcd_dat7	lcd_g3
Lcd_dat6/Slcd_dat6	lcd_g2
Lcd_dat5/Slcd_dat5	lcd_b7
Lcd_dat4/Slcd_dat4	lcd_b6
Lcd_dat3/Slcd_dat3	lcd_b5
Lcd_dat2/Slcd_dat2	lcd_b4
Lcd_dat1/Slcd_dat1	lcd_b3
Lcd_dat0/Slcd_dat0	lcd_b2
Lcd_lo6_o[5]	lcd_r1
Lcd_lo6_o[4]	lcd_r0
Lcd_lo6_o[3]	lcd_g1
Lcd_lo6_o[2]	lcd_g0
Lcd_lo6_o[1]	lcd_b1
Lcd_lo6_o[0]	lcd_b0

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17.10 Display Timing

17.10.1 General 16-bit and 18-bit TFT Timing

This section shows the general 16-bit and 18-bit TFT LCD timing diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed correspond to the LCD panel specification.

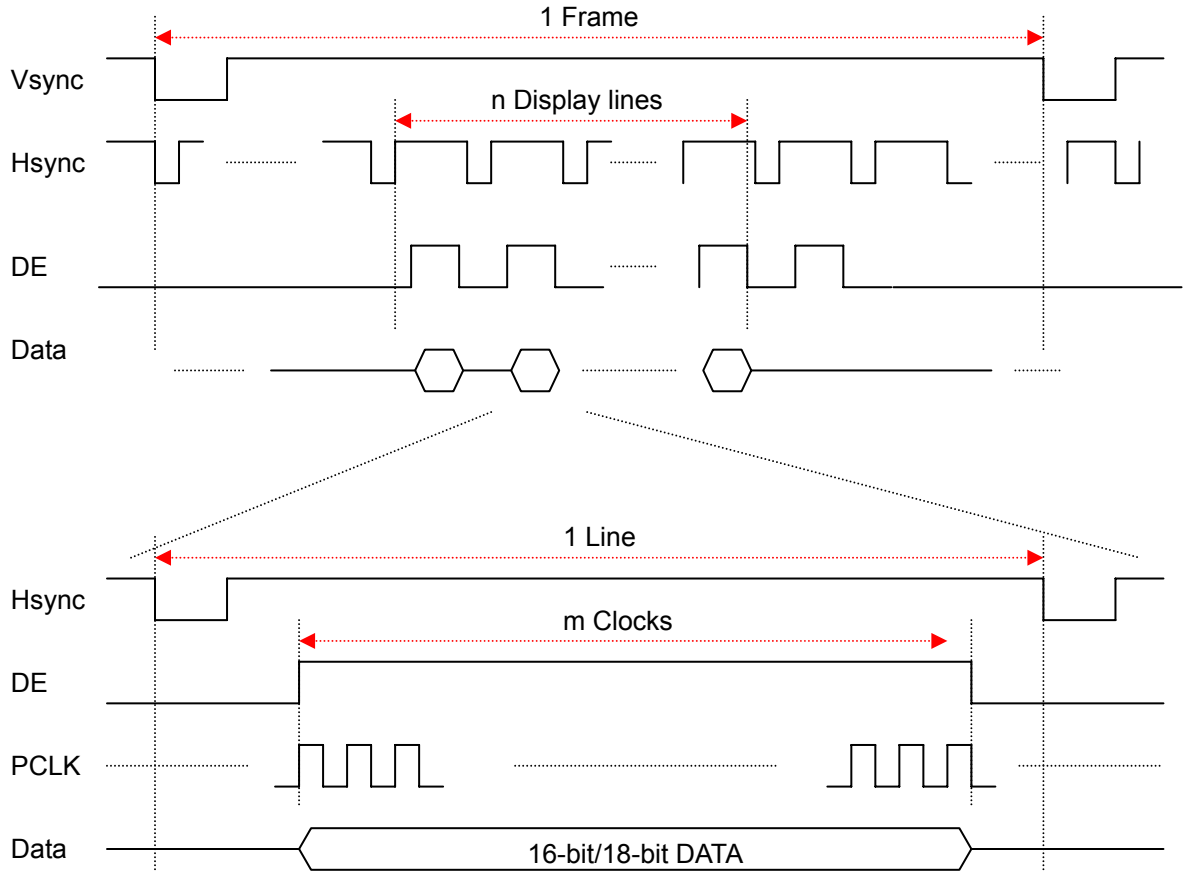


Figure 17-8 General 16-bit and 18-bit TFT LCD Timing

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17.10.2 8-bit Serial TFT Timing

This section shows the 8-bit serial TFT LCD timing diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed correspond to the LCD panel specification.

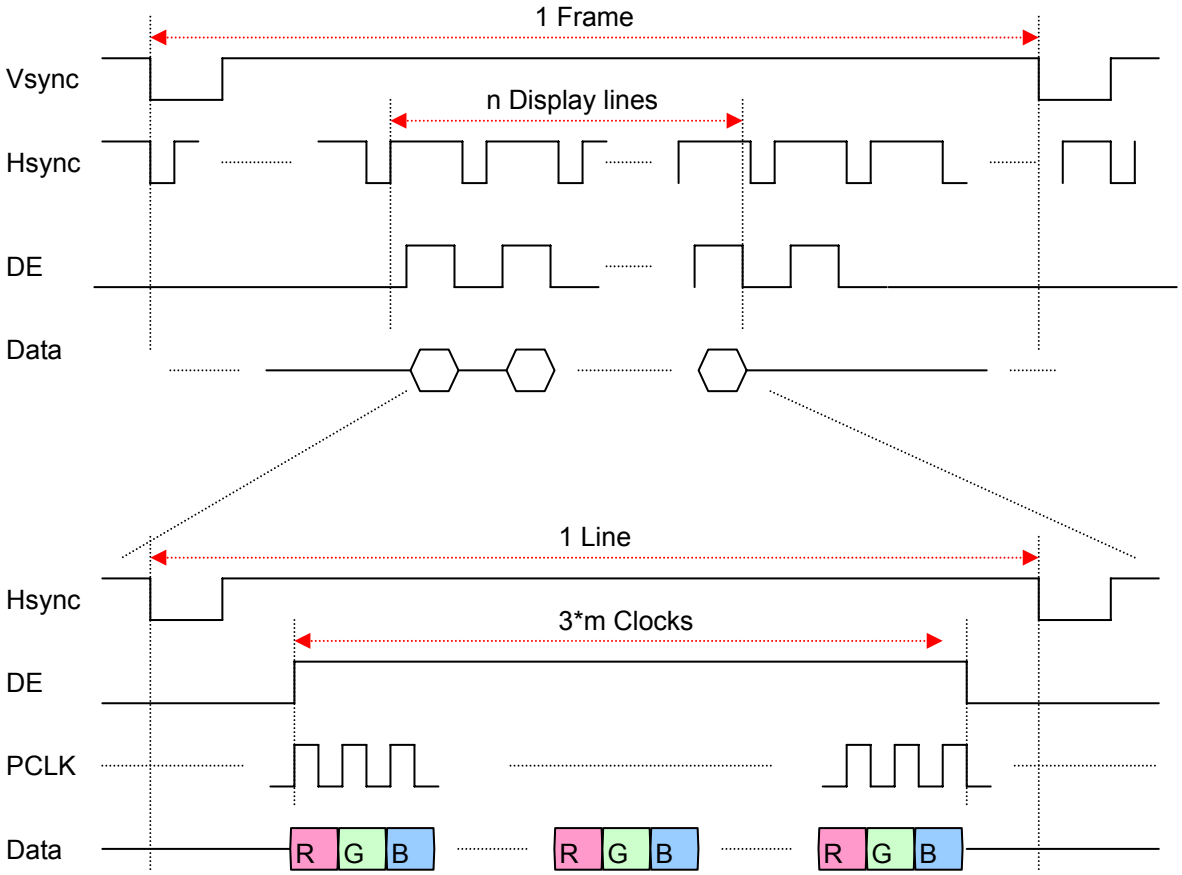


Figure 17-9 8-bit serial TFT LCD Timing (24bpp)

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17.10.3 Special TFT Timing

Based on the general TFT LCD support, this controller also provides 4 special signals that can be programmed to general some special timing used for some panel. All 4 signals are worked in two modes: pulse mode and toggle mode. Signal “CLS” is fixed in pulse mode, and “REV” in toggle mode. The work mode of signals “SPL” and “PS” are defined in the special TFT LCD mode 1 to mode 3, either pulse mode or toggle mode. The position and polarity of these 4 signals can be programmed via registers. The Figures show the two modes as follows: (The toggle mode of signal “SPL” is different with the others signal. “SPL” does toggle after display line.)

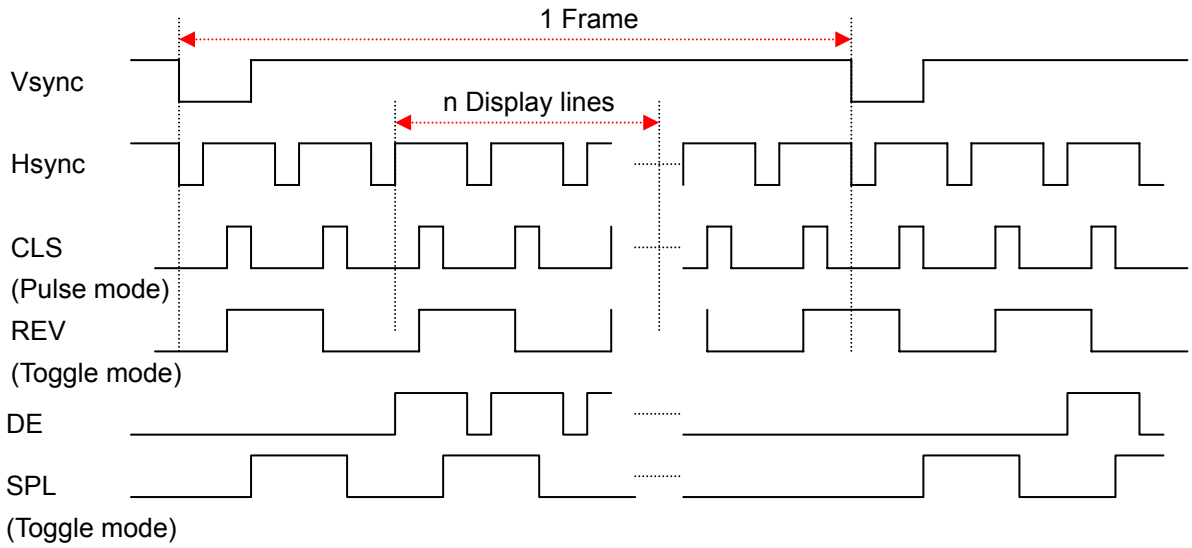


Figure 17-10 Special TFT LCD Timing 1

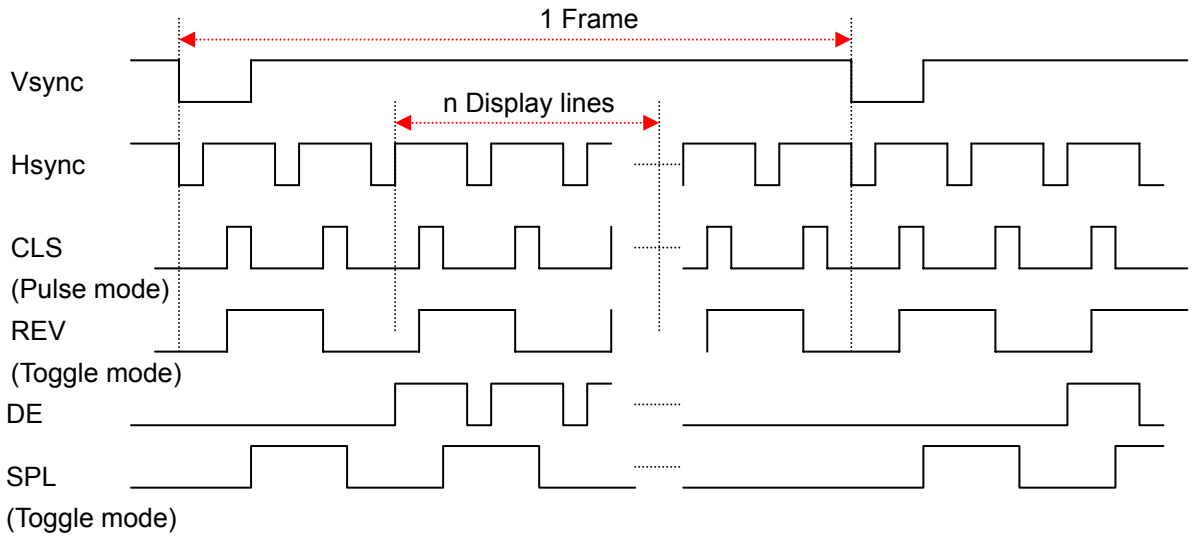


Figure 17-11 Special TFT LCD Timing 2

These two Figures show the timing of pulse mode and toggle mode, the pulse mode timing is same

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and the toggle mode timing is different. Timing 1 shows the condition when the total lines in 1 frame is odd (the number of display is even and the number of blank is odd), so the phase of REV inverse at the first line of each frame and the phase of SPL dose not inverse at the first line of each frame. Timing 2 shows the condition when the total lines in 1 frame is even (the number of display is even and the number of blank is even), so the phase of REV and SPL dose not inverse at the first line of each frame.

When LCDC is enabled ,there will be a null line to be add before transferring data to LCD panel. So the toggle mode exept SPL signal of special 3 TFT mode is when reset level is high,the first valid edge will be rising edge. SPL signal of special 3 TFT mode is when reset level is high,the first valid edge will be falling edge.

17.10.4 Delta RGB panel timing

This section shows the Delta RGB timing diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed. And the odd/even line RGB order also can be programmed correspond to the LCD panel specification.

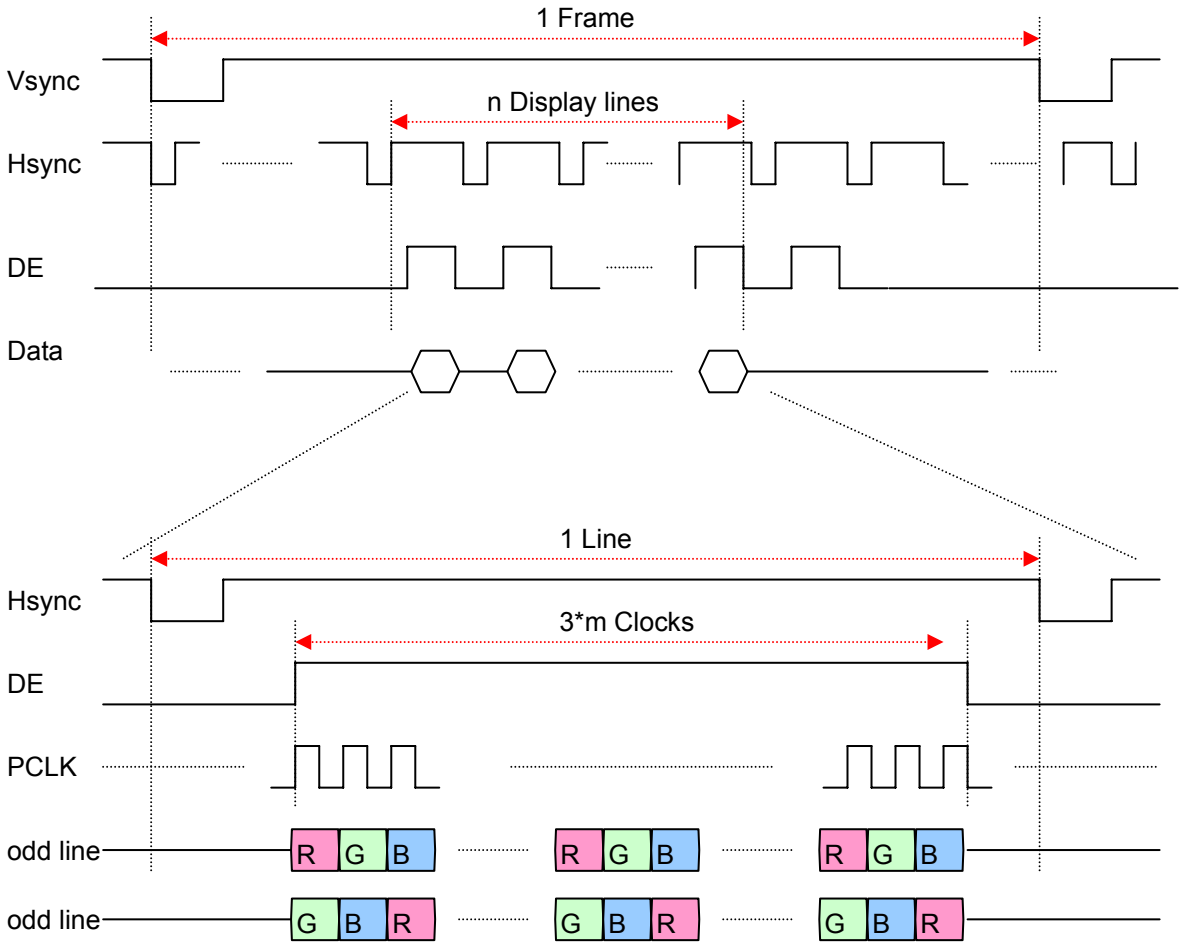
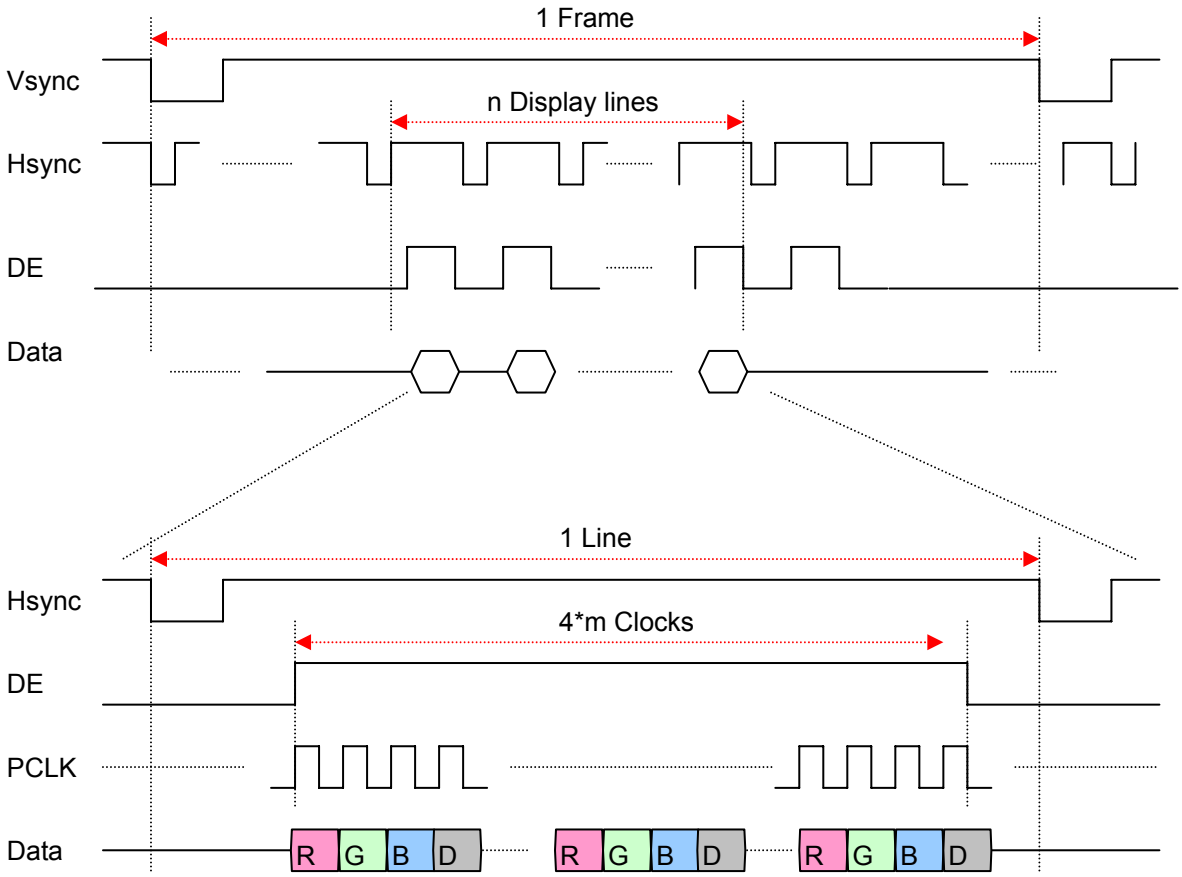


Figure 17-12 Delta RGB timing

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17.10.5 RGB Dummy mode timing

This section shows the RGB Dummy diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed.



***Dummy = 0**

Figure 17-13 RGB Dummy timing

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17.11 Format of Palette

This LCD controller contains a palette RAM with 256-entry x 16-bit used only for BPP8, BPP4, BPP2 and BPP1. Palette RAM data is loaded directly from the external memory palette buffer by DMAC channel 0. Each word of palette buffer contains 2 palette entries.

1 In 8-bpp modes, palette buffer size is128 words.
2 In 4-bpp modes, palette buffer size is 8 words.
3 In 2-bpp modes, palette buffer size is 2 words.
4 In 1-bpp modes, palette buffer size is 1 word.
5 In 16/18/24-bpp modes, has no palette buffer.

Palette buffer base address	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-1 bit: 15 . . . 0	Entry-0 bit: 15 . . . 0
Palette buffer base address + 4	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-3 bit: 15 . . . 0	Entry-2 bit: 15 . . . 0
Palette buffer base address + 8	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-5 bit: 15 . . . 0	Entry-4 bit: 15 . . . 0

17.11.1 STN

For STN Panel, 16-bpp pixel data is encoded with RGB 565 or RGB 555.
Please refer to register LCDCTRL.RGB.

BPP 16, RGB 565, pixel encoding for STN Panel:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

BPP 16, RGB 555, pixel encoding for STN Panel:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

17.11.2 TFT

BPP 16, RGB 565, pixel encoding for TFT Panel:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

NOTE: For BPP 16, 18, 24, palette is bypass.

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17.12 Format of Frame Buffer

17.12.1 16bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

17.12.2 18bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	R5	R4	R3	R2	R1	R0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G5	G4	G3	G2	G1	G0	0	0	B5	B4	B3	B2	B1	B0	0	0

17.12.3 24bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

17.12.4 16bpp with alpha

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A7	A6	A5	A4	A3	A2	A1	A0	0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1

17.12.5 18bpp with alpha

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A7	A6	A5	A4	A3	A2	A1	A0	R5	R4	R3	R2	R1	R0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G5	G4	G3	G2	G1	G0	0	0	B5	B4	B3	B2	B1	B0	0	0

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17.12.6 24bpp with alpha

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A7	A6	A5	A4	A3	A2	A1	A0	R7	R6	R5	R4	R3	R2	R1	R0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

17.12.7 24bpp compressed

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BLUE 1 [7:0]								RED 0 [7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GREEN 0 [7:0]								BLUE 0 [7:0]							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GLEEN 2 [7:0]								BLUE 2 [7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RED 1 [7:0]								GLEEN 1 [7:0]							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RED 3 [7:0]								GLEEN 3 [7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BLUE3 [7:0]								RED2 [7:0]							

17.13 Format of Data Pin Utilization

17.13.1 Mono STN

In Mono STN mode, data pin pixel ordering of one LCD screen row. Column 0 is the first pixel of a screen row.

Upper panel								
Panel data width	**Col0**	**Col1**	**Col2**	**Col3**	**Col4**	**Col5**	**Col6**	**Col7**
1 bit	D0	D0	D0	D0	D0	D0	D0	D0
2 bit	D1	D0	D1	D0	D1	D0	D1	D0
4 bit	D3	D2	D1	D0	D3	D2	D1	D0
8 bit	D7	D6	D5	D4	D3	D2	D1	D0
Lower panel (dual-panel mode)								
4 bit	D11	D10	D9	D8	D11	D10	D9	D8
8 bit	D15	D14	D13	D12	D11	D10	D9	D8

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17.13.2 Color STN

In Color STN mode, data pin pixel ordering of one LCD screen row. Column 0 is the first pixel of a screen row.

Upper panel							
Col0 (R)	**Col0 (G)**	**Col0 (B)**	**Col1 (R)**	**Col1 (G)**	**Col1 (B)**	**Col2 (R)**	**Col2 (G)**
D7	D6	D5	D4	D3	D2	D1	D0
Lower panel (dual-panel mode)							
D15	D14	D13	D12	D11	D10	D9	D8

17.13.3 18-bit Parallel TFT

Col0 (RGB)																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

17.13.4 16-bit Parallel TFT

Col0 (RGB)															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

17.13.5 8-bit Serial TFT (24bpp)

Col0 (R)							
D7	D6	D5	D4	D3	D2	D1	D0
Col0 (G)							
D7	D6	D5	D4	D3	D2	D1	D0
Col0 (B)							
D7	D6	D5	D4	D3	D2	D1	D0

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17.14 LCD Controller Operation

17.14.1 Set LCD Controller AHB Clock and Pixel Clock

The LCD Controller has 2 clock input: AHB clock and pixel clock. The both clocks are generated by CPM (Clock and Power Manager). The frequency of the 2 clocks can be set by CPM registers. lcdc 's AHB clock is equal to AHB0 clock (HCLK in CPM spec), and CPM.LPCDR set LCD pixel clock division ratio. Please refer to CPM spec for detail.

LCD AHB clock is the LCD controller's internal clock while LCD pixel clock is output to drive LCD panel. There have 2 rules for LCD clocks:

1 For TFT Panel, the frequency of LCD AHB clock must be at least 1.5 times of LCD pixel clock.
2 For STN Panel, the frequency of LCD AHB clock must be at least 3 times of LCD pixel clock.

LCD panel determines the frequency of LCD pixel clock.

17.14.2 Enabling the Controller

If the LCD controller is being enabled for the first time after system reset or sleep reset, all of the LCD registers must be programmed as follows:

1 Write the frame descriptors and, if needed, the palette descriptor to memory.
2 Program the entire LCD configuration registers except the Frame Descriptor Address Registers (LCDDAx) and the LCD Controller enable bit (LCDCTRL.ENA).
3 Program LCDDAx with the memory address of the palette/frame descriptor.
4 Enable the LCD controller by writing to LCDCTRL.ENA.

If the LCD controller is being re-enabled, there has not been a reset since the last programming; only the registers LCDDAx and LCDCTRL.ENA need to be reprogrammed. The LCD Controller Status Register (LCDSTATE) must also be written to clear any old status flags before re-enabling the LCD controller.

Once the LCD controller has been enabled, do not write new values to LCD registers except LCDCTRL.ENA or DIS or LCDDA0/1 or LCDOSDC.F0/1EN .

17.14.3 Disabling the Controller

The LCD controller can be disabled in two ways: regular and quick.

1 Regular disabling.
Regular disabling is accomplished by setting the disable bit, LCDCTRL.DIS. The other bits in LCDCTRL must not be changed — read the register, set the DIS bit, and rewrite the register. This method causes the LCD controller to stop cleanly at the end of a frame. The LCD Disable Done bit, LCDSTATE.LDD, is set when the LCD controller finishes displaying the last frame, and the enable bit, LCDCTRL.ENA, is cleared automatically by hardware.
LCDCTRL.DIS must be set zero when enabling the controller.

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2 Quick disabling.

Quick disabling is accomplished by clearing the enable bit, LCDCTRL.ENA. The LCD controller will finish any current DMA transfer, stop driving the panel, setting the LCD Quick Disable bit (LCDSTATE.QD) and shut down immediately. This method is intended for situations such as a battery fault, where system bus traffic has to be minimized immediately so the processor can have enough time to store critical data to memory before the loss of power. The LCD controller must not be re-enabled until the QD bit is set, indicating that the quick shutdown is complete. Do not set the DIS bit when a quick disabling command has been issued.

NOTE: It is strongly recommended that software set the "LCD Module Stop Bit" in PMC to shut down LCDC clock supply to save power consumption after disable LCDC. Please refer to PMC for detailed information.

17.14.4 Resetting the Controller

At reset, the LCD Controller is disabled. All LCD Controller Registers are reset to the conditions shown in the register descriptions.

17.14.5 Frame Buffer & Palette Buffer

The starting address of frame buffer stored in external memory must be aligned to 4, 8 or 16 words boundary according to register LCDCTRL.BST. The length of buffer must be multiple of word (32-bit).

If LCDCTRL .BST = 0, align frame and palette buffer to 16 word boundary
If LCDCTRL .BST = 1, align frame and palette buffer to 8 word boundary
If LCDCTRL .BST = 2, align frame and palette buffer to 4 word boundary

One frame buffer contains encoded pixel data of multiple of screen lines; each line of encoded pixel data must be aligned to word boundary. If the length of a line is not the multiple of word, extra bits must be applied to reach a word boundary. It is suggested that the extra bits to be set zero.

17.14.6 CCIR601/CCIR656

CCIR601: just as 16bit-parallel output.

CCIR656: need external encoder, or software designer need give digital blanking data and timing reference signal in data buffer.

17.14.7 OSD Operation

1 Normal process.

a Configuration.

* LCDCFG and LCDCTRL
* LCDOSDC and LCDOSDCTRL

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* LCDRGBC and LCDIPUR

b Set Color.
* LCDBGC, LCDKEY0, LCDKEY1, LCDALHPA

c Set Display.
* LCDVAT, LCDDAH, LCDDAV
* LCDXYP0, LCDXYP1, LCDSIZE0, LCDSIZE1
* LCDVSYNC, LCDHSYNC

d Set DMAC.
* LCDIID
* LCDDA0, LCDSA0, LCDFID0, LCDCMD0, LCDOFFS0, LCDPW0, LCDCNUM0, LCDDESSIZE0
* LCDDA1, LCDSA1, LCDFID1, LCDCMD1, LCDOFFS1, LCDPW1, LCDCNUM1, LCDDESSIZE1

e Enable LCDC.

f Check the state from register LCDSTATE and LCDOSDS.

2 Reconfigure OSD.

If foreground0 and foreground1 (enable, position, size) need to reconfigure during display process, there has two methods.

Method1: (recommend in TFT and SLCD)

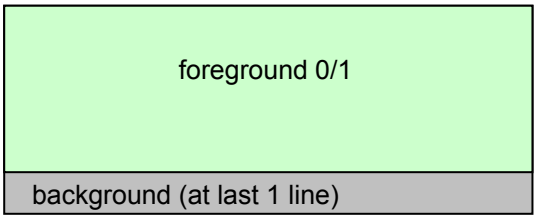
a Reconfigure the relate Register after disable LCDC.
b In TFT mode, use normal disable to avoid lcd panel flicker.
c In SLCD mode, use quick disable. (smart LCD could keep the frame by its inner buffer)
d After disable LCDC, you can reconfigure any register/descriptor, but please make sure this process is quick enough in TFT mode. (less than the interval between two frame)

Method2:

Dynamic reconfigure the register:

You can reconfigure some register(LCDOSDC.F0/1EN) during display process but there some rule you must follow:

a Foreground 0/1 are at last 1 line less than background.



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b Foreground 0 and foreground 1's data can not less than 33 words(except 0 word). Or you only can change those register after disable LCDC.

c When use TFT panel. During the display process, you can re-configure the LCDOSDC.F0EN, LCDCOSDC.F1EN; (You can not change them when use SLCD or TVE) but the new configuration will recognized by LCDC module after finished a complete frame. If you need to re-configure LCDOSDCTRL.IPU to select IPU or DMA channel 1, you need to follow the process below:
   - Quick or Normal disable LCDC. (SLCD only can use Quick disable)
   - Configure the LCDOSDCTRL to set IPUEN, and then enable LCD.

   To change IPU to DMA1 you can:
   - Quick or Normal disable LCDC. (SLCD only can use Quick disable)
   - Configure the LCDOSDCTRL to set IPUEN = 0, and then enable LCD.

3 During the display process, while foreground 1 use IPU, to change size of foreground 1 you need follow the step shown bellow:
   a Quick or Normal disable LCDC. (SLCD only can use Quick disable)
   b Configure the IPU, and LCDSIZE1.
   c Run IPU and enable LCDC.

4 You **CAN NOT** change BPP or OSDBPP during the display process. if you want to change them first you should disable LCDC, change the BPP or OSDBPP and then enable LCDC.
If you need not use Foreground0 during the whole display process. set BPP to 5.

5 You can change LCDSIZE0/1 during display process without disable LCD controller.
Method 1:
   a Set LCDCOSDC.F0/1EN = 0. (follow the rule above)
   b Re-configure LCDSIZE0/1 (and the relate DMA0/1 descriptor); then set LCDOSDCTRL.CHANGE = 1.
   c Wait until CHANGE = 0 and then set LCDOSDC.F0/1EN = 1.

Method 2:
   a Set LCDOSDCTRL.CHANGE = 1.
   b Wait until LCDOSDS. READY = 1.
   c Change relate DMA0/1 channel descriptor.
   d Wait until LCDOSDCTRL.CHANGE = 0.

*Please notice that in TVE (not include VGA) and SLCD only use method 2.

6 You can change LCDXY0/1 during display process without disable LCD controller.
Method 1:
   a Set LCDOSDC.F0/1EN = 0. (follow the rule above)
   b Change LCDXYPOS0/1 and then set LCDOSDCTRL.CHANGE = 1.

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c Wait until LCDOSDCTRL.CHANGE = 0.

Method 2:

a Change LCDXYPOS0/1.
b Set LCDOSDCTRL.CHANGE = 1.
c Wait until LCDOSDCTRL.CHANGE = 0.

*Please notice that in TVE (not include VGA) and SLCD only use method 2.

*Please notice that if you do not change foreground 0/1's size and position, keep LCDOSDCTRL.CHANGE = 0. And you can only change one of them in one time.

7 How to "close/open" foreground0 and foreground1?

Method 1:

a Set LCDOSDCTRL.CHANGE = 1.
b Wait until LCDOSDS. READY = 1.
c Direct change LCDOSDC.F0/1EN.
d Wait until LCDOSDCTRL.CHANGE = 0.

Method 2:

Change foreground0/1 size to 0 Without change LCDOSDC.F0/1EN.

Method 3: (recommend)

Normal disable LCDC, and change LCDOSDC.F0/1EN. Use normal disable need to wait LCDSTATE.LDD, and set relate register soon, to make sure the LCD panel are not flicker.

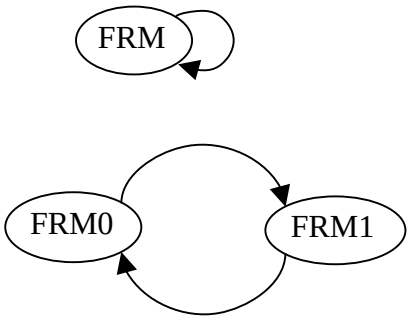
*Please notice that in TVE (not include VGA) and SLCD only use method 2,3. And strongly suggest that DO NOT close both foreground0 and 1 or set both foreground0 and 1 's size to 0.

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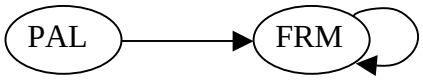
17.14.8 Descriptor Operation

1 TFT panel

Not use palette: you can use only one descriptor or several connected descriptor. As which shown below.



Use palette: add one PAL descriptor at the beginning of descriptor chain.



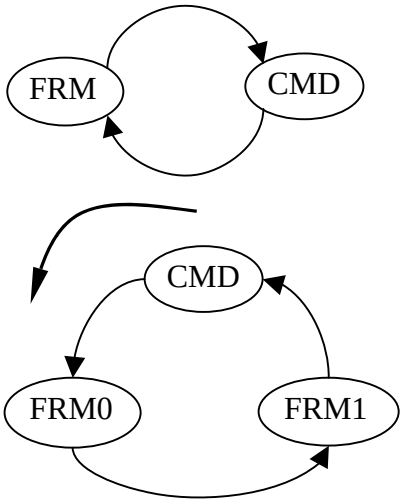
When you need to change palette during the display you need follow the steps shown below.



*Please notice that you **cannot** disable foreground 0 during the whole process. and also You can not change PAL when Foreground 0' s area == 0 or not enable LCDOSDC.F0EN.

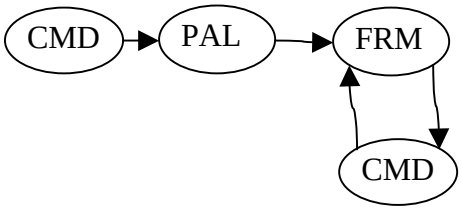
2 SLCD

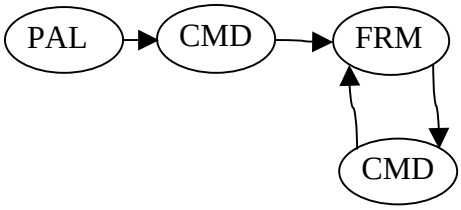
Not use palette.



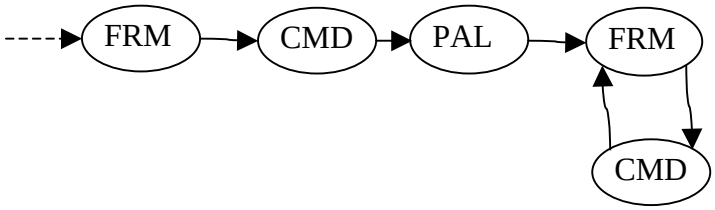
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Use palette.





Change palette.



You can not change PAL when Foreground 0' s area == 0. Or not enable LCDOSDC.F0EN and during you change PAL, you can not change F0 or F1's size.

17.14.9 IPU direct connect mode

When you use IPU direct connect mode, you need to:

1 Open IPU early than LCDC.
2 Use normal disable in TFT mode, and use quick disable in SLCD/TVE mode.
3 When you use normal disable you need to wait IPU frame end flag.
4 When you use quick disable you must not wait IPU frame end flag, and must reset IPU before restart LCDC and IPU.
5 In SLCD mode, you can first wait IPU frame end flag, then quick stop LCDC. Then you need not reset IPU before restart LCDC and IPU.

* "IPU frame end flag" please refer to IPU spec.

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17.14.10 VGA output

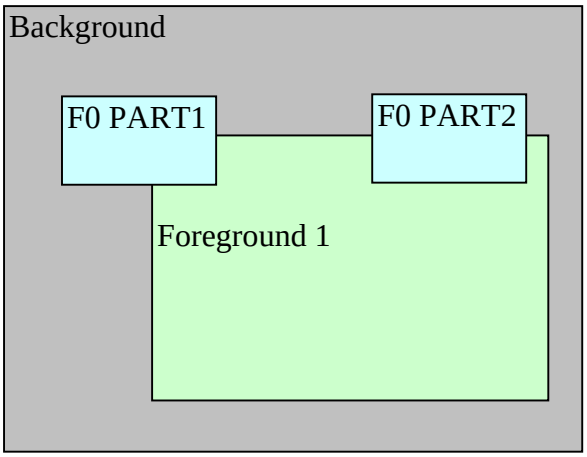
When you use VGA output you need:

1 Open all channel of DAC. (refer to TVEDAC spec)
2 Set TVEN to 0.
3 Disable LCD panel pins (except HSYNC/VSYNC) for save power. (refer to GPIO spec)

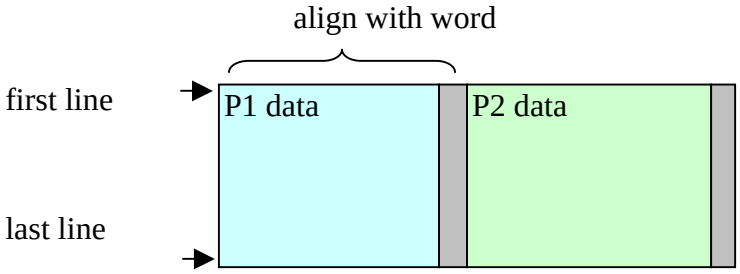
17.14.11 Foreground 0 divide mode

In divide mode the original register of foreground 0 position and size are correspond to F0 PART1, the additional (named with "_part2") registers correspond to F0 PART2.
LCDOSDC.F0EN correspond the total foreground 0 （part1 and part2）and each part has a F0PxEN to enable.
F0EN, F0P2EN, F0P1EN, and part2's position/size can be reconfigure during display process. (refer to 1.12.6)

MODE 1: LCDOSDC.F0DIVMD = 0. F0P2MD = 1.



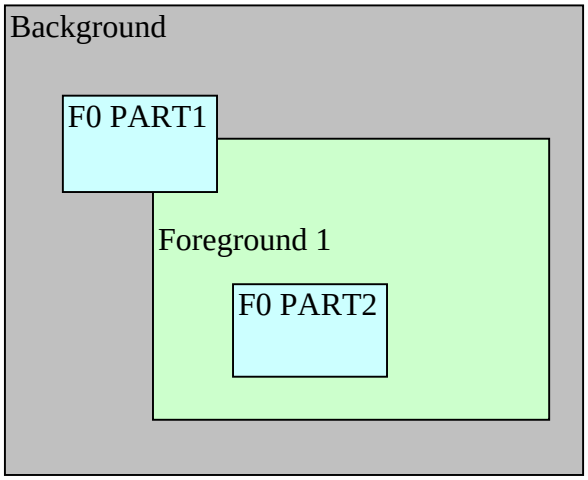
Foreground 0 divided into 2 parts, and PART1, PART2 must begin with same line and has the same height. They can have different width but cannot overlay each other.
They can use only one descriptor (connect to it self).
The two parts data must "combination" in one data buffer as follow:



*Please notice that in this mode, you need to disable LCDC before reconfigure foreground0/1's Register.

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MODE 2: LCDOSDC.F0DIVMD = 1. F0P2MD = 0. F0P1EN = 1. F0P2EN = 1.



Foreground 0 divided into 2 parts, and PART1, PART2 can have different width and height but cannot overlay each other. PART2 must below PART1 they also cannot have any superposition in vertical.

PART1 and PART2 use independent descriptor refer to descriptor register with “part2”

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18 Smart LCD Controller

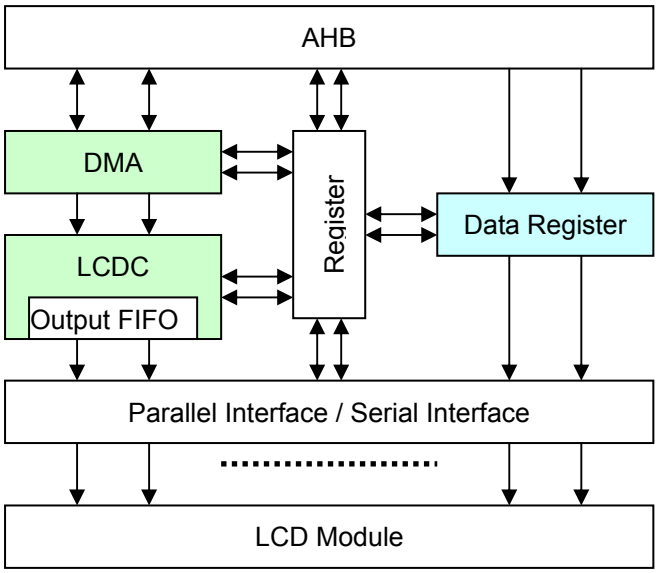
18.1 Overview

The Smart LCD Controller affords an interface to transfer data from the LCD controller to the LCD Module. It supports DMA operation and register operation.

Features:

- Supports a large variety of LCD Module from different vendors
- Supports parallel and serial interfaces
- Supports different size of display panel
- Supports different width of pixel data
- Supports internal DMA operation and register operation
- Supports Write Operation. Read Operation is not supported

18.2 Structure



*Please notice that the command only can transfer by DMA channel 0. No matter the DMA channel 1 or IPU are use or not.

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18.3 Pin Description

Table 18-1 SLCD Pins Description

Name	I/O	Description	Interface
SLCD_RS	O	Command/Data Select Signal. The polarity of the signal can be programmable.	Serial: RS Parallel: RS
SLCD_CS	O	Data Sample Signal. The polarity of the signal can be programmable.	Serial: CS Parallel: Sample Data with the edge of CS
SLCD_CLK	O	The clock of SLCD. The polarity of the clock can be programmable.	Serial or not used
SLCD_DAT*1 [17:0]	O	The data of SLCD. Relate to 1.9.4 Data mapping to GPIO function.	Serial: SLCD_DAT [15] Parallel: 18bit SLCD_DAT [17:0] 16bit SLCD_DAT [15:0] 8bit SLCD_DAT [7:0]
LCD_LO6_O	O	24 bit parallel SLCD RGB (or 24 bit command) low bit ([17:16],[9:8],[1:0]) output Relate to 1.9.4 Data mapping to GPIO function.	--

NOTE:

***1:** SLCD_DAT [15] is also use as data pin for serial. The SLCD pins are shared with LCDC. You can see the set of register LCDCFG.LCDPIN in LCDC spec.

18.4 Register Description

In this section, we will describe the registers in Smart LCD controller. Following table lists all the registers definition. All register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
MCFG	SLCD Configure Register	RW	0x0000	0x130500A0	32
MCTRL	SLCD Control Register	RW	0x00	0x130500A4	8
MSTATE	SLCD Status Register	RW	0x00	0x130500A8	8
MDATA	SLCD Data Register	RW	0x00000000	0x130500AC	32

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18.4.1 SLCD Configure Register (MCFG)

The register MCFG is used to configure SLCD.

MCFG																0x130500A0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			DWIDTH			CWIDTH		Reserved			CSPLY	RSPLY	Reserved	CLKPLY	TYPE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:10	DWIDTH*1	Data Width. DWIDTH / Data Width 000 18-bit once Parallel/Serial 001 16-bit once Parallel/Serial 010 8-bit third time Parallel 011 8-bit twice Parallel 100 8-bit once Parallel/Serial 101 24-bit once Parallel 111 9-bit twice Parallel 110 Reserved *Please notice that you can only use 24-bit parallel command when use 24-bit parallel data. (The command may not 24-bit but need put them as 24-bit in memory(one command use one word))	RW
9:8	CWIDTH*1	Command Width. CWIDTH / Command Width 00 16-bit once / 9bit once 01 8-bit once 10 18-bit once 11 24-bit once *Please notice that you can only use 24-bit parallel command when use 24-bit parallel data. (The command may not 24-bit but need put them as 24-bit in memory (one command use one word))	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	CSPLY	CS Polarity. (CS initial level will be different from CS Polarity) 0: Active Level is Low; 1: Active Level is High.	RW
3	RSPLY	RS Polarity. 0: Command RS = 0, Data RS = 1 1: Command RS = 1, Data RS = 0	RW
2	Reserved	Writing has no effect, read as zero.	R

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1	CLKPLY	LCD_CLK Polarity.,0: Active edge is Falling; 1: Active edge is Rising.	RW
0	TTYPE	Transfer Type. 0: Parallel; 1: Serial.	RW

NOTE:

*[1]: The set of DWIDTH and CWIDTH should keep to the rules as follows:

Interface Mode	Command Width	Data Width	Color
Parallel	18-bit	18-bit once	R6G6B6
	16-bit	16-bit once	R5G6B5
		9-bit twice	--
	9-bit	9-bit twice	--
	8-bit	8-bit once	--
		8-bit twice	
		8-bit third times	--
Serial	18-bit	18-bit once	--
	16-bit	16-bit once	--
	9-bit	9bit twice	--
	8-bit	8-bit once	--
		8-bit twice	--
		8-bit third times	--

18.4.2 SLCD Control Register (MCTRL)

MCTRL is SLCD Control Register.

MCTRL 0x130500A4

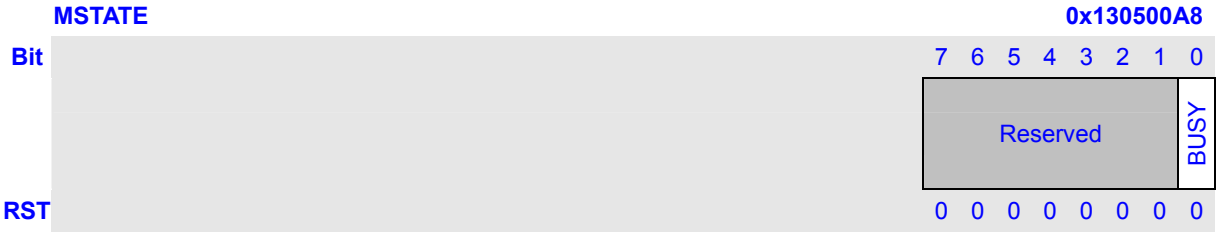
Bit	7	6	5	4	3	2	1	0
	Reserved					DMASTART	DMAMODE	Reserved
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	DMAMODE	SLCD descriptor DMA mode select. 0: DMA will continually transfer data follow descriptor chain 1: DMA will stop when one descriptor finished	RW
1	DMASTART	Only use when DMAMODE = 1, set 1 to restart DMA transfer.	RW
0	Reserved	Writing has no effect, read as zero.	R

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18.4.3 SLCD Status Register (MSTATE)

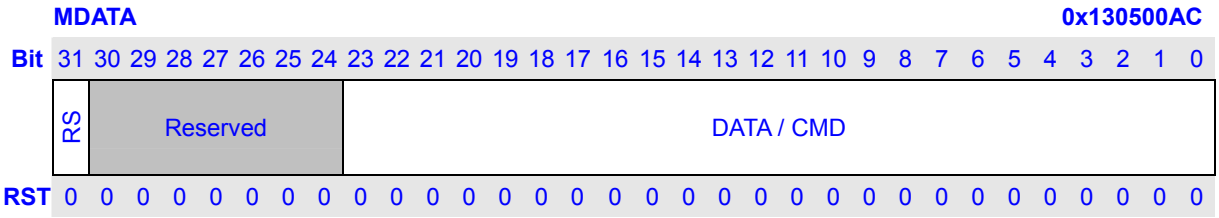
The register of MSTATE is SLCD status register.



Bits	Name	Description	RW
7:1	Reserved	Writing has no effect, read as zero.	R
0	BUSY	Transfer is working or not. This bit will be set to 1 when transfer is working. It will be cleared by hardware when transfer is finished. 0: not busy 1: busy	RW

18.4.4 SLCD Data Register (MDATA)

The register MDATA is used to send command or data to LCM. When RS=0, the low 24-bit is used as command. When RS=1, the low 24-bit is used as data.



Bits	Name	Description	RW
31	RS	The RS bit of data register is used to decide the meanings of the low 24-bit. 0: data 1: command	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23:0	DATA/CMD	Data or Command Register.	RW

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18.5 System Memory Format

18.5.1 Data format

You can configure these registers according to LCDC module.

18.5.2 Command Format

1 18-bit command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X	X	X	X	X	X	X	X	X	X	X	X	X	X	C17	C16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

2 16-bit command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

3 9-bit command once

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X	X	X	X	X	X	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	X	X	X	X	X	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

4 8-bit command once

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C7	C6	C5	C4	C3	C2	C1	C0	C7	C6	C5	C4	C3	C2	C1	C0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C7	C6	C5	C4	C3	C2	C1	C0	C7	C6	C5	C4	C3	C2	C1	C0

5 8-bit command twice (Command = command part + data part)

*Please notice that when you use this kind command, set CWIDTH as 8bit once and set the LCDCNUM.CNUM as doubled the real command number.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D7	D6	D5	D4	D3	D2	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0

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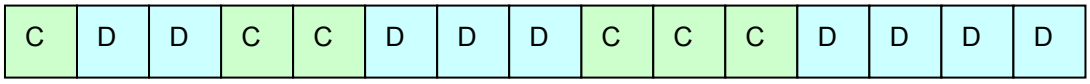
18.6 Transfer Mode

Two transfer modes can be used: DMA/IPU Transfer Mode and Data Register Transfer Mode. In DMA/IPU mode, always transfer commands by DMA 0.

18.6.1 DMA Transfer Mode

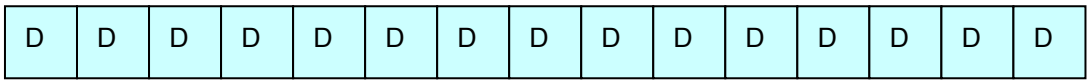
Command and data can be recognized by RS bit coming from memory. The format of DMA transfer can be as follows:

1 Command and Data



*Please notice that the command only can insert between two complete frame and the number of command is 0~255.

2 Only Data



*You can also not use command but you still need to use a command descriptor and set the CNUM = 0.

Because DMA transfer mode only can work in OSD mode, you need to configure the panel according OSD mode:

1 Configuration.
* LCDCFG and LCDCTRL
* LCDOSDC and LCDOSDCTRL
* LCDRGBC and LCDIPUR

2 Set Color.
* LCDBGC, LCDKEY0, LCDKEY1, LCDALHPA

3 Set Display.
* LCDVAT, LCDDAH, LCDDAV
* LCDXYP0, LCDXYP1, LCDSIZE0, LCDSIZE1
* LCDVSYNC, LCDHSYNC

4 Set DMAC.
* LCDIID
* LCDDA0, LCDSA0, LCDFID0, LCDCMD0, LCDOFFS0, LCDPW0, LCDCNUM0, LCDDESSIZE0

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* LCDDA1, LCDSA1, LCDFID1, LCDCMD1, LCDOFFS1, LCDPW1, LCDCNUM1, LCDDESSIZE1

5 Enable slcd DMA.

6 Enable LCDC.

18.6.2 Register Transfer Mode

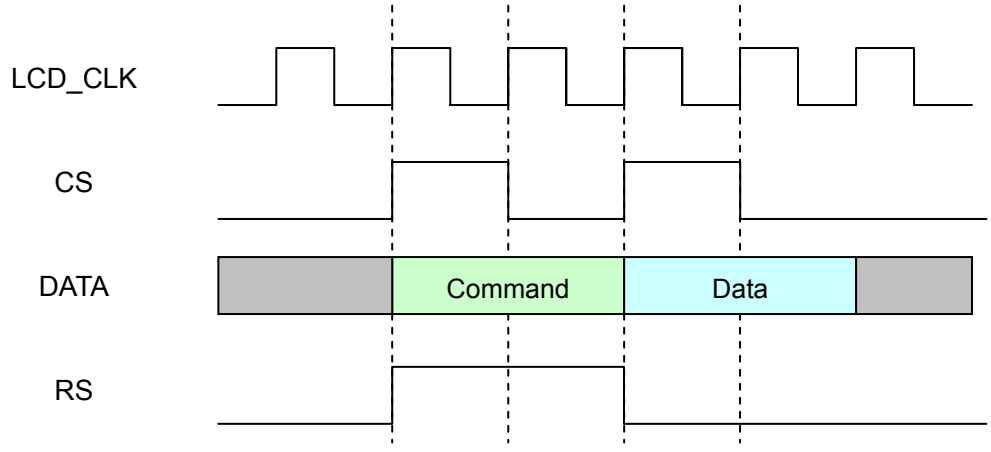
Each time you can write a command or a data to the register, then it will transfer the RS signal and data or command to LCM. Command and data can be recognized by RS bit coming from data register. The format of data register transfer can be as follows:



Command	RS [31] = 1	XXX [30:n+1]	Command [n:0]
Data	RS [31] = 0	XXX [30:24]	Data [23:0]
	RS [31] = 0	XXX [30:16]	Data [15:0]
	RS [31] = 0	XXX [30:9]	Data [8:0]
	RS [31] = 0	XXX [30:8]	Data [7:0]

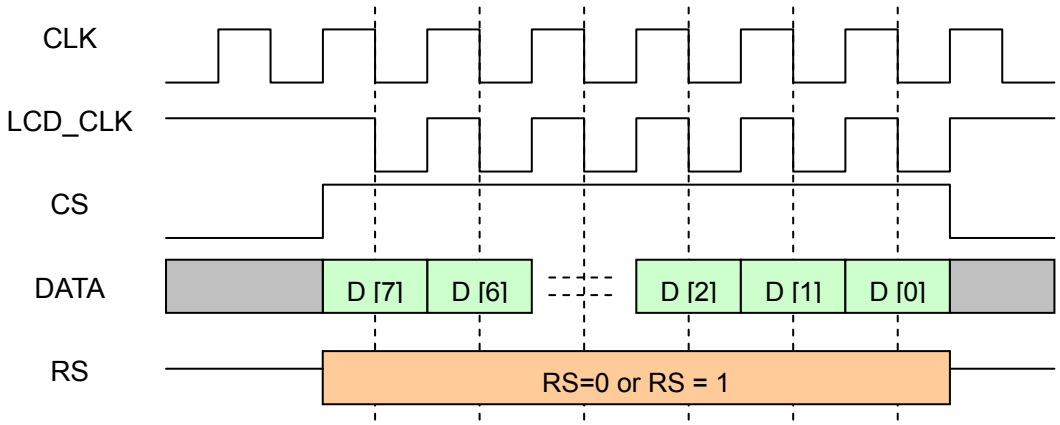
18.7 Timing

18.7.1 Parallel Timing



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18.7.2 Serial Timing



18.8 Operation Guide

18.8.1 DMA Operation

1 Start DMA transfer.

a Set LCDCFG.MODE to 1101 to choose LCM.

b Set LCDCTRL.BST to choose burst length for transferring.

c Set register LCDIID0, LCDDA0, LCDSA0, LCDFID0, LCDCMD0, LCDOFFS0, LCDPW0, LCDCNUM0, LCDDESSIZE0 to initial internal DMA.

d Also set register LCDIID1, LCDDA1, LCDSA1, LCDFID1, LCDCMD1, LCDOFFS1, LCDPW1, LCDCNUM1, LCDDESSIZE1 when use DMA channel 1 in OSD mode.

e Set MCFG to configure SLCDC.

f Before starting DMA, Wait for MSTATE.BUSY == 0.

g Set MCTRL.DMATXEN to 1 to prepare DMA transfer.

Note that if you don't want to stop DMA transfer, you need not to check MSTATE.BUSY.

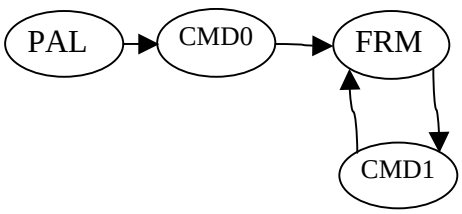
h Set LCDCCTRL.ENA to 1 to start LCDC internal DMA.

i The LCDC internal DMA will transfer data to SLCDC, and SLCDC transfer data to LCM.

Repeat this step till you want to close the SLCDC to transfer data to LCM Panel.

*please notice that use and only use DMA0 to transfer command no matter use DMA0 to transfer frame data or not.

One recommend descriptor chain (CMD0 with CNUM>0 and CMD1 with CNUM=0):



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2 Stop DMA transfer.

a Set LCDCCTRL.ENA to 0 to stop LCDC internal DMA at once.

b Wait till MSTATE.BUSY is set to 0 by hardware.
MSTATE.BUSY == 1: there is data in the FIFO waited for transferring to LCM.
MSTATE.BUSY == 0: all data in the FIFO have finished transferring to LCM.

c Set MCTRL.DMATXEN to 0 to stop DMA transfer.

3 Restart DMA transfer.

When MCTRL.DMATXEN is set to 0, and then you want to restart DMA transfer at once, you should ensure that MCTRL.DMATXEN must keep 0 at least three cycles of PIXCLK.

18.8.2 Register Operation

1 Set MCFG to configure SLCD.
2 Wait for MSTATE.BUSY == 0.
3 Set MDATA register.
4 Wait for MSTATE.BUSY == 0.
5 Set MDATA register.
6 Wait for MSTATE.BUSY == 0.
7 … …

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19 Decompresser

19.1 Overview

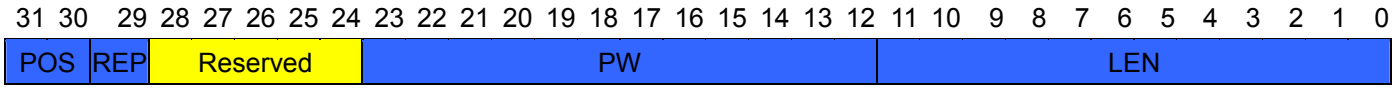
- Support bpp16 compressed data
- Support bpp24 compressed data with alpha
- Support bpp24 compressed data without alpha

19.2 Compress Method

Components

There are two kinds of Components in this method , one is command, the other is data .

Command:



Bits	Name	Description
31:30	POS	Position flag, indicates this command is in the head or middle or end of a giving line. Value / Description: 2'b00 Reserved 2'b01 This is the last command of the line 2'b10 This is sequent command of the line 2'b11 The is the first command of the line
29	REP	Repeated flag, indicates the following data is/are repeated or not , in another word , indicates the following data is/are compressed or original. 0: repeated 1: non-repeated
28:24	Reserve	All zero.
23:12	PW	Page width of current line. In the start cmd, it Indicates how many words in this line. In other cmd, it is zero.
11:0	LEN	Length , in repeated case, it indicates how many times the following data repeated; in non-repeated case , it indicates the number of following data frames. *in the case of compressed without alpha bpp24, this should be all zero.

*In the case of compressed without alpha bpp24, there is just start command , no sequent command and last command, the length is the high 8bits of every data.

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Data:

In the case of compressed without alpha bpp24, the length is the high 8bits of every data , other bits are original data.

In the case of compressed with alpha bpp24, the data is ARGB8888.

In the case of compressed bpp16, the data is RGB565 or RGB555, and should be word aligned.

Example

There is an example, in next page.

The first one of the following figures is compressed with alpha;

The second one of the following figures is compressed without alpha.

That is 7 x 4 picture.

The dummies will not be fetched by DMA.

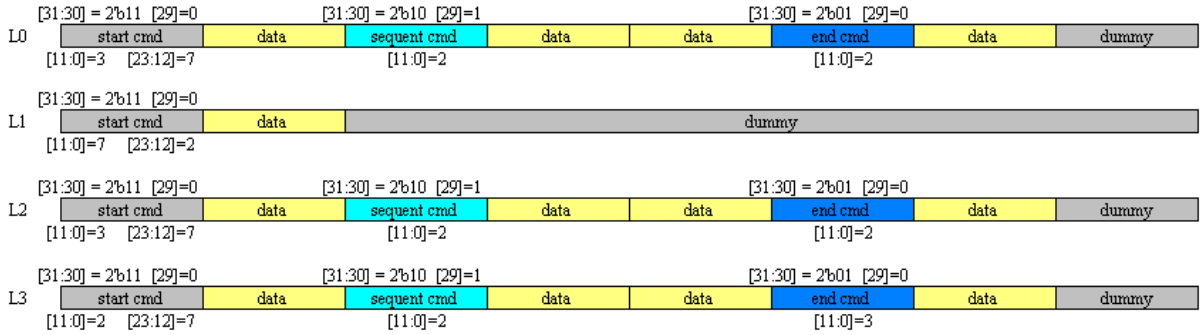
The first line contains 3 repeated pixels, 2 non-repeated pixels, and 2 repeated pixels;

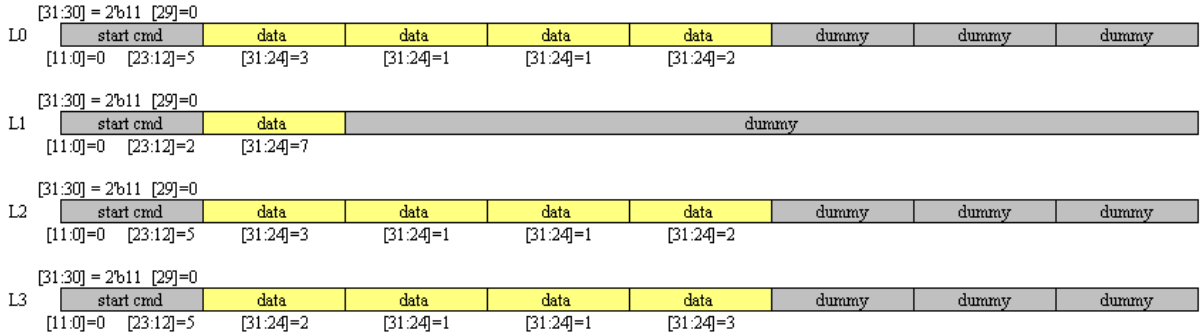
The second contains 7 repeated pixels;

The third line contains 3 repeated pixels , 2 non-repeated pixels, and 2 repeated pixels;

The last line contains 2 repeated pixels , 2 non-repeated pixels, and 3 repeated pixels.

:





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19.3 Operation Guide

The routine operations are the same as normal operations except descriptor operation:

1 Uncomp_en (LCDCMDx[27])should be set if decompressing function is used.
2 Uncomp_md(LCDCMDx[26])should be set if the frame is bpp24 without alpha compressed frame, otherwise, should be clear.
3 LCDPWx don't need to set value.
4 LEN (LCDCMDx[11:0]) should be set to the LPP value of the frame.
5 LCDOFFSx should be set to how many word in per line of frame buffer for compressed frame, count in word, 64-word align or 16-word align(depend on the configuration of aosd_comp).

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20 TV Encoder

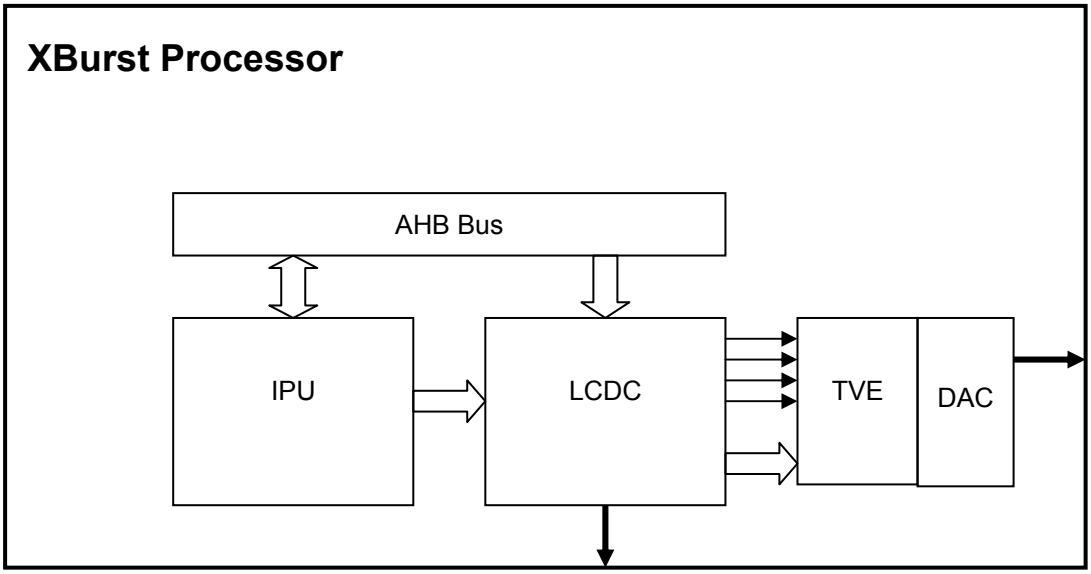
20.1 Overview

The TV Encoder enables the data for LCD panel showing in TV screen.
This release does not support S-video output.

Features:

- CVBS output
- PAL and NTSC supported

20.2 Structure



20.3 Pin Description

Table 20-1 TVE Pins Description

Name	I/O	Description	Interface
YCMP	AO	CVBS analog output	

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20.4 Register Description

TVE memory mapped registers are put together with LCD controller, occupied address area of 'H13050140 ~ 'H130501FF. Following table lists all the registers definition. All register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Size
TVECR	TV Encoder Control register	RW	0x01040301	0x13050140	32
FRCFG	Frame configure register	RW	0x00170271	0x13050144	32
SLCFG1	TV signal level configure register 1	RW	0x0320011A	0x13050150	32
SLCFG2	TV signal level configure register 2	RW	0x012800F0	0x13050154	32
SLCFG3	TV signal level configure register 3	RW	0x00000048	0x13050158	32
LTCFG1	Line timing configure register 1	RW	0x00143F4E	0x13050160	32
LTCFG2	Line timing configure register 2	RW	0x05A0103D	0x13050164	32
CFREQ	Chrominance sub-carrier frequency configure register	RW	0x2A098ACB	0x13050170	32
CPHASE	Chrominance sub-carrier phase configure register	RW	0x00000001	0x13050174	32
CCFG	Chrominance filter configure register	RW	0x3B3B8989	0x13050178	32
WSSCR	Wide screen signal control register	RW	0x00000070	0x13050180	32
WSSCFG1	Wide screen signal configure register 1	RW	0x00000000	0x13050184	32
WSSCFG2	Wide screen signal configure register 2	RW	0x00000000	0x13050188	32
WSSCFG3	Wide screen signal configure register 3	RW	0x00000000	0x1305018C	32

20.4.1 TV Encoder Control Register (TVECR)

This register is used to control TV encoder.

TVECR **0x13050140**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						YUV	ECVBS	Reserved			DAPD	Reserved	YCDLY			CGAIN		CBW		Reserved		SYNCT	PAL	FINV	ZBLACK	CR1ST	CLBAR	Reserved			SWRST
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25	YUV	Keep this bit zero.	RW

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<table>
<tr><td>24</td><td>ECVBS</td><td>Keep this bit one.</td><td>RW</td></tr>
<tr><td>23:21</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>20</td><td>DAPD</td><td>DAC power down. When it is 0, power down all DACs.</td><td>RW</td></tr>
<tr><td>19</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>18:16</td><td>YCDLY</td><td>(internal used only)</td><td>RW</td></tr>
<tr><td>15:14</td><td>CGAIN</td><td>Chrominance modulated signal gain factor setting when it is added to luminance signal in composite output format.
<table>
<tr><th>CGAIN</th><th>Description</th></tr>
<tr><td>00</td><td>1</td></tr>
<tr><td>01</td><td>1/4</td></tr>
<tr><td>10</td><td>1/2</td></tr>
<tr><td>11</td><td>3/4</td></tr>
</table></td><td>RW</td></tr>
<tr><td>13:12</td><td>CBW</td><td>Bandwidth setting for chrominance filter.
<table>
<tr><th>CBW</th><th>Description</th></tr>
<tr><td>00</td><td>Narrow band</td></tr>
<tr><td>01</td><td>Wide band</td></tr>
<tr><td>10</td><td>Extra wide band</td></tr>
<tr><td>11</td><td>Ultra wide band</td></tr>
</table></td><td>RW</td></tr>
<tr><td>11:10</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>9</td><td>SYNCT</td><td>Choose the sequence of field synchronizing pulses duration.
<table>
<tr><th>SYNCT</th><th>Description</th></tr>
<tr><td>0</td><td>The duration of sequence of field synchronizing pulses is 3 H, where H is a line period. Set SYNCT to this for NTSC TV set</td></tr>
<tr><td>1</td><td>The duration of sequence of field synchronizing pulses is 2.5 H. Set SYNCT to this for PAL TV set</td></tr>
</table></td><td>RW</td></tr>
<tr><td>8</td><td>PAL</td><td>Set this to 1 for PAL TV set, 0 for NTSC TV set.</td><td>RW</td></tr>
<tr><td>7</td><td>FINV</td><td>When this bit is 1, invert top and bottom fields.</td><td>RW</td></tr>
<tr><td>6</td><td>ZBLACK</td><td>Black of luminance (Y) input is 0. Set this bit to 1 if the input video luminance data for black is 0. Set this bit to 0 if the input video luminance data for black is 16. When this bit is 0, the Y input data will be clamped to ≥ 16.</td><td>RW</td></tr>
<tr><td>5</td><td>CR1ST</td><td>This bit described the Cb and Cr data order in input video.
<table>
<tr><th>ECVBS</th><th>Description</th></tr>
<tr><td>0</td><td>Cb comes before Cr, which is ITU656 standard</td></tr>
<tr><td>1</td><td>Cr comes before Cb</td></tr>
</table></td><td>RW</td></tr>
<tr><td>4</td><td>CLBAR</td><td>Color bar mode. In this mode, a color bar picture is output to TV.
<table>
<tr><th>CLBAR</th><th>Description</th></tr>
<tr><td>0</td><td>Output input video to TV</td></tr>
<tr><td>1</td><td>Output color bar to TV</td></tr>
</table></td><td>RW</td></tr>
</table>

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3:1	Reserved	Writing has no effect, read as zero.	R
0	SWRST	Software reset. When set this bit to 1, TVE is reset.	RW

20.4.2 Frame configure register (FRCFG)

This register is used to configure line in a frame.

FRCFG **0x13050144**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								L1ST								Reserved						NLINE									
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	L1ST	This field defines the first active video line of a field. The reset value is 23 in decimal. The frame active video line number is (NLINE – 1 – 2 * L1ST). The top and bottom field line number is a half of the frame line number.	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	NLINE	This field defines number of lines per-frame. The reset value is **625** in decimal.	RW

20.4.3 Signal level configure register 1, 2 and 3 (SLCFG1, SLCFG2, SLCFG3)

These registers are used to configure the TV signal level in difference phases.

SLCFG1 **0x13050150**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						WHITEL										Reserved						BLACKL									
RST	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	WHITEL	Signal level for white color. The reset value is 800 in decimal.	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	BLACKL	Signal level for black color. The reset value is 282 in decimal.	RW

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SLCFG2 **0x13050154**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						VBLANKL										Reserved						BLANKL									
RST	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	VBLANKL	Signal level in vertical blank period. The reset value is 296 in decimal.	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	BLANKL	Signal level in other blank period. The reset value is 240 in decimal.	RW

SLCFG3 **0x13050158**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SYNCL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SYNCL	Signal level in sync period. The reset value is 72 in decimal.	RW

20.4.4 Line timing configure register 1 and 2 (LTCFG1, LTCFG2)

These registers are used to configure timing period in a line.

LTCFG1 **0x13050160**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											FRONTP					Reserved	HSYNCW							Reserved	BACKP						
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	1	1	0	1	0	0	1	1	1	0

Bits	Name	Description	RW
31:21	Reserved	Writing has no effect, read as zero.	R
20:16	FRONTP	Front porch width, 16 cycles of 13.5MHz for 525 line system and 20 cycles for 625 line.	RW
15	Reserved	Writing has no effect, read as zero.	R
14:8	HSYNCW	HSYNC width in cycles of 13.5MHz. The reset value is 63 in decimal.	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	BACKP	Back porch width in cycles of 13.5MHz. The reset value is 78 in decimal.	RW

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LTCFG2 0x13050164

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					ACTLIN											Reserved			PREBW					Reserved						BURSTW		
RST	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0	1

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	ACTLIN	Active line length in cycles of 27MHz. The reset value is 1440 in decimal, which represent 720 pixels per line.	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:8	PREBW	Pre-burst width. The width after HSYNC and before the burst signals of back porch in cycles of 27MHz. The reset value is **16** in decimal.	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	BURSTW	The sub-carrier burst width inside back porch in cycles of 27MHz. The reset value is **61** in decimal.	RW

20.4.5 Chrominance configure registers (CFREQ, CPHASE, CFCFG)

This register is used to define chrominance sub-carrier frequency.

CFREQ 0x13050170

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFREQ																															
RST	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	1	0	1	0	1	1	0	0	1	0	1	1

Bits	Name	Description	RW
32	CFREQ	Chrominance sub-carrier frequency.	RW

This register is used to define chrominance sub-carrier phase.

CPHASE 0x13050174

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INITPH								ACTPH								Reserved															CCRSTP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:24	INITPH	Initial phase of chrominance sub-carrier. Corresponding to upper 8	RW

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		bits of CFREQ.	
23:16	ACTPH	This is added to chrominance sub-carrier angle (corresponding to upper 8 bits of CFREQ) in case of active video period.	RW
15:2	Reserved	Writing has no effect, read as zero.	R
1:0	CCRSTP	Chrominance clock reset period. After the reset, chrominance clock is set to INITPH. Besides this, chrominance clock is reset also to INITPH in case of chip reset. **CCRSTP** / **Description** 00 — Every 8 field 01 — Every 4 fields 10 — Every 2 lines 11 — Never	RW

This register is used to configure chrominance filter.

CCFG **0x13050178**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CBBA								CRBA								CBGAIN								CRGAIN							
RST	0	0	1	1	1	0	1	1	0	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1

Bits	Name	Description	RW
31:24	CBBA	Cb amplitude for burst period. The reset value is 59 in decimal, which corresponding to 59*4 = 236 ≈ (WHITEL – BLANKL) * 4 / 10 (±10%) = 224 ± 22 ≈ (WHITEL – BLANKL) * 3 / 7 (±3%) = 240 ± 7	RW
23:16	CRBA	Cr amplitude for burst period. The reset value is 59 in decimal. In PAL mode CRBA value is 59 in decimal and in NTSC mode CRBA value is 0 in decimal.	RW
15:8	CBGAIN	Cb gain. The reset value is 137 in decimal. CBGAIN=128 means no changing to the incoming Cb data.	RW
7:0	CRGAIN	Cr gain. The reset value is 137 in decimal. CRGAIN=128 means no changing to the incoming Cr data.	RW

20.5 Switch between LCD panel and TV set

LCD panel ➔ TV set switch

Step 1. Configure TVE (CVBS, N/P, and etc), enable DAC.

Step 2. Disable LCDC. If data is from IPU, stop IPU. Then LCD panel is turned off.

Step 3. Configure LCDC for output via TVE.

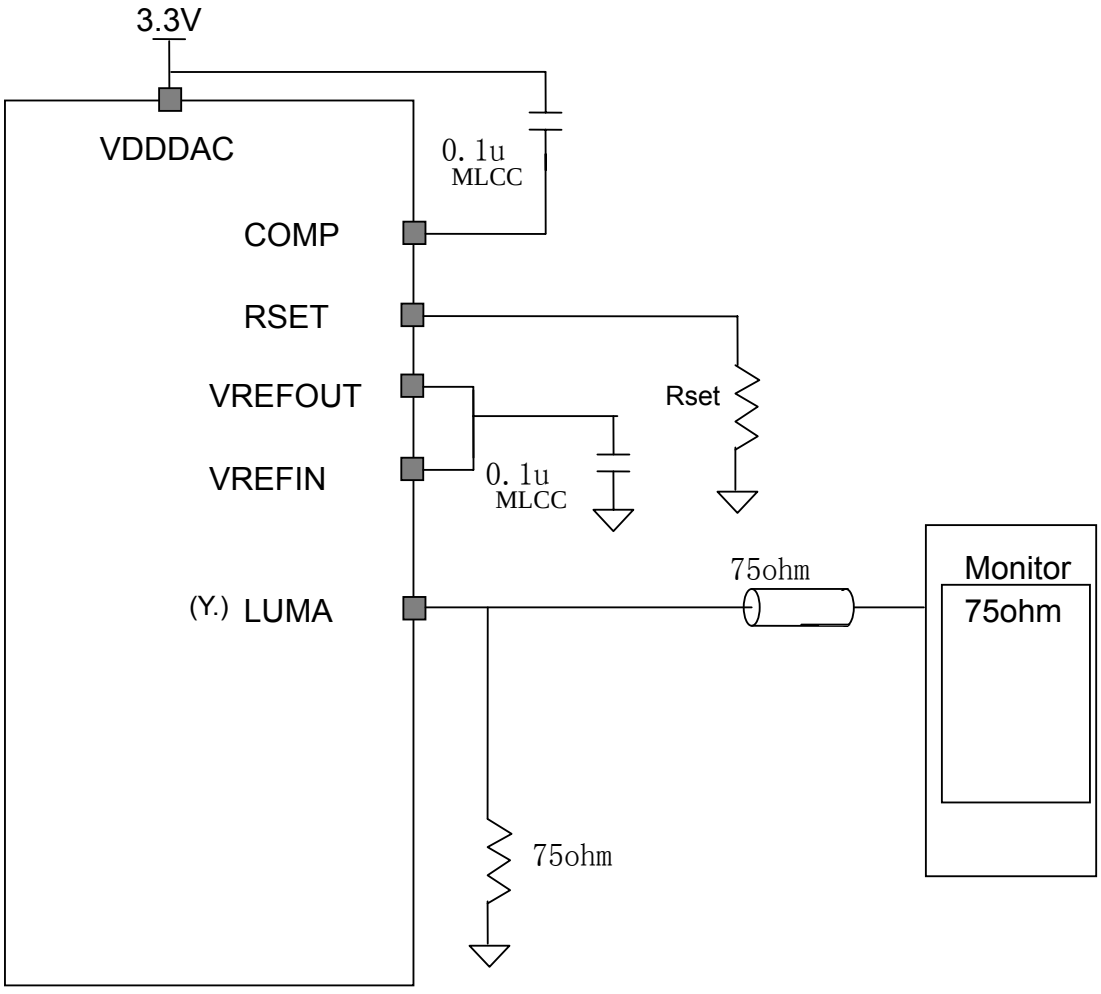
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Step 4. Configure TVE and LCDC pixel clock and enable TVE clock (CPM).
Step 5. If data is from IPU, start IPU. Then start LCDC.
Step 6. Enable TVE (TVECR.SWRST=0). Then data stream from LCDC is output to TV set via TVE.

TV set ➔ LCD panel switch
Step 1. Disable TVE (TVECR.SWRST=1). Then no signal is output to TV set.
Step 2. Disable TVE clock (CPM), and disable DAC.
Step 3. Disable LCDC. If data is from IPU, stop IPU.
Step 4. Configure LCDC pixel clock. Configure LCDC for output to LCD panel.
Step 5. If data is from IPU, start IPU. Start LCDC. Then LCD panel is work.

20.6 DAC

20.6.1 DAC Connection



Full-Scale adjust resistor. A resistor (RSET) connected between this the magnitude of the full-scale video signal. RSET (ohm) = VREFIN(V)* 10.5/ IOFS (A), where IOFS is

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full-scale output current per channel under the conditions of IREN =0, andSOGEN = 0.

20.6.2 DAC DC Character

VDDDAC =3.3V; DVDD=1.2V; RL=37.5ohm, CL=10Pf; Temp = 25℃.

Parameter	Symbol	Min	Type	Max	Unit
Operating voltage range	VDDDAC	3.0	3.3	3.6	V
Max output voltage	DVDD	1.08	1.20	1.32	V
DAC resolution		--	10	--	bits
Integral non-linearity error	INL	-1.2	-0.6~+0.6	+1.2	LSB
Differential non-linearity er	DNL	-1.2	-0.6~+0.6	+1.2	LSB

20.6.3 DAC Power Down Setup Time

As the output current's max value per channel is 34.1mA, keep the DAC power down when you not use TV encoder.

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21 EPD Controller

21.1 Overview

The controller provides a low cost SOC solution for EPD applications.

Features:

- Supports PVI and AUO compatible EPD panels
- Supports different size up to 1024x768
- Supports 2/4/5 bits grayscale and color display
- Supports up to 8 multi-zone concurrent updating
- Supports hand-writing mode
- Supports SW LUT algorithm

21.2 EPDC Pin Mappings

Table 21-1 EPDC Pin Mapping

PVI	AUO	PIN
GDCLK	YCLK	LCD_VSYN_PC19
GDRL	UD	LCD_B0_LCD_REV_PC00
GDSP	YDIOU	LCD_B1_LCD_PS_PC01
GDOE	YOE	LCD_B2_PC02
SDCLK	XCLK	LCD_PCLK_PC08
SDOE		LCD_DE_PC09
SDLE	LD	LCD_HSYN_PC18
SDRL	RL	LCD_B3_PC03
SDCE [7]	YDIOD	LCD_R1_PC21
SDCE [6]	VCOM[1]	LCD_R0_LCD_CLS_UART4_RXD_PC20
SDCE [5]	VCOM[0]	CIM_D5_EPD_SCE5__PB15
SDCE [4]		CIM_D4_EPD_SCE4__PB14
SDCE [3]		CIM_D3_EPD_SCE3__PB1
SDCE [2]		CIM_D2_EPD_SCE2__PB12
SDCE [1]	XDIOR	LCD_G1_PC11
SDCE [0]	XDIOL	LCD_G0_LCD_SPL_UART4_TXD_PC10
SDDO [15]	DATA [15]	LCD_R7_PC27
SDDO [14]	DATA [14]	LCD_R6_PC26
SDDO [13]	DATA [13]	LCD_R5_PC25
SDDO [12]	DATA [12]	LCD_R4_PC24

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SDDO [11]	DATA [11]	LCD_R3_PC23
SDDO [10]	DATA [10]	LCD_R2_PC22
SDDO [9]	DATA [9]	LCD_G7_PC17
SDDO [8]	DATA [8]	LCD_G6_PC16
SDDO [7]	DATA [7]	LCD_G5_PC15
SDDO [6]	DATA [6]	LCD_G4_PC14
SDDO [5]	DATA [5]	LCD_G3_PC13
SDDO [4]	DATA [4]	LCD_G2_PC12
SDDO [3]	DATA [3]	LCD_B7_PC07
SDDO [2]	DATA [2]	LCD_B6_PC06
SDDO [1]	DATA [1]	LCD_B5_PC05
SDDO [0]	DATA [0]	LCD_B4_PC04
PWRCOM		CIM_MCLK_EPD_PWC_PB09
PWR7	PWR7	AIC0_SDATO_EPD_PWR7_PE07
PWR6	PWR6	AIC0_SDATI_EPD_PWR6_PE06
PWR5	PWR5	LRCLK0_EPD_PWR5_PD13
PWR4	PWR4	UART3_RXD_BCLK0_EPD_PWR4_PD12
PWR3	PWR3	CIM_D7_EPD_PWR3_PB17
PWR2	PWR2	CIM_D6_EPD_PWR2_PB16
PWR1	PWR1	CIM_D1_EPD_PWR1_PB11
PWR0	PWR0	CIM_D0_EPD_PWR0_PB10
BD[3]	BD[3]	TSDI5_EPD_BD3_PB25
BD[2]	BD[2]	TSDI4_EPD_BD2_PB24
BD[1]	BD[1]	TSDI3_EPD_BD1_PB23
BD[0]	BD[0]	TSDI2_EPD_BD0_PB22

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21.3 Function Block Diagram

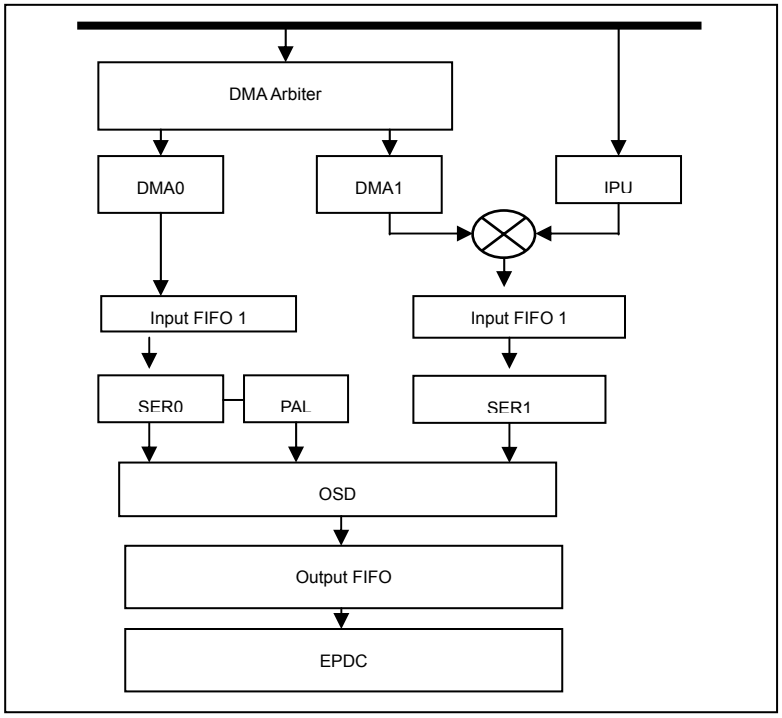


Figure 21-1 EPDC Function Diagram

21.4 EPD Controller Registers

Table 21-2 EPD Controller Registers

Name	Address	Reset Value	Access Size	RW
EPDC_CTRL	0x13050200	0x00000000	32	RW
EPDC_STA	0x13050204	0x00000000	32	R
EPDC_ISR	0x13050208	0x00000000	32	RW
EPDC_CFG0	0x1305020C	0x00000000	32	RW
EPDC_CFG1	0x13050210	0x00000000	32	RW
EPDC_PPL0	0x13050214	0x00000000	32	RW
EPDC_PPL1	0x13050218	0x00000000	32	RW
EPDC_VAT	0x1305021C	0x00000000	32	RW
EPDC_DAV	0x13050220	0x00000000	32	RW
EPDC_DAH	0x13050224	0x00000000	32	RW
EPDC_VSYN	0x13050228	0x00000000	32	RW
EPDC_HSYN	0x1305022C	0x00000000	32	RW
EPDC_GDCLK	0x13050230	0x00000000	32	RW
EPDC_GDOE	0x13050234	0x00000000	32	RW

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EPDC_GDSP	0x13050238	0x00000000	32	RW
EPDC_SDOE	0x1305023C	0x00000000	32	RW
EPDC_SDSP	0x13050240	0x00000000	32	RW
EPDC_PMGR0	0x13050244	0x00000000	32	RW
EPDC_PMGR1	0x13050248	0x00000000	32	RW
EPDC_PMGR2	0x1305024C	0x00000000	32	RW
EPDC_PMGR3	0x13050250	0x00000000	32	RW
EPDC_PMGR3	0x13050254	0x00000000	32	RW
EPDC_VCOM0	0x13050258	0x00000000	32	RW
EPDC_VCOM1	0x1305025C	0x00000000	32	RW
EPDC_VCOM2	0x13050260	0x00000000	32	RW
EPDC_VCOM3	0x13050264	0x00000000	32	RW
EPDC_VCOM4	0x13050268	0x00000000	32	RW
EPDC_VCOM5	0x1305026C	0x00000000	32	RW
EPDC_BORDR	0x13050270	0x00000000	32	RW
EPDC_HWPAL	0x1305027C	0x00000000	32	RW
EPDC_PPL0_POS	0x13050280	0x00000000	32	RW
EPDC_PPL0_SIZE	0x13050284	0x00000000	32	RW
EPDC_PPL1_POS	0x13050288	0x00000000	32	RW
EPDC_PPL1_SIZE	0x1305028C	0x00000000	32	RW
EPDC_PPL2_POS	0x13050290	0x00000000	32	RW
EPDC_PPL2_SIZE	0x13050294	0x00000000	32	RW
EPDC_PPL3_POS	0x13050298	0x00000000	32	RW
EPDC_PPL3_SIZE	0x1305029C	0x00000000	32	RW
EPDC_PPL4_POS	0x130502A0	0x00000000	32	RW
EPDC_PPL4_SIZE	0x130502A4	0x00000000	32	RW
EPDC_PPL5_POS	0x130502A8	0x00000000	32	RW
EPDC_PPL5_SIZE	0x130502AC	0x00000000	32	RW
EPDC_PPL6_POS	0x130502B0	0x00000000	32	RW
EPDC_PPL6_SIZE	0x130502B4	0x00000000	32	RW
EPDC_PPL7_POS	0x130502B8	0x00000000	32	RW
EPDC_PPL7_SIZE	0x130502BC	0x00000000	32	RW

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21.5 Registers Description

21.5.1 EPDC Control Registers

EPDC_CTRL **0x13050200**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PPL7_FRM_INTE	PPL6_FRM_INTE	PPL5_FRM_INTE	PPL4_FRM_INTE	PPL3_FRM_INTE	PPL2_FRM_INTE	PPL1_FRM_INTE	PPL0_FRM_INTE	Reserved	FRM_VCOM_INTE	IMG_DONE_INTE	FRM_DONE_INTE	FRM_ABT_INTE	PWR_OFF_INTE	PWR_ON_INTE	DMA_DONE_INTE	PPL7_FRM_ENA	PPL6_FRM_ENA	PPL5_FRM_ENA	PPL4_FRM_ENA	PPL3_FRM_ENA	PPL2_FRM_ENA	PPL1_FRM_ENA	PPL0_FRM_ENA	IMG_RFE_ABT	IMG_REF_ENA	PWROFF	PWRON	Reserved		EPD_DMA_MODE	EPD_ENA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PPL7_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
30	PPL6_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
29	PPL5_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
28	PPL4_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
27	PPL3_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
26	PPL2_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
25	PPL1_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
24	PPL0_FRM_INTE	PPL7_FRM_INT interrupt enable.	RW
23	Reserved	Writing has no effect, read as zero.	R
22	FRM_VCOM_INTE	FRM_VCOM_INT interrupt enable.	RW
21	IMG_DONE_INTE	IMG_DONE_INT interrupt enable.	RW
20	FRM_DONE_INTE	FRM_DONE_INT interrupt enable.	RW
19	FRM_ABT_INTE	FRM_ABT_INT interrupt enable.	RW
18	PWR_OFF_INTE	PWR_OFF_INT interrupt enable.	RW
17	PWR_ON_INTE	PWR_ON_INT interrupt enable.	RW
16	DMA_DONE_INTE	DMA_DONE_INT interrupt enable.	RW
15	PPL7_FRM_ENA	Enable the 8th pipeline updating, cleared by HW when it finished.	RW
14	PPL6_FRM_ENA	Enable the 7th pipeline updating, cleared by HW when it finished.	RW
13	PPL5_FRM_ENA	Enable the 6th pipeline updating, cleared by HW when it finished.	RW
12	PPL4_FRM_ENA	Enable the 5th pipeline updating, cleared by HW when it finished.	RW
11	PPL3_FRM_ENA	Enable the 4th pipeline updating, cleared by HW when it finished.	RW
10	PPL2_FRM_ENA	Enable the 3rd pipeline updating, cleared by HW when it finished.	RW
9	PPL1_FRM_ENA	Enable the 2nd pipeline updating, cleared by HW when it finished.	RW
8	PPL0_FRM_ENA	Enable the 1st pipeline updating, cleared by HW when it finished.	RW
7	IMG_REF_ABT	Abort current image updating, cleared by HW when it finished.	RW
6	IMG_REF_ENA	Start to update the image, cleared by HW when it finished.	RW
5	PWROFF	Start the power off sequence, cleared by HW when it finished.	RW

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4	PWRON	Start the power on sequence, cleared by HW when it finished.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	EPD_DMA_MODE	1: The DMA will stop at the last frame data has been loaded; 0: The DMA will stop at end of each frame data has been loaded. It is available when DMAMODE in LCD MCTRL set to 1.	RW
0	EPD_ENA	Enable EPD controller.	RW

21.5.2 EPDC Status Register

EPDC_STA **0x13050204**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CUR_TOT_FRM																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CUR_TOT_FRM	The numbers of frames have been processed in current operation, including border updating.	RW

21.5.3 EPDC ISR Register

EPD_ISR **0x13050208**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PPL7_FRM_INT	PPL6_FRM_INT	PPL5_FRM_INT	PPL4_FRM_INT	PPL3_FRM_INT	PPL2_FRM_INT	PPL1_FRM_INT	PPL0_FRM_INT	Reserved	FRM_VCOM_INT	IMG_DONE_INT	FRM_DONE_INT	FRM_ABT_INT	PWR_OFF_INT	PWR_ON_INT	DMA_DONE_INT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	PPL7_FRM_INT	The 8th pipeline interrupt.	RW
14	PPL6_FRM_INT	The 7th pipeline interrupt.	RW
13	PPL5_FRM_INT	The 6th pipeline interrupt.	RW
12	PPL4_FRM_INT	The 5th pipeline interrupt.	RW
11	PPL3_FRM_INT	The 4th pipeline interrupt.	RW
10	PPL2_FRM_INT	The 3rd pipeline interrupt.	RW
9	PPL1_FRM_INT	The 2nd pipeline interrupt.	RW

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8	PPL0_FRM_INT	The 1st pipeline interrupt.	RW
7	Reserved	Writing has no effect, read as zero.	R
6	FRM_VCOM_INT	This interrupt will be asserted when frame counter reaches 95 at current updating. It means SW should update EPDC_VCOM0~5 if necessary. It is available when need more than 96 frames to update an image or text.	RW
5	IMG_DONE_INT	It interrupt will be asserted when all pipelines completed.	RW
4	FRM_DONE_INT	It interrupt will asserted when each frame.	RW
3	FRM_ABT_INT	This interrupt will be asserted when abort current display updating completed.	RW
2	PWR_OFF_INT	It interrupt will be asserted when perform power off sequence completed.	RW
1	PWR_ON_INT	This interrupt will be asserted when perform power on sequence completed.	RW
0	DMA_DONE_INT	This interrupt will be asserted when last frame data loaded by DMA.	RW

21.5.4 EPDC Configuration Register 0

EPDC_CFG0 **0x1305020C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DUAL_GATE	COLOR_MODE	COLOR_FMT			SDSP_CAS	SDSP_MODE	GDCLK_MODE	GDOE_MODE		GDUD	SDRL	GDCLK_POL	GDOE_POL	GDSP_POL	SDCLK_POL	SDOE_POL	SDSP_POL	SDCE_POL	SDLE_POL	Reserved		GDSP_CAS	Reserved					EPD_OBPP			EPD_OMODE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DUAL_GATE	Dual Gate Mode for some AUO EPD.	RW
30	COLOR_MODE	Color or mono mode selection.	RW
29:27	COLOR_FMT	Source Driver data format when in color mode.	RW
26	SDSP_CAS	It means output start pulse for Source Drivers cascading from XDIOR or XDIOL depending on data shift direction.	RW
25	SDSP_MODE	It means output start pulse for Source Drivers to start line a line data, or using chip enable for data sampling.	RW
24	GDCLK_MODE	0: GDCLK will be terminated when the last line data output, 1: GDCLK will last another line when outputted the last line data. For PVI EPD, it always should be set to 1; for AUO EPD, set it to 0 for normal mode and set it to 1 for fast mode.	RW
23:22	Reserved	Writing has no effect, read as zero.	R

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21	GDUD	Up/Down pulse direction control and setting concatenating sequence for the Gate Driver.	RW
20	SDRL	Left/Right pulse direction control and setting concatenating sequence for the Source Driver.	RW
19	GDCLK_POL	Polarity of Gate Driver clock.	RW
18	GDOE_POL	Polarity of Gate Driver output enable.	RW
17	GDSP_POL	Polarity of Gate Driver start pulse.	RW
16	SDCLK_POL	Source Driver clock sample edge selection. 0: sample data at rising edge 1: sample data at falling edge	RW
15	SDOE_POL	Polarity of Source Driver output enable.	RW
14	SDSP_POL	Polarity of Source Driver start pulse.	RW
13	SDCE_POL	Polarity of Source Drivers chip enable.	RW
12	SDLE_POL	Polarity of Source Driver data latch signal.	RW
11:10	Reserved	Writing has no effect, read as zero.	R
9	GDSP_CAS	It means output start pulse for Gate Drivers cascading from YDIOU or YDIOD depending on data shift direction.	RW
8:4	Reserved	Writing has no effect, read as zero.	R
3:1	EPD_OBPP	Bits per pixel for Source Driver. 1: 2 bits per pixel 2: 4 bits per pixel others reserved	RW
0	EPD_OMODE	The Source Driver data bus width. 0: 8-bit 1: 16-bit	RW

21.5.5 EPDC Configuration Register 1

EPDC_CFG1 **0x13050210**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SDDO_REV	PDAT_SWAP	SDCE_REV	Reserved			SDOS									PDAT								SDCE_STN				SDCE_NUM			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	SDDO_REV	Set it to reverse pixels arrangement output to Source Driver. For instance, if SDDO_REV = 0, EPD_OBPP = 1, EPD_OMODE = 0, controller will output 4 pixels in each SDCLK in the format: [P3,	RW

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		P2, P1, P0]. But if SDDO_REV = 1, then the output looks like [P0, P1, P2, P3].	
29	PDAT_SWAP	Swap padding data or not, using it with SDRL in following combinations: PDAT_SWAP = 0, SDRL = 0: padding after the display data PDAT_SWAP = 0, SDRL = 1: padding before the display data PDAT_SWAP = 1, SDRL = 0: padding before the display data PDAT_SWAP = 1, SDRL = 1: padding after the display data	RW
28	SDCE_REV	If Source Driver using chip enable, set it will reverse chips enable sequence, using it with SDCE_STN and SDCE_NUM. For instance, if SDCE_NUM = 4, SDCE_STN = 0, controller output chips enable [SDCE0, SDCE1, SDCE2, SDCE3] in order. But if SDCE_REV = 1, outputs will be [SDCE3, SDCE2, SDCE1, SDCE0].	RW
27:25	Reserved	Writing has no effect, read as zero.	R
24:16	SDOS	It is available when Source Driver using chip enable. SDOS = (Single Source Driver output size) / (Pixels per Clock)	RW
15:8	PDAT	Source Driver padding data, only available when Source Driver use chip enable. PDAT = (Source Driver Output Size * Number – Line Display Size) / (Pixels per Clock)	RW
7:4	SDCE_STN	Source Driver start number, only available when Source Driver use chip enables.	RW
3:0	SDCE_NUM	Source Driver total number, only available when Source Driver use chip enables.	RW

21.5.6 EPDC Pipeline Frame Register 0

EPDC_PPL0 **0x13050214**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PPL3_FRM_NUM								PPL2_FRM_NUM								PPL1_FRM_NUM								PPL0_FRM_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	PPL3_FRM_NUM	The 4th pipeline frame number.	RW
23:16	PPL2_FRM_NUM	The 3rd pipeline frame number.	RW
15:8	PPL1_FRM_NUM	The 2nd pipeline frame number.	RW
7:0	PPL0_FRM_NUM	The 1st pipeline frame number.	RW

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21.5.7 EPDC Pipeline Frame Register 1

EPDC_PPL1 **0x13050218**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PPL7_FRM_NUM								PPL6_FRM_NUM								PPL5_FRM_NUM								PPL4_FRM_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	PPL7_FRM_NUM	The 8th pipeline frame number.	RW
23:16	PPL6_FRM_NUM	The 7th pipeline frame number.	RW
15:8	PPL5_FRM_NUM	The 6th pipeline frame number.	RW
7:0	PPL4_FRM_NUM	The 5th pipeline frame number.	RW

21.5.8 EPDC Virtual Display Area Setting Register

EPDC_VAT **0x1305021C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								VT								Reserved				HT											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VT	The period of each frame in lines.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HT	The period of each line in SDCLK.	RW

21.5.9 EPDC Vertical Display Area Setting Register

EPDC_DAV **0x13050220**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								VDE								Reserved				VDS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VDE	The line number at which each frame displays data ends.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDS	The line number at which each frame displays data starts.	RW

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21.5.10 EPDC Horizontal Display Area Setting Register

EPDC_DAH **0x13050224**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HDE												Reserved				HDS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HDE	The position at which each line displays data ends.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HDS	The position at which each line displays data starts.	RW

21.5.11 EPDC Vertical Synchronous Start Pulse Setting

EPDC_VSYN **0x13050228**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				VPE												Reserved				VPS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VPE	The last line number for Gate Driver generating start pulse.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VPS	The first line number for Gate Driver generating start pulse.	RW

21.5.12 EPDC Horizontal Synchronous Start Pulse Setting

EPDC_HSYN **0x1305022C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HPE												Reserved				HPS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HPE	The position at which Source Driver data latch signal de-asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HPS	The position at which Source Driver data latch signal asserts.	RW

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21.5.13 EPDC Gate Driver Clock Setting Register

EPDC_GDCLK **0x13050230**

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	GDCLK_DIS	Reserved	GDCLK_ENA
RST	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	GDCLK_DIS	The position at which Gate Driver clock signal de-asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	GDCLK_ENA	The position at which Gate Driver clock signal asserts.	RW

21.5.14 EPDC Gate Output Enable Setting Register

EPDC_GDOE **0x13050234**

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	GDOE_DIS	Reserved	GDOE_ENA
RST	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	GDOE_DIS	The position at which Gate Driver output enable signal de-asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	GDOE_ENA	The position at which Gate Driver output enable signal asserts.	RW

21.5.15 EPDC Gate Driver Start Pulse Setting

EPDC_GDSP **0x13050238**

Bit	31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	GDSP_DIS	Reserved	GDSP_ENA
RST	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	GDSP_DIS	The position at which Gate Driver start pulse signal de-asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	GDSP_ENA	The position at which Gate Driver start pulse signal asserts.	RW

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21.5.16 EPDC Source Driver Output Enable Setting Register

EPD_SDOE **0x1305023C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SDOE_DIS												Reserved				SDOE_ENA											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	SDOE_DIS	The position at which Source Driver output enable signal de-asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	SDOE_ENA	The position at which Source Driver output enable signal asserts.	RW

21.5.17 EPDC Source Driver Start Pulse Setting Register

EPDC_SDSP **0x13050240**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SDSP_DIS												Reserved				SDSP_ENA											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	SDSP_DIS	The position at which Source Driver start pulse signal asserts.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	SDSP_ENA	The position at which Source Driver start pulse signal de-asserts.	RW

21.5.18 EPDC Power Management Registers 0

EPDC_PMGR0 **0x13050244**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PWR_DLY12												Reserved				PWR_DLY01											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PWR_DLY12	The delay time in line between PWR [1] and PWR [2].	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PWR_DLY01	The delay time in line between PWR [0] and PWR [1].	RW

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21.5.19 EPDC Power Management Registers 1

EPDC_PMGR1 **0x13050248**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PWR_DLY34												Reserved				PWR_DLY23											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PWR_DLY34	The delay time in lines between PWR [3] and PWR [4].	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PWR_DLY23	The delay time in lines between PWR [2] and PWR [3].	RW

21.5.20 EPDC Power Management Registers 2

EPDC_PMGR2 **0x1305024C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PWR_DLY56												Reserved				PWR_DLY45											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PWR_DLY56	The delay time in lines between PWR [5] and PWR [6].	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PWR_DLY45	The delay time in lines between PWR [4] and PWR [5].	RW

21.5.21 EPDC Power Management Registers 3

EPDC_PMGR3 **0x13050250**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VCOM_IDLE	PWRCOM_POL	UNI_POL	PPL7_BDR_ENA	BDR_LEVEL	BDR_IDLE	PWR_POL										Reserved				PWR_DLY67											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:30	VCOM_IDLE	VCOM [1:0] default value when idle.	RW
29	PWRCOM_POL	The polarity of PWRCOM.	RW
28	UNIPOL	This bit choose PWRCOM or VCOM [1:0] as common voltage control signals of Source Driver. 0: VCOM [1:0] 1: PWRCOM	RW
27	PPL7_BDR_ENA	The 7th pipeline used for border updating or not.	RW
26	BDR_LEVEL	Border voltage control level setting. 0:2 bits 1:4 bits	RW
25:24	BDR_IDLE	Border voltage control signals default value when idle.	RW
23:16	PWR_POL	Polarity of PWR7~0.	R
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PWR_DLY67	The delay time in lines between PWR [6] and PWR [7].	RW

21.5.22 EPDC Power Management Registers 4

EPDC_PMGR4 **0x13050254**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								PWR_ENA								Reserved								PWR_VAL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	PWR_ENA	These bits enable PWR7~0 individually.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWR_VAL	The PWR [x] pin value individually if it is not enabled.	RW

21.5.23 EPDC VCOM Registers 0~5

EPDC_VCOM0, EPDC_VCOM1, EPDC_VCOM1 **0x13050258, 0x1305025C, 0x13050260**

EPDC_VCOM3, EPDC_VCOM4, EPDC_VCOM5 **0x13050264, 0x13050268, 0x1305026C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VCOM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	VCOM	The VCOM [1:0] of each frame up to 16-frames, EPDC_VCOM0	RW

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		contains the first 16 frames of VCOM[1:0]. EPDC_VCOM0: 16~1 EPDC_VCOM1: 32~17 EPDC_VCOM2: 48~33 EPDC_VCOM3: 64~49 EPDC_VCOM4: 80~65 EPDC_VCOM5: 96~81	

21.5.24 EPDC Border Voltage Setting Registers

	EPDC_BORDR																															
																		0x13050270														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BORDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	BORDR	These bits set border voltage control signals in each frame. If BDR_LEVEL = 0, it contains up to 16 frames, but if BDR_LEVEL = 1, it contains only 8 frames.	RW

21.5.25 EPDC Handwriting Mode Setting

	EPDC_HWPAL																															
																															0x1305027C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PPL7_HW_MODE	PPL6_HW_MODE	PPL5_HW_MODE	PPL4_HW_MODE	PPL3_HW_MODE	PPL2_HW_MODE	PPL1_HW_MODE	PPL0_HW_MODE	PPL_HW_COLOR															PAL_ADDR_OFF										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PPL7_HW_MODE.	The 8th pipeline handwriting mode.	RW
30	PPL6_HW_MODE.	The 7th pipeline handwriting mode.	RW
29	PPL5_HW_MODE.	The 6th pipeline handwriting mode.	RW
28	PPL4_HW_MODE.	The 5th pipeline handwriting mode.	RW
27	PPL3_HW_MODE.	The 4th pipeline handwriting mode.	RW
26	PPL2_HW_MODE.	The 3rd pipeline handwriting mode.	RW
25	PPL1_HW_MODE.	The 2nd pipeline handwriting mode.	RW

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24	PPL0_HW_MODE.	The 1st pipeline handwriting mode.	RW
23:9	PPL_HW_COLOR.	In color mode: PPL_HW_COLOR = { R[4:0], G[4:0], B[4:0] } In grayscale mode: PPL_HW_COLOR = { [4:0] } When a pipeline in handwriting mode, any pixels in its zone and match PPL_HW_COLOR will be updated using HW waveform.	RW
8:0	PAL_ADDR_OFF.	The address offset for dynamic changing palette.	RW

21.5.26 EPDC Pipeline 0 ~7 Position Registers

EPDC_PPL0_POS, EPDC_PPL1_POS, 0x13050280, 0x13050288
EPDC_PPL2_POS, EPDC_PPL3_POS 0x13050290, 0x13050298
EPDC_PPL4_POS, EPDC_PPL5_POS, 0x130502A0, 0x130502A8
EPDC_PPL6_POS, EPDC_PPL7_POS 0x130502B0, 0x130502B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PPL_YPOS												Reserved				PPL_XPOS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PPL_YPOS	The top-left Y position of rectangle zone for the specific pipeline.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PPL_XPOS	The top-left X position of rectangle zone for the specific pipeline.	RW

21.5.27 EPDC Pipeline 0~7 Size Registers

EPDC_PPL0_SIZE, EPDC_PPL1_ SIZE, 0x13050284, 0x1305028C
EPDC_PPL2_ SIZE, EPDC_PPL3_ SIZE 0x13050294, 0x1305029C
EPDC_PPL4_ SIZE, EPDC_PPL5_ SIZE, 0x130502A4, 0x130502AC
EPDC_PPL6_ SIZE, EPDC_PPL7_ SIZE 0x130502B4, 0x130502BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PPL_HEIGHT												Reserved				PPL_WIDTH											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	PPL_HEIGHT	The height of rectangle zone for the specific pipeline.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	PPL_WIDTH	The width of rectangle zone for the specific pipeline.	RW

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21.6 Application Guide

21.6.1 Pixel format in buffers

The format of texts and images stored in buffers is depending on how they're used. But it can be rearranged by setting PEDN and BEDN in LCDCTRL. Following tables illustrate the formats with different BPP.

Table 21-3 2 bits per pixel data buffer format

	pixel 7	**pixel 6**	**pixel 5**	**pixel 4**	**pixel 3**	**pixel 2**	**pixel 1**	**pixel 0**
FG0/1	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
	pixel 15	**pixel 14**	**pixel 13**	**pixel 12**	**pixel 11**	**pixel 10**	**pixel 9**	**pixel 8**
FG0/1	31:30	29:28	27:26	25:24	23:22	21:20	19:18	17:16

Table 21-4 4 bits per pixel data buffer format

	pixel 7	**pixel 6**	**pixel 5**	**pixel 4**	**pixel 3**	**pixel 2**	**pixel 1**	**pixel 0**
FG0	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
FG1	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0

Table 21-5 5 bits per pixel data buffer format

		pixel 3		**pixel 2**		**pixel 1**		**pixel 0**
FG0/1	31:29	28:24	**23:21**	20:16	15:13	12:8	7:5	4:0

21.6.2 Waveform LUT Format

There are 3x512 words RAM embedded in LCD used for waveform LUT. The number of LUT frames it can store depending on COLOR_MODE, OBPP, OSDOBPP and EPD_OBPP. A frame LUT needs $2^{(\text{Bits per pixel for text or image} * 2) + (\text{Bits per pixel for source driver})}$ bits RAM in mono mode. For example, when COLOR_MODE = 0, OBPP = OSDBPP = 2, and EPD_OBPP = 1, a frame LUT needs 2^9 = 512 bits RAM. In other words, the whole RAM can store up to 96 frames LUT in this case. For multi-zone concurrent updating and handwriting mode, the topmost frame LUT reserved for "Do Noting LUT", and the second topmost frame reserved for "Handwriting Mode LUT".

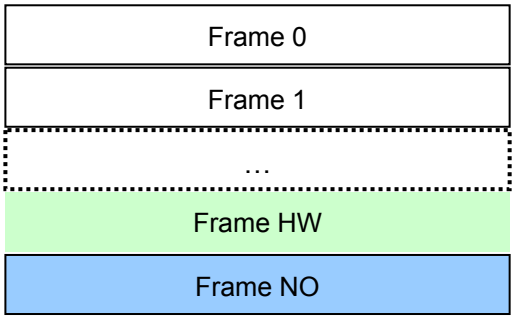


Figure 21-2 Mono mode frame LUT format

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The following tables illustrate frame LUT content. The Index is generated by,
Index = {Pixel in FG1, Pixel in FG0}.For instance, when pixel in FG0 equals to 0x0 and pixel in FG1 equals to 0xf, then the green highlighted one will be addressed. Specially, the “Frame HW” and “Frame NO” index are generated by pipeline’s current frame count.

Table 21-6 Frame N LUT format

WORD	31:30	29:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
15	255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240

Table 21-7 Frame HW/NO LUT format

WORD	31:30	29:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
0	Frame 15	…	…	…	…	…	…	…	…	…	…	…	…	…	…	Frame 0
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
15	Frame 255	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

21.6.3 Power On/Off Sequence

The controller has individual bits to enable and set all power management signals’ polarity. This is useful for using high and low active power switches. All delay times are in lines, calculated by, (Delay between PWRn to PWRm) = PWR_DLYnm * (HT * (SDCLK Clock Period)).
Those power management pins delays which are not used should be set to 0. Please refer to vendor’s EPD displays panel data sheet to find out the required power on/off sequence for VDNS, VDPS, VDPG, VDNG, and VCOM_L and VCOM_H when using AUO EPD. Confirm EPD controller enabled and EPDC_PMGR0~3 settings correct before you start power on/off sequence by setting the bit EPD_PWRON in EPDC_CTRL.

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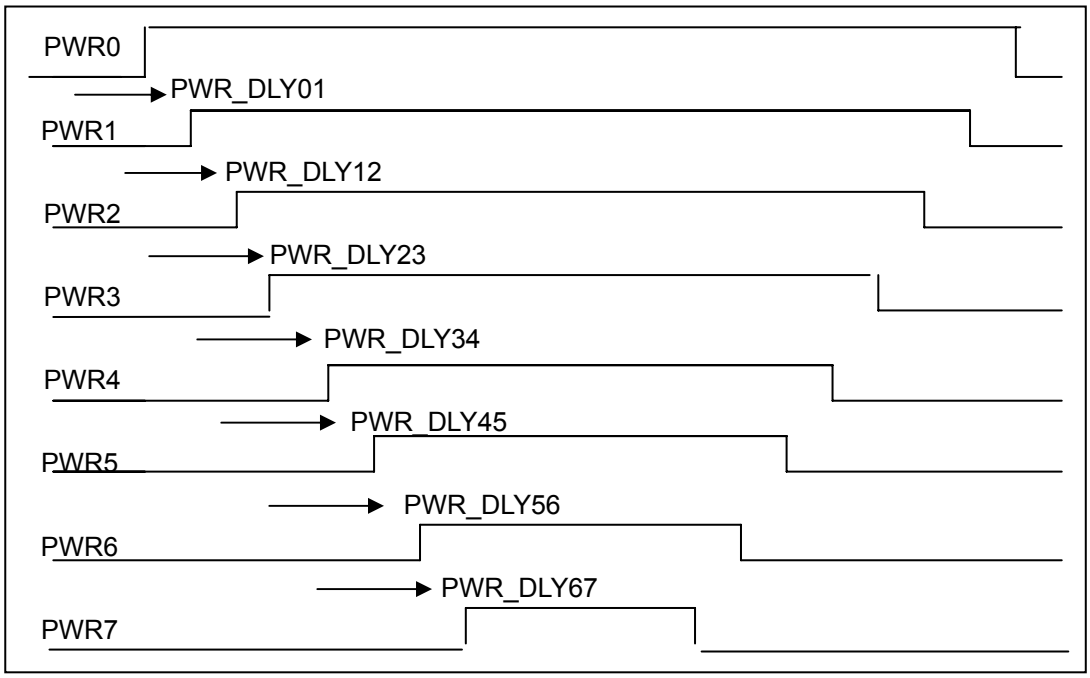


Figure 21-3 Powers On/Off Sequence

21.6.4 Display Timing Setting

The controller is designed as part of LCD controller. The frequency of pixel clock of the LCD is always double of the Source Driver clock. Typically, the frame frequency is 50 Hz in EPD display. Calculate timing parameters as followings,

Frame Rate = Line Number * Line Period, and Line number is set as VT.

Line Period = HT * (SDCLK Clock Period), SDCLK Clock Period = 2 * Pixel Clock Period.

So, first set pixel clock frequency according vendor's data sheet to get requirement SDCLK and frame rate. The following diagrams illustrate the Source and Gate Drivers' timing parameters for PVI and AUO EPD.

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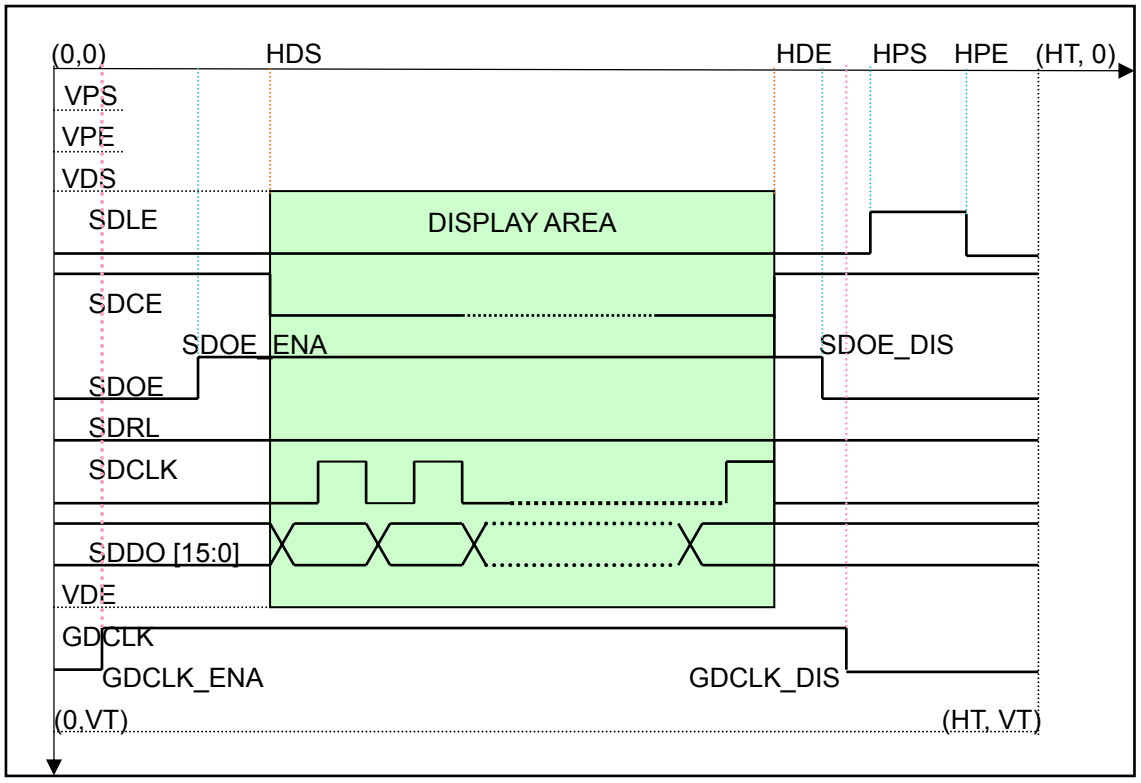


Figure 21-4 Source Drivers Reference Timing for PVI EPD

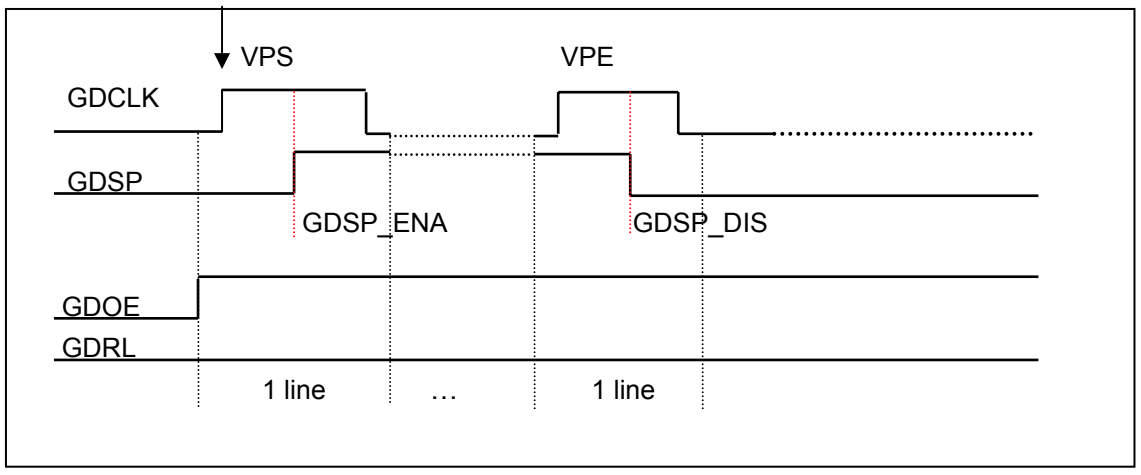


Figure 21-5 Gate Drivers Reference Timing for PVI EPD

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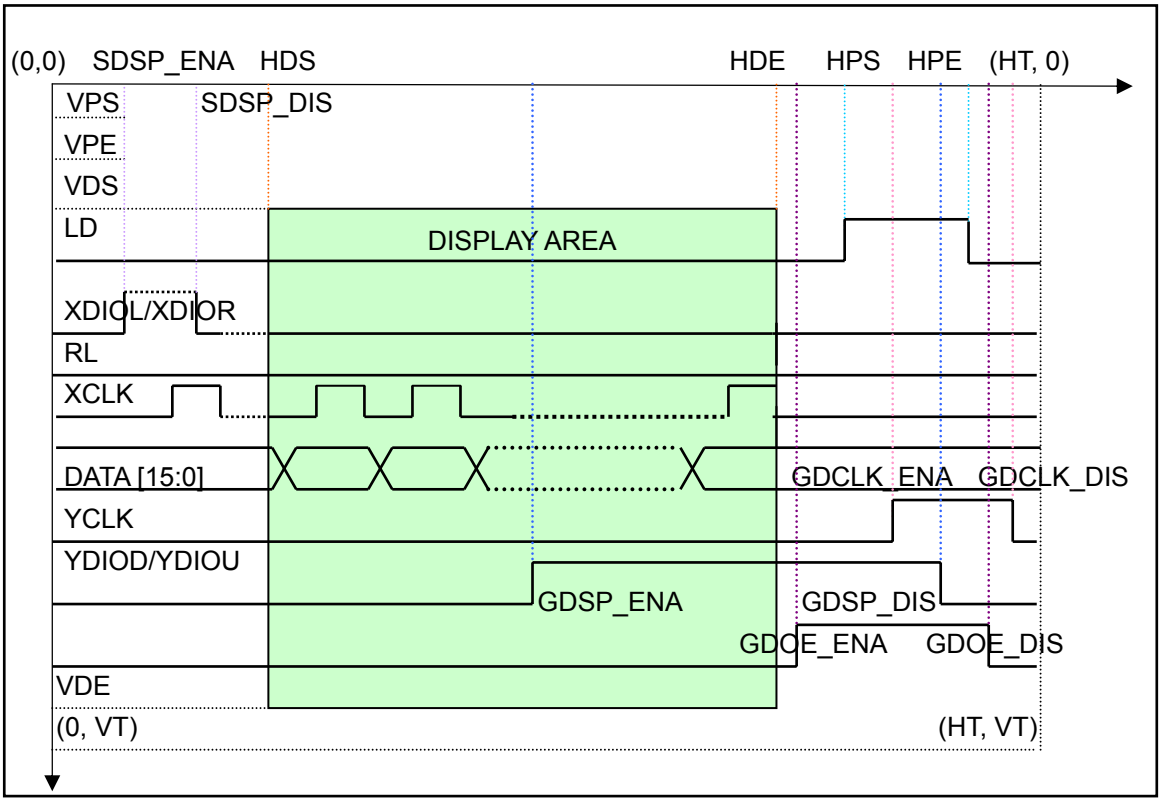


Figure 21-6 Source Drivers Reference Timing for AUO EPD

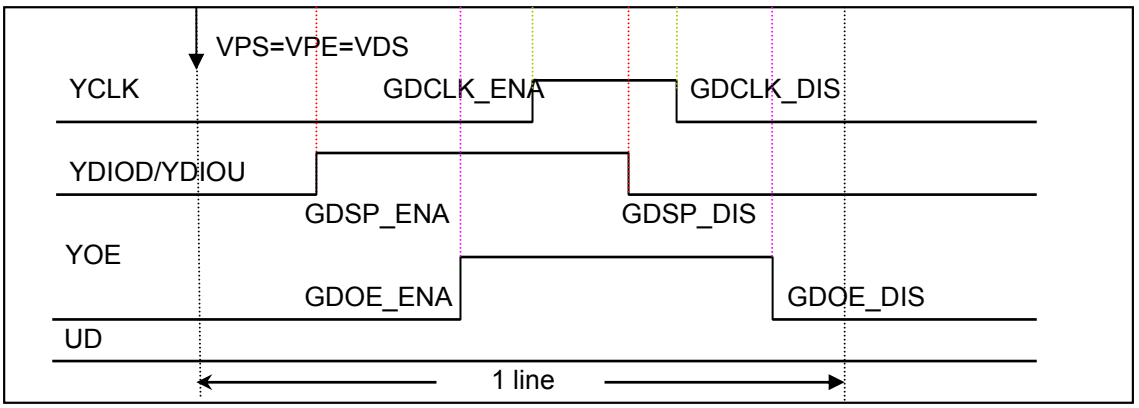


Figure 21-7 Gate Drivers Reference Timing for AUO EPD

21.6.5 Update image/text flow

1 Initialize LCD and EPD registers, such as display resolution, grayscale, and power on/off sequence requirements, source & gate driver's timings, according EPD data sheets.

2 Prepares LUT waveforms, display buffers and their descriptors relatively.

3 Set pipelines' sizes and frames if need multi-zone concurrent updating.

4 Starting EPD power on sequence, wait PWRON_INT assertion.

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5 Start LCD DMA to transfer LUT and buffers data to controller and set PPL_FRM_ENA and IMG_REF_ENA to update image on EPD display.
6 If necessary, start power off sequence to reduce power.

21.6.6 Multi-zone concurrent updating

Waveform LUT for “Do Nothing LUT” frame should be filled before using multi-zone updating. If Source Driver using PWRCOM, just fill 0 to all words of it. But if using VCOM, fill it with VCOM values for all frames. If a pipeline is available, it can be start at any time by setting its frame and size. A pipeline’s frame count will increments from 0 to its PPL_FRM_NUM after it started. That is independent from others pipelines. There pipelines zones should not overlap, if not, pipeline 0 has higher priority than pipeline 1, and so on.

21.6.7 Update VCOM0~5

VCOM0~5 should be updated when need more than 96 frame to display an image or text. If FRM_VCOM_INTE enabled, a FRM_VCOM_INT interrupt will be asserted when controller has outputted 95 frame data.

21.6.8 Handwriting mode

Multi-zone pipelines can be used for handwriting. There are individual bits to enable each pipeline’s handwriting mode. If a pipeline used for handwriting, any pixels in FG1 buffer lies in its zone and matches PPL_HW_COLOR will be updated using “HW Mode LUT” waveform. If not matches PPL_HW_COLOR, it will be updated using “Do Nothing LUT”, means no change will happen for that pixel. Before starting handwriting, SW fills the “Do Nothing LUT” and “HW Mode LUT” properly, which are indexed by pipeline’s frame count.

21.6.9 Border Display

Some EPD want to display border, if necessary, the 7th pipeline can be used to update border.
Border updating can be used with images or texts display. Properly set EPDC_BORDR, BDR_LEVEL and BDR_IDLE, then set PPL7_BDR_ENA, the 7th frame number and start it.

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22 Image Process Unit

22.1 Overview

IPU (Image process unit) contains Resize and CSC (color space conversion), which is used for image post processing.

22.1.1 Feature

- Location: AHB bus
- Input format
  - Separate frame: YUV /YCbCr (4:2:0, 4:2:2, 4:4:4, 4:1:1), RGB888
  - Packaged data: YUV422, RGB888, RGB565, RGB555, YUV444
  - Separate frame in block format: YUV/YCbCr 420
- Output data format
  - RGB (565, 555, 888, AAA)
  - Packaged data YUV422
- Color convention coefficient: configurable (CSC enable)
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 4095x4095
- Maximum output image size (pixel)
  - Width: up to 4095 (without vertical resizing)
    up to **2048** (with vertical resizing)
  - Height: up to 4095
- Image resizing
  - Support bilinear
  - 0 and bi-cube zooming mode
  - Up scaling ratios up to 1:31 in fractional steps with 1/32 accuracy
  - Down scaling ratios up to 31:1 in fractional steps with 1/32 accuracy

**For more details, refer to Special Instruction.*

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22.2 Block

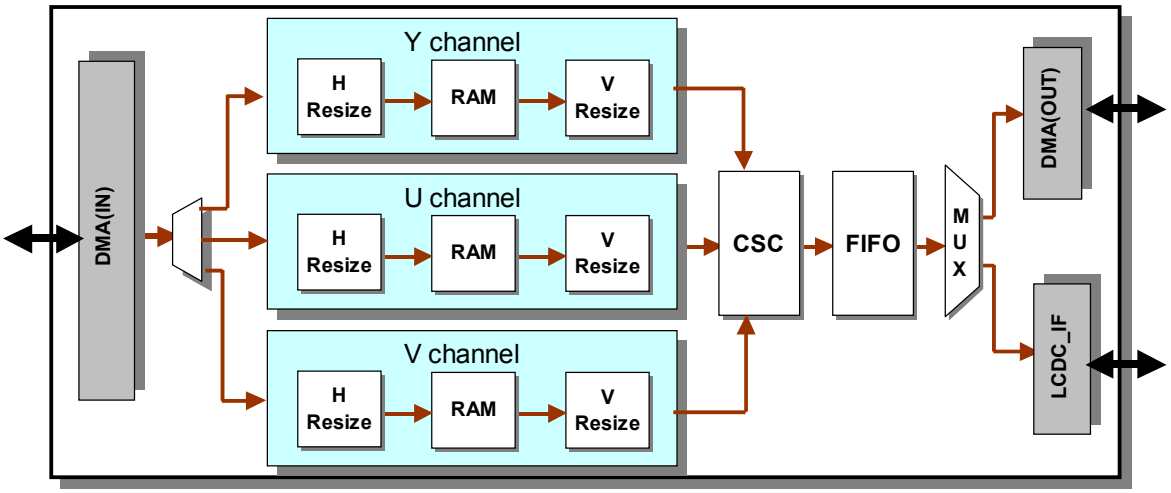


Figure 22-1 The Block about the IPUData flow

22.3 Data flow

22.3.1 Input data

- Separated YUV (or YcbCr/RGB888; the following use YUV for convenience) Frame case: Y, U, V data would be fetched from external memory by DMA burst read operation.
- Packaged YUV422 (or RGB888/ RGB565/ RGB555/YUV444) case: Packaged YUV(RGB888/ RGB565/ RGB555/YUV444) data would be fetched from external memory by DMA burst read operation.

22.3.2 Output data

- DMA output to external memory case: The output data format could be RGB (565, 555, 888) or YUV (package422), and the data would be stored to the external memory by DMA burst write operation.
- Flow into LCDC case: The output data format can be RGB or YUV (package), and the transfer would not cross AHB BUS.

22.3.3 Resize Coefficients LUT

The resize coefficients look up table is preset by software according to specific format (see for 22.4.30, 22.4.31 detail). There are 2 tables to support independent horizontal and vertical scaling. Each table has 32 entries that can accommodate up to 32 coefficient-groups.

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22.4 Registers Descriptions

The physical address base for the address-mapped registers of IPU is **0x13080000.**
The following table will show all the register address.

Table 22-1 register list

NAME	Offset	Descript
IPU_CONTROL	0x0	IPU global controller
IPU_STATUS	0x4	IPU global status register
D_FMT	0x8	IPU data format register
Y_ADDR	0xC	Source Y (or R) base address
U_ADDR	0x10	Source U (or G) base address
V_ADDR	0x14	Source V (or B) base address
IN_FM_GS	0x18	Input Geometric Size (height and width)
Y_STRIDE	0x1C	Source Y frame stride
UV_STRIDE	0x20	Source U and V frame stride
OUT_ADDR	0x24	Result frame base address
OUT_GS	0x28	Result frame size (height and width)
OUT_STRIDE	0x2C	Result frame stride
RSZ_COEF_INDEX	0x30	Resize Coefficients Table Index
CSC_C0_COEF	0x34	Color conversion Coefficient
CSC_C1_COEF	0x38	Color conversion Coefficient
CSC_C2_COEF	0x3C	Color conversion Coefficient
CSC_C3_COEF	0x40	Color conversion Coefficient
CSC_C4_COEF	0x44	Color conversion Coefficient
HRSZ_COEF_LUT	0x48	Horizontal Resize Coefficients Look Up Table
VRSZ_COEF_LUT	0x4C	Vertical Resize Coefficients Look Up Table
CSC_OFSET_PARA	0x50	Color conversion offset Coefficient
SRC_TLB_ADDR	0x54	Base address of the source Y's physical address map table
DEST_TLB_ADDR	0x58	Base address of the destination's physical address map table
TLB_MONITOR	0x60	TLB monitor
IPU_ADDR_CTRL	0x64	IPU address set controller
Y_ADDR_N	0x84	Source Y base address of next frame
U_ADDR_N	0x88	Source U base address of next frame
V_ADDR_N	0x8C	Source V base address of next frame
OUT_ADDR_N	0x90	Result frame base address of next frame
SRC_TLB_ADDR_N	0x94	Base address of the source Y's physical address map table for next frame
DEST_TLB_ADDR_N	0x98	Base address of the destination's physical address map table for next frame
TLB_CTRL	0x68	TLB controller
PIC_ENC_TABLE	0x400 ~0X7FF	Picture enhance table stone.

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22.4.1 IPU Control Register

IPU_CONTROL **0x0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							DMA_OPT	PENC_OPT	Reserved	CONF_MODE	ADDR_SEL	Reserved	ZOOM_SEL	DFIX_SEL	FIELD_SEL	FIELD_CONF	DISP_SEL	DPAGE_MAP	SPAGE_MAP	LCDC_SEL	SPKG_SEL	Reserved		IPU_STOP*4	IPU_RST	FM_IRQ_EN	CSC_EN	VRSZ_EN	HRSZ_EN	IPU_RUN	CHIP_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect, read as zero.	R
24	DMA_OPT	DMA strategy evaluation: 0: disable 1: enable DMA strategy auto adjust	RW
23	PENC_OPT	Picture enhance selector: 0: no picture enhance 1: picture enhance(for YUV format)	RW
22	Reserved	Writing has no effect, read as zero.	R
21	CONF_MODE	IPU configure mode selector. 0: IPU's registers can be changed any time 1: IPU's registers only can be changed when it is not busy	RW
20	ADDR_SEL*3	IPU address mode selector. 0: IPU source and destination address only can be modified when IPU is free, just like it is in XBurst JZ4750 processor 1: IPU source and destination address can be modified anytime	RW
19	Reserved	Writing has no effect, read as zero.	R
18	ZOOM_SEL	IPU rooming mode selector. 1: bi-cube 0: bilinear	RW
17	DFIX_ SEL	Fixed destination address choose. (Valid when LCDC_SEL == 0) 0: not use the fixed address 1: use the fixed address	RW
16	FIELD_SEL *1	Destination field choose. (Valid when FIELD_CONF_EN == 1) 0: top field 1: bottom field	RW

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15	FIELD_CONF_EN *1	FIELD_SEL mask. 0: do not change FIELD_SEL 1: configure FIELD_SEL Read as zero.	W
14	DISP_ SEL	Destination display choose. 0: frame display mode 1: field display mode	RW
13	DPAGE_MAP	Destination address page mapping choose. 0: not use the page mapping 1: use the page mapping	RW
12	SPAGE_MAP	Source address page mapping choose. 0: not use the page mapping 1: use the page mapping	RW
11	LCDC_SEL	Output data destination choose. 0: output to external memory 1: output to LCDC FIFO	RW
10	SPKG_SEL	Input data case choose. 0: Separated Frame 1: Packaged Frame	RW
9:8	Reserved	Writing has no effect, read as zero.	R
7	IPU_STOP*4	Stop IPU. 1: stop IPU. When stop IPU, the end flag will be pull up to 1.	W
6	IPU_RST *2	Reset IPU. Writing 1: reset IPU; 0: no effect. Read as zero.	W
5	FM_IRQ_EN	Frame process finish interrupt enable. 1: enable; 0: disable.	RW
4	CSC_EN	CSC enable. 1: enable; 0: disable.	RW
3	VRSZ_EN	Vertical Resize enable. 1: enable; 0: disable.	RW
2	HRSZ_EN	Horizontal Resize enable. 1: enable; 0: disable.	RW
1	IPU_RUN	Run the IPU. 1: run. Software just can set 1 to IPU_RUN.	RW
0	CHIP_EN	IPU chip enable. 1: enable; 0: disable.	RW

NOTES:

1 *[1]: The FIELD_SEL will work when the DISP_ SEL is 1, which indicates the IPU is under the field display mode. And the IPU will output the picture from the initial field (top or bottom) to the next field (bottom or top) automatically when the current field has been outputted or stopped. The initial field can be configured by setting the FIELD_SEL to 0 or 1 with FIELD_CONF_EN is 1. The FIELD_CONF_EN is just the trigger that controls the FIELD_SEL‘s valuation.

2 *[2]: Setting 1 to IPU_RST can reset all registers except the CHIP_EN immediately, but user must make sure the IPU is free when need to assert IPU_RST.

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3 *[3]: When ADDR_SEL is set to 0, the address set method is the same as XBurst JZ4750 processor, and the frame address of IPU can be set just like the way in XBurst JZ4750 processor, which limits the address setting time to IPU none working period (after frame end-flag). When the ADD_SEL is 1, the above limitation is released. The addresses of IPU can be changed at anytime. It just needs to set the correspond bits in IPU_ADDR_CTRL to 1 to tell IPU that new address can be used, after the addresses are changed.

4 *[4]: The IPU_STOP is used to stop IPU in anytime in save mode. When the IPU_STOP has been written to 1, the IPU need some time to stop. And the user can monitor the IPU_STATUS.OUT_END to make sure the IPU has been stopped.

22.4.2 IPU Status Register

IPU_STATUS **0x4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										MSTATUS		Reserved	SIZE_ERR	FMT_ERR	OUT_END
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect, read as zero.	R
5:4	MSTATUS	IPU main status. 00: IPU is free and waiting the CPU or LCDC to get the IPU's control 01: IPU is running now 10: IPU is under the control of CPU 11: reserved	R
3	Reserved	Writing has no effect, read as zero.	R
2	SIZE_ERR	The size error flag. 1: size error; 0: size ok.	R
1	FMT_ERR	IPU format error flag. 1: format error; 0: format OK.	R
0	OUT_END *1	Output termination flag. 1: finished; 0: not finished.	R/W

NOTE:

*1: If **IPU_CONTROL**.FM_IRQ_EN has been set 1, once OUT_END is set value 1 which denotes a frame's post process done, an low level active interrupt request will be issued until corresponding software handler read IPU_STATUS and clean end flag.

When the **IPU_CONTROL**.FM_LCDC_SEL has been set 1, and the IPU has finished one transfer, the LCDC and CPU need to occupy the IPU control. The IPU will monitor the request signal from LCDC and the read signal from the CPU, then it will determine whether dre-configure itself by the CPU if the CPU read first or output the same frame to LCDC again if the LCDC get the control.

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22.4.3 IPU address control register

IPU_ADDR_CTRL **0x64**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										PTD_RY	PTS_RY	D_RY	V_RY	U_RY	Y_RY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect, read as zero.	R
5	PTD_READY	New destination TLB base address ready. (Only used when IPU_CONTROL.ADDR_SEL==1&&IPU_CONTROL.DPAGE_MAP == 1)	RW
4	PTS_READY	New source TLB base address ready. (only used when IPU_CONTROL.ADDR_SEL==1&&IPU_CONTROL.SPAGE_MAP == 1)	RW
3	D_READY	New destination address ready.	RW
2	V_READY	New source V address ready.	RW
1	U_READY	New source U address ready.	RW
0	Y_READY	New source Y address ready.	RW

NOTES:

1 When the xx_READY bit has been set 1, the IPU will use the new corresponding address in the next frame, and use the old address value whose corresponding bit in **IPU_ADDR_CTRL** is 0.

2 **IPU_ADDR_CTRL** works when **IPU_CONTROL. ADDR_SEL** is 1.

3 When the **IPU** has fetched the new address, it will clear the **IPU_ADDR_CTRL** to 0.

22.4.4 Data Format Register

D_FMT **0x8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						RGB_888	RGB_OUT_OFT			OUT_FMT			YUV_PKG_OUT_OFT			Reserved											BLK_SEL	IN_OFT		IN_FMT	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:26	Reserved	Writing has no effect, read as zero.	R
25	RGB_888_	RGB888 output format indicator. (only used in RGB888 out	RW

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	OUT_FMT	OUT_FMT == 010) 0: the low 24 bits will be the pixel in a word 1: the high 24 bits will be the pixel in a word	
24:22	RGB_OUT_OFT	Output data packaged offset. (only used in RGB out OUT_FMT != 011) 000: RGB 001: RBG 010: GBR 011: GRB 100: BRG 101: BGR Others: reserved	RW
21:19	OUT_FMT	Indicates the destination data format. 000: RGB555 001: RGB565 010: RGB888 011: YUV422 package 100: RGBAAA(R(or G or B) is 10 bits wide)	RW
18:16	YUV_PKG_OUT_OFT	Output data packaged offset. (only used in CSC disable case and in the source is YUV422 packaged case (**IPU_CONTROL.** SPKG_SEL == 1)) 000: Y1UY0V 001: Y1VY0U 010: UY1VY0 011: VY1UY0 100: Y0UY1V 101: Y0VY1U 110: UY0VY1 111: VY0UY1	RW
15: 6	Reserved	Writing has no effect, read as zero.	R
4	BLK_SEL	Indicate the source data format when source is YUV420	RW
3:2	IN_OFT	Input data packaged offset. (when the source is YUV422 packaged case (**IPU_CONTROL.** SPKG_SEL == 1 && IN_FMT == 01)) 00: Y1UY0V 01: Y1VY0U 10: UY1VY0 11: VY1UY0	RW
1:0	IN_FMT	Indicates the source data format. When **IPU_CONTROL.**SPKG_SEL == 0 00: YUV 4:2:0 01: YUV 4:2:2 10: YUV 4:4:4 11: YUV 4:1:1 When **IPU_CONTROL.**SPKG_SEL == 1 00: RGB555 01: YUV 4:2:2 10: RGB888 or YUV444 11: RGB565	RW

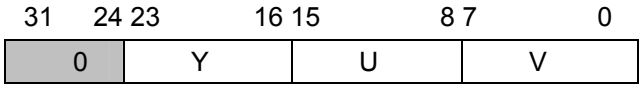
NOTES:

1 When the source frame is packed RGB, the **IPU_CONTROL.** SPKG_SEL must be 1 and IN_FMT must be 10, and when the source frame is packed YUV, the **IPU_CONTROL.**

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SPKG_SEL must be 1 and IN_FMT must be 01.

2 When the source frame is packed YUV444, the data format about a pixel should be as following:



22.4.5 Input Y Data Address Register

Y_ADDR **0xc**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Y_ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	Y_ADDR *1	In separated Frame case, it indicates the source Y (or R) data buffer's start address. In source YUV422 package case, it indicates the start Address of the packaged Frame.	RW

NOTES:

1 When the **IPU_CONTROL**.SPAGE_MAP == 1, the Y_ADDR should be the start virtual address.

2 Y_ADDR should be **word align**.

22.4.6 Input U Data Address Register

U_ADDR **0x10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U_ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	U_ADDR *1	The source U data buffer's start address of separated frame case.	RW

NOTES:

1 When the IPU_CONTROL.SPAGE_MAP == 1, the U_ADDR should be the start virtual

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address.

2 U_ADDR should be **word align**.

22.4.7 Input V Data Address Register

V_ADDR **0x14**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	V_ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	V_ADDR	The source V data buffer's start address of separated Frame case.	RW

NOTES:

1 When the IPU_CONTROL.SPAGE_MAP == 1, the V_ADDR should be the start virtual address.

2 V_ADDR should be word align.

22.4.8 Input source TLB base address

SRC_TLB_ADDR **0x54**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC_TLB_ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRC_TLB_ ADDR	The SOURCE TLB base address. (This register will act when the IPU_CONTROL.PAGE_MAP==1)	RW

22.4.9 Destination TLB base address

DEST_TLB_ADDR **0x58**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEST_TLB_ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	DEST_TLB_ ADDR	The destination frame's TLB base address. (This register will work when the IPU_CONTROL.DPAGE_MAP==1)	RW

22.4.10 TLB monitor

TLB_MONITOR **0x60**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					MIS_CNT										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:11	Reserved	Writing has no effect, read as zero.	R
10:0	MIS_CNT	The TLB cache miss counter.	RW

22.4.11 TLB controller

TLB_CTRL **0x68**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DEST_ BURST				DEST_PAGE				Reserved								SRC_ BURST				SRC_PAGE			
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect, read as zero.	R
23:20	DEST_BURST	The destination TLB burst length. 1: 1; 2:2; 4:4; 8:8.	RW
19:16	DEST_PAGE	The destination TLB page size. 1: 4K; 2: 8K; 4:16K; 8:32K.	RW
15:4	Reserved	Writing has no effect, read as zero.	R
7:4	SRC_BURST	The sources TLB burst length. 1: 1; 2:2; 4:4; 8:8.	RW
3:0	SRC_PAGE	The source TLB page size. 1: 4K; 2: 8K; 4:16K; 8:32K.	RW

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22.4.12 Input Y Data Address of next frame Register

Y_ADDR_N **0x84**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Y_ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	Y_ADDR_N	In separated Frame case, it indicates the source Y (or R) data buffer's start address of the next frame. In package case, it indicates the start address of the packaged Frame of the next frame.	R

22.4.13 Input U Data Address of next frame Register

U_ADDR_N **0x88**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U_ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	U_ADDR_N	The source U (G) data buffer's start address of the next frame in separated frame case.	RW

NOTE: When the IPU_CONTROL.SPAGE_MAP == 1, the U_ADDR_N will be the start virtual address.

22.4.14 Input V Data Address of next frame Register

V_ADDR_N **0x8C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	V_ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	V_ADDR_N	The source V (B) data buffer's start address of the next frame in separated frame case.	RW

NOTE: When the IPU_CONTROL.SPAGE_MAP == 1, the V_ADDR_N will be the start virtual address.

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22.4.15 Source TLB base address of next frame

SRC_TLB_ADDR_N **0x94**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC_TLB_ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRC_TLB_ADDR_N	The TLB base address about the next source frame's data which will be DMA in.	R

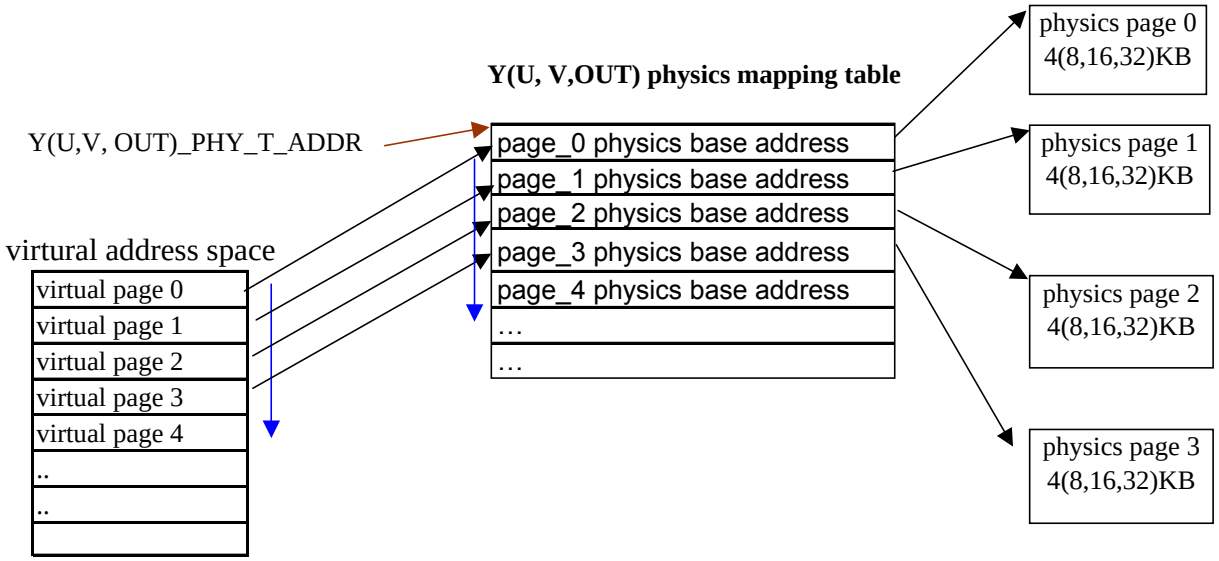
22.4.16 Destination TLB base address of next frame

DEST_TLB_ADDR_N **0x98**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEST_TLB_ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DEST_TLB_ADDR_N	The TLB base address about the next frame's data that will be DMA out.	R

22.4.17 ADDRESS Mapping



The Y (U, V, OUT)_PHY_T_ADDR should store the **base address** of the Y (U, V, OUT)

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physics-mapping table. In the Y (U, V, OUT) physics-mapping table, it should contain different physics page base address, and the physics page must be 4(8, 16, 32)KB align.

22.4.18 Input Geometric Size Register

IN_FM_GS **0x18**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				IN_FM_W												Reserved				IN_FM_H											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	IN_FM_W	The width of the input frame (unit: byte). Y data width is the same as this value while U/V or Cb/Cr data width should do relatively zoom in according to the source data format. And **in the source package pattern**, this value should be the Y data width also.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	IN_FM_H	The height of the input frame (unit: byte). Y data width is same as this value while U/V or Cb/Cr data width should do relatively zoom in according to the source data format.	RW

22.4.19 Input Y Data Line Stride Register

Y_STRIDE **0x1c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Y_S														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	Y_S	The line stride of the source Y data in the external memory of separated Frame case or packaged Frame stride(Unit: byte).	RW

NOTE: Y_S should be world align.

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22.4.20 Input UV Data Line Stride Register

UV_STRIDE **0x20**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			U_S											0	0	Reserved			V_S											0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29	Reserved	Writing has no effect, read as zero.	R
28:16	U_S	The line stride of the source U data in the external memory.	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	V_S	The line stride of the source V data in the external memory.	RW

NOTE: U_S and V_S should be word align and unit is byte.

22.4.21 Output Frame Start Address Register

OUT_ ADDR **0x24**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT_ ADDR																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	OUT_ ADDR *1	The output buffer's start address.	RW

NOTES:

1 *1: When the IPU_CONTROL.DPAGE_MAP == 1, the OUT_ADDR should be the start virtual address.

2 it should be word align.

22.4.22 Output Data Address of next frame Register

OUT_ ADDR_N **0x90**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT_ ADDR_N																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:0	OUT_ ADDR *1	The output buffer's start address.	RW

NOTES:

1 *1: When the IPU_CONTROL.DPAGE_MAP == 1, the OUT_ADDR should be the start virtual address.

2 it should be word align.

22.4.23 Output Geometric Size Register

OUT_GS **0x28**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OUT_FM_W														Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30:16	OUT_FM_W	The width of the output destination frame (unit: byte).	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	OUT_FM_H	The height of the output destination frame (unit: byte).	RW

NOTES:

1 In the package YUV out pattern, the OUT_FM_W should be the **pixel number** in a line.

2 In the **RGB** out pattern, the OUT_FM_W should be the **data space** width in the RAM.

3 In the out package pattern, the OUT_FM_W **must be** even number, and otherwise IPU will not run.

e.g.

Package YUV out: 480x273 (OUT_FM_W: 480 OUT_FM_H: 273)

RGB 888 (or AAA) out: 480x273 (OUT_FM_W: 480*4 OUT_FM_H: 273)

RGB 555 (or 565) out: 480x273 (OUT_FM_W: 480*2 OUT_FM_H: 273)

22.4.24 Output Data Line Stride Register

OUT_STRIDE **0x2c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														0	0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	OUT_S	The line stride of the destination data buffer in the external memory(Unit: byte).	RW

22.4.25 CSC C0 Coefficient Register

CSC_C0_COEF **0x34**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				C0_COEF												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	C0_COEF	The C0 coefficient of the YUV/YCbCr to RGB conversion. C0_COEF = [C0 * 1024 + 0.5].	RW
NOTE: R = C0*(Y –LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF) – C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

22.4.26 CSC C1 Coefficient Register

CSC_C1_COEF **0x38**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				C1_COEF												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	C1_COEF	The C1 coefficient of the YUV/YCbCr to RGB conversion. C1_COEF = [C1 * 1024 + 0.5].	RW
NOTE: R = C0*(Y – LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF) – C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

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22.4.27 CSC C2 Coefficient Register

CSC_C2_COEF 0x3C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				C2_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	C2_COEF	The C2 coefficient of the YUV/YCbCr to RGB conversion. C2_COEF = [C2 * 1024 + 0.5].	RW
NOTE: R = C0*(Y – LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF) – C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

22.4.28 CSC C3 Coefficient Register

CSC_C3_COEF 0x40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				C3_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	C3_COEF	The C3 coefficient of the YUV/YCbCr to RGB conversion. C3_COEF = [C3 * 1024 + 0.5].	RW
NOTE: R = C0*(Y – LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF) – C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

22.4.29 CSC C4 Coefficient Register

CSC_C4_COEF 0x44

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				C4_COEF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	C4_COEF	The C4 coefficient of the YUV/YCbCr to RGB conversion. C4_COEF = [C4 * 1024 + 0.5].	RW
NOTE: R = C0*(Y – LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF) – C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

22.4.30 Resize Coefficients Table Index Register

RSZ_COEF_INDEX **0x30**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												HE_IDX				Reserved											VE_IDX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:21	Reserved	Writing has no effect, read as zero.	R
20:16	HE_IDX *1	Indicates the end address of the horizontal resize look up table.	RW
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	VE_IDX *1	Indicates the end address of the vertical resize look up table.	RW

NOTE: The HE_IDX (VE_IDX) should be the depth of the horizontal (vertical) resize look up table **minus 1**, and how to get HE_IDX or VE_IDX, please refer to 3.34.

22.4.31 Horizontal Resize Coefficients Look Up Table Register group

HRSZ_COEF_LUT (bi-cube) **0x48**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SIGN	W_COEF_31										SIGN	W_COEF_20									HRSZ_OFT					H_CONF	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserve	Writing has no effect, read as zero.	W
27:17	W_COEF_31	Weighting coefficients for pix_3 or pix_1.	W
16:6	W_COEF_20	Weighting coefficients for pix_2 or pix_0.	W

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5:1	HRSZ_OFT	Horizontal Resize pixel offset.	W
0	H_CONF	Start to configure the horizontal resize table, read as zero: 1: start.	W

HRSZ_COEF_LUT (bilinear) **0x48**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SIGN	W_COEF0									H_OFT					H_CONF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:10	Reserve	Writing has no effect, read as zero.	R
16:6	W_COEF0	Weighting coefficients for pix_0.	W
5:1	H_OFT	Horizontal Resize pixel offset.	W
0	H_CONF	Start to configure the horizontal resize table, read as zero: 1: start.	W

NOTES:

1 The **bilinear zooming** weighting coefficients should be calculated as following: because it is 11 bits length, a one bit is the sign-bit, so, that is to say the precision is 1/512.

For up-scaling,

$W_k = 1 – (k*n/m – [k*n/m]), k = 0, 1, … m-1.$

For down-scaling,

```
for (t=0, k=0; k < n; k++)
{
   If ([(t*n+1)/m] – k >=1) { W_k = 0;}
   else if ((t*n+1)/m – k == 0) { W_k = 1; t++;}
   else { W_k = 1 – ( (t*n+1)/m – [t*n/m]); t++;}
}
```

$W\_COEF_k = [512 * W_k]$ (stands for get the rounding integer, [20.33] = 20 while [20.66] = 21)

Here n stands for original pixel points, m stands for pixel points after resize. For example down-scaling 5:3, n = 5, m = 3. Moreover, m and n are prime, that is, for example 8:2 should be converted to 4:1.

When IPU_CONTROL.RSZ_EN set as 1 and m:n = 1:1, all coefficients should be calculated as up-scale case.

2 The **bi-cube zooming** weighting coefficients should be calculate as following: because it is 10 bits length, that is to say the precision is 1/512.

Step1:

For up-scaling,

$W_k = 1 – (k*n/m – [k*n/m]), k = 0, 1, … m-1.$

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For down-scaling,

```
for (t=0, k=0; k < n; k++)
{
    If ([(t*n+1)/m] – k >=1) { W_k = 0;}
    else if ((t*n+1)/m – k == 0) { W_k = 1; t++;}
    else { W_k = 1 – ( (t*n+1)/m – [t*n/m]); t++;}
}
```

W_COEF_k = [512 * W_k] (stands for get the rounding integer, [20.33] = 20 while [20.66] = 21)

Here n stands for original pixel points, m stands for pixel points after resize. For example down-scaling 5:3, n = 5, m = 3. Moreover, m and n are prime, that is, for example 8:2 should be converted to 4:1.

When IPU_CONTROL.RSZ_EN set as 1 and m:n = 1:1, all coefficients should be calculated as up-scale case.

Step 2:

After calculate the Wk, then using the following rule to get the coefficients:

```
double SinXDivX(double x)
{
    const float a = -1; //a can be a=-2,-1,-0.75,-0.5 and so on to control the blur level
    double x2=x*x;
    double x3=x2*x;
    if (x<=1)
    return (a+2)*x3 - (a+3)*x2 + 1;
    else if (x<=2)
    return a*x3 - (5*a)*x2 + (8*a)*x - (4*a);
    else
    return 0;
}
```

W0 = 512*SinXDivX(1+Wk) W1 = 512*SinXDivX(Wk)

W2 = 512*SinXDivX(1-Wk) W3 = 512*SinXDivX(2-Wk)

Step 3:

And then the zooming weight coefficient should set to IPU as following:

Prepare: Set H_CONF to 1

a set W4n+1 & W4n+0

b set W4n+3 & W4n+2

Index(n)	step	W0	W1	step	W2	W3
0	0	-34	129	1	100	-19
1	2	-45	45	3	77	-33
2	4	-12	122	5	94	-56
3	6	-13	230	7	123	-77
4	8	-23	11	9	45	-100
5	10	-19	87	11	69	-90

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6	12	-12	79	13	148	-8

3 Calculate the H_OFT.

Step 1: calculate the line in enable flag (IN_EN) and out enable flag (OUT_EN) table.

IN_EN: In down scale case, IN_EN always equals 1.
In up scale case,
For (i=0, k=0; k < m; k++) {
If(i<= k*n/m) { IN_EN [k] = 1; i++;}
else { IN_EN [k] =0;}

OUT_EN: In up scale case, OUT_EN always equals 1.
In down scale case,
For (t=0, k=0; k < n; k++) {
If([(t*n+1)/m] – k >=1)
OUT_EN [k] = 0;
else {OUT_EN[k]=1; t++;}
}

Step 2: calculate the H_MAX_LUT.

H_MAX_LUT = max (m, n) – 1

*Step 3: C*alculate the LUT.

```
int hoft_table_buf[33];
int hcoef_table_buf[33];
int voft_table_buf[33];
int vcoef_table_buf[33];
int *hoft_table = &hoft_table_buf[1];
int *hcoef_table = &hcoef_table_buf[1];
int *voft_table = &voft_table_buf[1];
int *vcoef_table = &vcoef_table_buf[1];
int in_oft_tmp = 0;
int hcoef_real_heiht = 0   ;
int vcoef_real_heiht = 0   ;
int coef_tmp = 0   ;
j = -1 ;
 for (i=0; i<=H_MAX_LUT+1; i++)
 {
     if ( h_lut[i].out_n )
     {
          hoft_table[j] = (h_lut[i].in_n == 0)? 0: in_oft_tmp;
          hcoef_table[j] = coef_tmp;
          coef_tmp = h_lut[i].coef;
          in_oft_tmp = h_lut[i].in_n==0? in_oft_tmp : h_lut[i].in_n ;
          j++;
      }
      else
```


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```
            in_oft_tmp = h_lut[i].in_n + in_oft_tmp;
        }
    if ( h_lut[0].out_n )
    {
        hoft_table[j] = (h_lut[0].in_n == 0)? 0: in_oft_tmp;        \
        hcoef_table[j] = coef_tmp;
    }
    j++;
    hcoef_real_heiht = j;
     RSZ_COEF_INDEX. HE_IDX = j –1;
```

Step 4: Calculate the last table of resize coefficient.

Bilinear:

```
for (cnt =0 ; cnt<hcoef_real_heiht ; cnt ++)
        HRSZ_COEF_LUT_bilinear[cnt] = (hcoef_table[cnt], hoft_table[cnt]);
```

Bicube:

```
 int sinxdivx_table_8[(2<<9)+1];
for ( i = 0 ; i < (2<<9); ++i)
 {
     sinxdivx_table_8[i] = (int)(0.5 + 512*sinxdivx(i*(1.0/512)));
 }
int u_8;
for (i = 0 ; i <hcoef_real_heiht; i++ )
{
        int au_8[4];
        u_8 = 512 - hcoef_table[i];
        cube_hcoef_table[i][0] = sinxdivx_table_8[(1<<9)+u_8];
        cube_hcoef_table[i][1] = sinxdivx_table_8[u_8];
        cube_hcoef_table[i][2] = sinxdivx_table_8[(1<<9)-u_8];
        cube_hcoef_table[i][3] = sinxdivx_table_8[(2<<9)-u_8];
   }
for (cnt =0 ; cnt<hcoef_real_heiht ; cnt ++)
        HRSZ_COEF_LUT_bicube[cnt] = (cube_hcoef_table[cnt], hoft_table[cnt]);
```

4 Following are two examples of setting LUT in bilinear scale mode.

Resize coefficients for 7:3:

W	W_COEF	IN_EN	OUT_EN	Pixel 1	Pixel 2	OUT
2/3	341	1	1	P [0]	P [1]	P [0] * 2/3 + P [1] * 1/3
0	0	1	0	P [1]	P [2]	No new pixel out
1/3	171	1	1	P [2]	P [3]	P [2] * 1/3 + P [3] * 2/3
0	0	1	0	P [3]	P [4]	No new pixel out
0	0	1	0	P [4]	P [5]	No new pixel out
1	512	1	1	P [5]	P [6]	P [5] * 1 + P [6] * 0

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0	0	1	0	P [6]	P [7]	No new pixel out

Parameter set to IPU is following:

index	W	W_COEF	OFSET	Pixel1	Pixel 2	OUT
0	2/3	341	2	P [0]	P [1]	P [0] * 2/3 + P [1] * 1/3
1	1/3	171	3	P [2]	P [3]	P [2] * 1/3 + P [3] * 2/3
2	1	512	2	P [5]	P [6]	P [5] * 1 + P [6] * 0

Resize coefficients for 3:5:

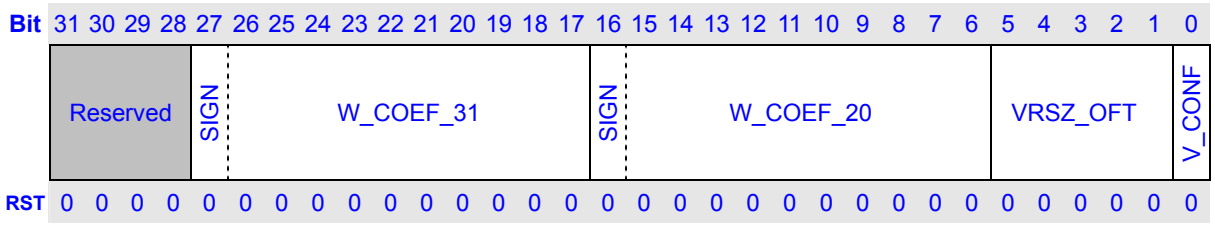
W	W_COEF	IN_EN	OUT_EN	Pixel 1	Pixel 2	OUT
1	512	1	1	P [0]	P [1]	P [0] * 1 + P [1] * 0
2/5	205	0	1	P [0]	P [1]	P [0] * 2/5 + P [1] * 3/5
4/5	410	1	1	P [1]	P [2]	P [1] * 4/5 + P [2] * 1/5
1/5	102	0	1	P [1]	P [2]	P [1] * 1/5 + P [2] * 4/5
3/5	307	1	1	P [2]	P [3]	P [2] * 3/5 + P [3] * 2/5

The parameter set to IPU is as following:

index	W	W_COEF	OFSET	Pixel 1	Pixel 2	OUT
0	1	512	0	P [0]	P [1]	P [0] * 1 + P [1] * 0
1	2/5	205	1	P [0]	P [1]	P [0] * 2/5 + P [1] * 3/5
2	4/5	410	0	P [1]	P [2]	P [1] * 4/5 + P [2] * 1/5
3	1/5	102	1	P [1]	P [2]	P [1] * 1/5 + P [2] * 4/5
4	3/5	307	1	P [2]	P [3]	P [2] * 3/5 + P [3] * 2/5

22.4.32 Vertical Resize Coefficients Look Up Table Register group

VRSZ_COEF_LUT (bi-cube) **0x4C**

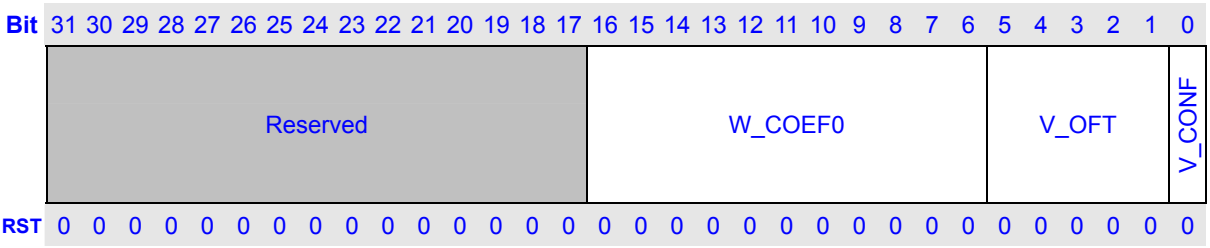


Bits	Name	Description	R/W
31:28	Reserved	Writing has no effect, read as zero.	W
27:17	W_COEF_31	Weighting coefficients for pix_3 or pix_1.	W
16:6	W_COEF_20	Weighting coefficients for pix_2 or pix_0.	W
5:1	VRSZ_OFT	Vertical Resize pixel offset.	W

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0	V_CONF	Start to configure the vertical resize table, read as zero: 1: start.	W

VRSZ_COEF_LUT (bilinear) **0x4C**



Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16:6	W_COEF0	Weighting coefficients for pix_0.	W
5:1	V_OFT	Vertical Resize pixel offset.	W
0	V_CONF	Start to configure the vertical resize table, read as zero: 1: start.	W

NOTE: refer to Horizontal HRSZ_COEF_LUT.

22.4.33 Calculation for Resized width and height

For software, to preset correct value for register OUT_GS, please refer to following formula.
Set IW stand for original input frame width, IH stand for original input frame height, OW stand for new frame width after resize, OH stand for new frame height after resize.

In Up-scale case (n < m):

If [(IW - 1) * (m/n)] * (n/m) ==(IW-1) then
    OW = [(IW - 1) * (m/n)] + 1;
Else OW = [(IW - 1) * (m/n)] + 2;
If [(IH - 1) * (m/n)] * (n/m) == (IH-1) then
    OH = [(IH - 1) * (m/n)] + 1;
Else OH = [(IH - 1) * (m/n)] + 2;

In Down-scale case (n>m):

If [(IW - 1) * (m/n)] * (n/m) ==(IW-1) then
    OW = [(IW - 1) * (m/n)];
Else OW = [(IW - 1) * (m/n)] + 1;
If [(IH - 1) * (m/n)] * (n/m) ==(IH-1) then
    OH = [(IH - 1) * (m/n)];
Else OH = [(IH - 1) * (m/n)] + 1;

For example:

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A 36x46 frame with the horizontal resize ratio of 4:5 (up-scale) and vertical resize ratio of 7:6 (down-scale), by the expressions above we get its new size after resize from the following process.

For Width: [(36 - 1) * (5/4)] * (4/5) = 34.4 ≠ (36-1)

So OW = [(36 - 1) * (5/4)] + 2 = 45

For Height: [(46 - 1) * (6/7)] * (7/6) = 44.33 ≠ (46 - 1)

So OH = [(46 - 1) * (6/7)] + 1 = 39

22.4.34 CSC Offset Parameter Register

CSC_OFSET_PARA **0x50**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CHROM_OF								Reserved								LUMA_OF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	CHROM_OF	Chroma offset value.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	LUMA_OF	Luma offset value.	RW
NOTE: R = C0*(Y – LUMA_OF) + C1*(Cr-CHROM_OF) G = C0*(Y – LUMA_OF) – C2*(Cb-CHROM_OF)– C3*(Cr-CHROM_OF) B = C0*(Y – LUMA_OF) + C4*(Cb-CHROM_OF)			

22.4.35 Picture enhance table

PENC_TAB **0x7FF~0x400**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C4n+3								C4n+2								C4n+1								C4n							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

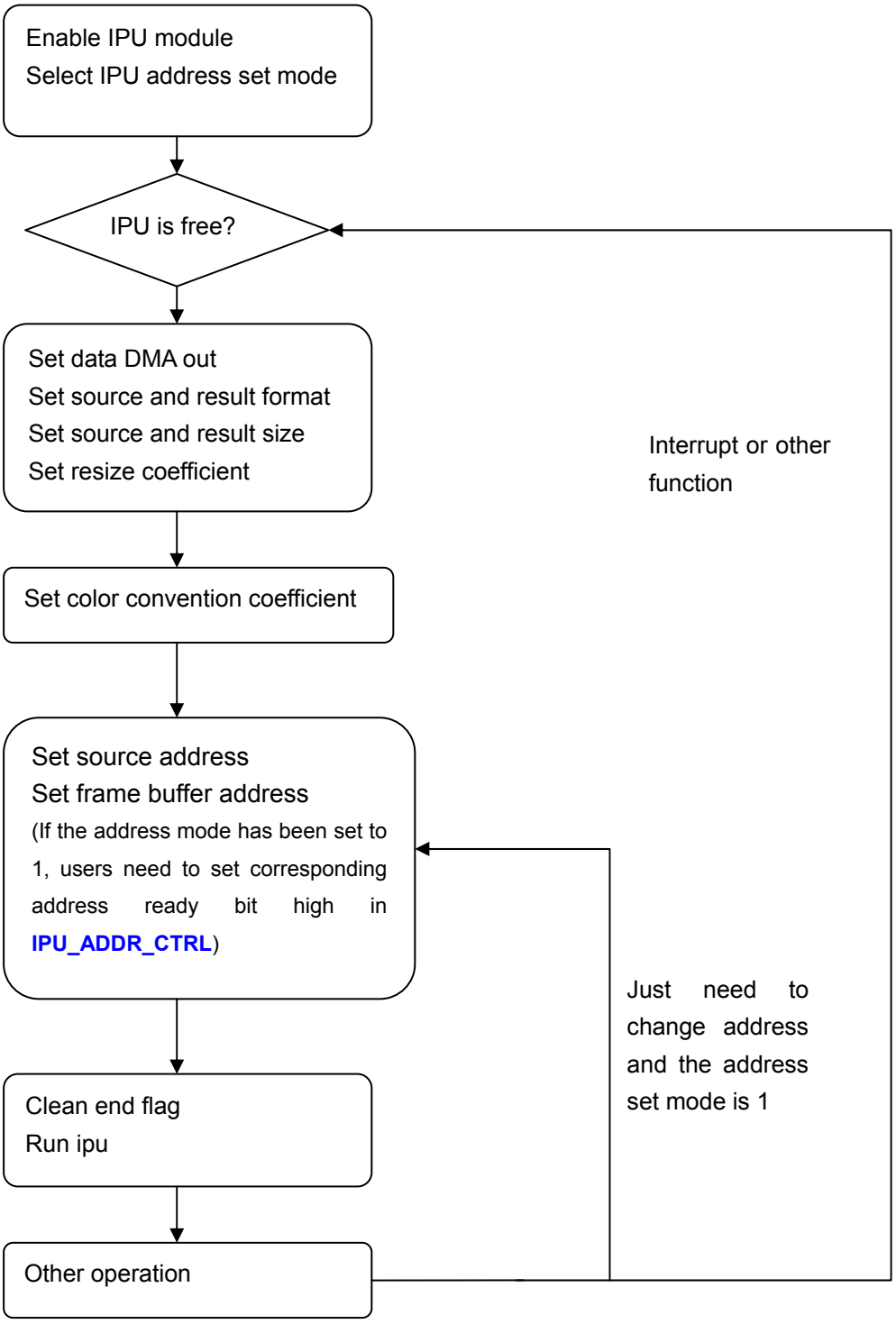
Bits	Name	Description	R/W
31:24	C4n+3	Color mapping result.	W
23:16	C4n+2	Color mapping result.	W
15:8	C4n+1	Color mapping result.	W
7:0	C4n	Color mapping result.	W

When the IPU_CONTROL.PENC_OPT == 1and the source picture is YUV, this table will act. This table will tell IPU how to mapping the resizing result to the final result. For an example, if the resizing result is 0x80, and the index 0x80 of this table is 0x70, so the final result will be 0x70.

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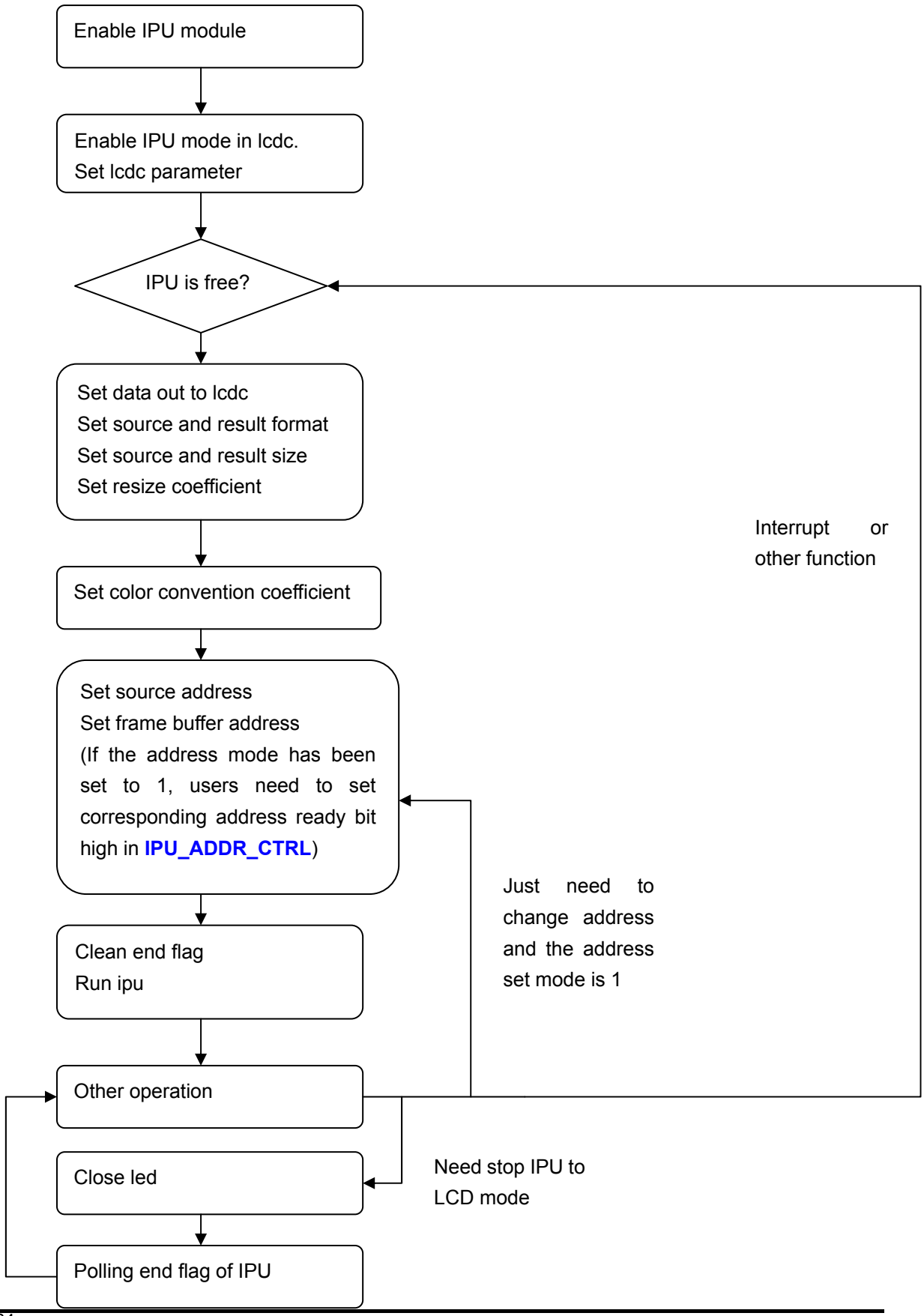
22.5 IPU Operation Flow

22.5.1 Data out to frame buffer



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22.5.2 Data out to lcdc



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22.5.3 Operation example

Table 22-2 no mapping mode

Step	Action
Base	Chip_enable()
Base_0	ipu_addr_sel(1);
0	Do { } while {!polling_end_flag}
1	set_primary_ctrl(VRSZ_ENABLE, HRSZ_ENABLE, CSC_EN, irq_en); //
2	set_source_ctrl(source_pkg_sel, SPAGE_SEL) ;
3	set_out_ctrl(lcdc_sel, DPAGE_SEL, DISP_SEL, FIELD_SEL, FIELD_CONF_EN) ;
4	set_scale_ctrl(V_SCALE, H_SCALE);
5	set_ipu_fmt(RGB888_OUT_FMT, OUT_OFT_RGB, OUT_FMT, OUT_Y1UY0V , IN_OF_YUYV, IN_FM_YUV444);
6	set_inframe_gsize(FIN_W, FIN_H, FIN_Y_STRIDE, FIN_U_STRIDE, FIN_V_STRIDE);

7	set_y_addr((unsigned int)fin_y & 0x1FFFFFFF);
	set_u_addr((unsigned int)fin_y & 0x1FFFFFFF);
	set_v_addr((unsigned int)fin_y & 0x1FFFFFFF);

8	set_outframe_gsize(FOUT_W, FOUT_H , FOUT_STRIDE);
9	set_out_addr((unsigned int)fout & 0x00000FFF);
9A	set_addr_ready(0xFF); **NOTE:** this step is necessary when ipu address set mode is 1.

10	set_csc_c0(YUV_CSC_C0);
	set_csc_c1(YUV_CSC_C1);
	set_csc_c2(YUV_CSC_C2);
	set_csc_c3(YUV_CSC_C3);
	set_csc_c4(YUV_CSC_C4);

11	set_csc_ofset_para (128, 0) ;
12	set_rsz_lut_end(H_MAX_LUT-1, V_MAX_LUT-1);
13	start_hlut_coef_write(); **NOTE:** This step is necessary before write new LUT.

14	for (i=0;i<H_MAX_LUT;i++) {
	set_hrsz_lut_coef(h_lut[i].coef, h_lut[i].in_n, h_lut[i].out_n);
	}

15	start_vlut_coef_write(); **NOTE:** This step is necessary before write new LUT.

16	for (i=0;i<V_MAX_LUT;i++) {
	set_vrsz_lut_coef(v_lut[i].coef, v_lut[i].in_n, v_lut[i].out_n);
	}

17	Clean_end_flag(); run_ipu();

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Table 22-3 mapping mode

Step	Action

Prepare	y_phy_table[0] = ((unsigned int)fin_y & 0x0FFFF000) | 0x20000000 ;
	u_phy_table[0] = ((unsigned int)fin_u & 0x0FFFF000) | 0x20000000 ;
	v_phy_table[0] = ((unsigned int)fin_v & 0x0FFFF000) | 0x20000000 ;
	out_phy_table[0] = ((unsigned int)fout & 0x0FFFF000) | 0x20000000 ;
	for (i =1; i<100; i++){
	y_phy_table[i] = y_phy_table[i-1] + 4096 ;
	u_phy_table[i] = u_phy_table[i-1] + 4096 ;
	v_phy_table[i] = v_phy_table[i-1] + 4096 ;
	out_phy_table[i] = out_phy_table[i-1] + 4096 ;
	}

Base	Chip_enable()
Base_0	ipu_addr_sel(1);
0	Do { } while {!polling_end_flag}
1	set_primary_ctrl(VRSZ_ENABLE, HRSZ_ENABLE, CSC_EN, irq_en); //
2	set_source_ctrl(source_pkg_sel, SPAGE_SEL) ;
3	set_out_ctrl(lcdc_sel, DPAGE_SEL, DISP_SEL, FIELD_SEL, FIELD_CONF_EN) ;
4	set_scale_ctrl(V_SCALE, H_SCALE);
5	set_ipu_fmt(RGB888_OUT_FMT, OUT_OFT_RGB, OUT_FMT, OUT_Y1UY0V , IN_OF_YUYV, IN_FM_YUV444);
6	set_inframe_gsize(FIN_W, FIN_H, FIN_Y_STRIDE, FIN_U_STRIDE, FIN_V_STRIDE);

7	set_y_addr((unsigned int)fin_y & 0xFFF);
	set_u_addr((unsigned int)fin_y & 0xFFF);
	set_v_addr((unsigned int)fin_y & 0xFFF);

8	set_outframe_gsize(FOUT_W, FOUT_H , FOUT_STRIDE);
9	set_out_addr((unsigned int)fout & 0x00000FFF);
10	set_y_phy_t_addr((unsigned int)y_phy_table & 0x1FFFFFFF) ; set_u_phy_t_addr((unsigned int)u_phy_table & 0x1FFFFFFF) ; set_v_phy_t_addr((unsigned int)v_phy_table & 0x1FFFFFFF) ; set_out_phy_t_addr((unsigned int)out_phy_table & 0x1FFFFFFF) ;
10A	set_addr_ready(0xFF); **NOTE:** this step is necessary when ipu address set mode is 1.

11	set_csc_c0(YUV_CSC_C0);
	set_csc_c1(YUV_CSC_C1);
	set_csc_c2(YUV_CSC_C2);
	set_csc_c3(YUV_CSC_C3);
	set_csc_c4(YUV_CSC_C4);

12	set_csc_ofset_para (128, 0) ;
13	set_rsz_lut_end(H_MAX_LUT-1, V_MAX_LUT-1);

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```
14      start_hlut_coef_write();
        NOTE: This step is necessary before write new LUT.
15        for (i=0;i<H_MAX_LUT;i++) {
            set_hrsz_lut_coef(h_lut[i].coef, h_lut[i].in_n, h_lut[i].out_n);
          }
16        start_vlut_coef_write();
        NOTE: This step is necessary before write new LUT.
17        for (i=0;i<V_MAX_LUT;i++) {
            set_vrsz_lut_coef(v_lut[i].coef, v_lut[i].in_n, v_lut[i].out_n);
          }
18      Clean_end_flag();
        run_ipu();
```

22.6 Special Instruction

A1. Resizing size feature

Input size (W x H)		Output size (W x H)	
Min	4x4	Disable vertical scale	Min: 4x4
			Max: 4095x4095
Max	4095x4095	Enable vertical scale	Min: 4x4
			Max: 1280x4095

A2. Color convention feature

Source format	Output format	Parameter configure (necessary)
RGB	RGB	IPU_CONTROL.CSC_EN =0 IPU_CONTROL. SPKG_SEL = 0 or 1
		D_FMT. IN_FMT
		D_FMT.OUT_FMT = 2'b00, 2'b01, 2'b10
YUV	RGB	IPU_CONTROL.CSC_EN =1
		IPU_CONTROL. SPKG_SEL
		D_FMT. IN_FMT
		D_FMT. IN_OFT ***(IPU_CONTROL. SPKG_SEL == 1)***
		D_FMT.OUT_FMT = 2'b00, 2'b01, 2'b10
		D_FMT.RGB_OUT_OFT.
		CSC_C0 (1,2,3,4)_COEF, CSC_OFSET_PARA
YUV	YUV (package)	IPU_CONTROL.CSC_EN =0

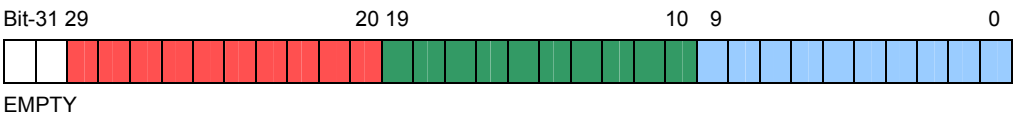
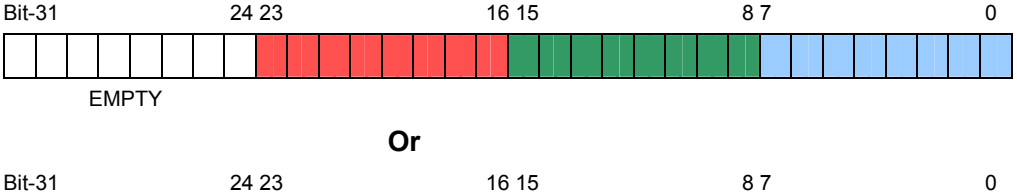
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		IPU_CONTROL. SPKG_SEL
		D_FMT. IN_FMT
		D_FMT. IN_OFT ***(IPU_CONTROL. SPKG_SEL == 1)***
		D_FMT.OUT_FMT = 2'b11

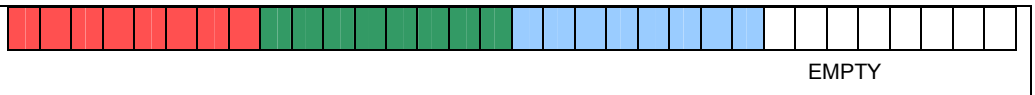
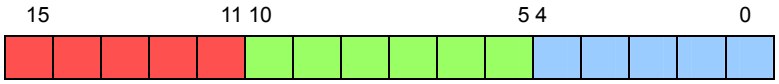
A3. YUV/YCbCr to RGB CSC Equations

Input data	Matrix	CSC_COEF
YUV	R = C0*(Y – X0) + C1*(V-128) G = C`0*(Y – X0) – C2*(U-128) – C3*(V-128) B = C0*(Y – X0) + C4*(U-128) X0: 0 C0: 1 C1: 1.4026 C2: 0.3444 C3: 0.7144 C4: 1.7730	CSC_C0_COEF = 0x400 CSC_C1_COEF= 0x59C CSC_C2_COEF = 0x161 CSC_C3_COEF = 0x2DC CSC_C4_COEF = 0x718
YCbCr	R = C0*(Y – X0) + C1*(Cr-128) G = C0*(Y – X0) – C2*(Cb-128) – C3*(Cr-128) B = C0*(Y – X0) + C4*(Cb-128) X0: 16 C0: 1.164 C1: 1.596 C2: 0.391 C3: 0.813 C4: 2.018	CSC_C0_COEF = 0x4A8 CSC_C1_COEF = 0x662 CSC_C2_COEF = 0x191 CSC_C3_COEF = 0x341 CSC_C4_COEF = 0x811

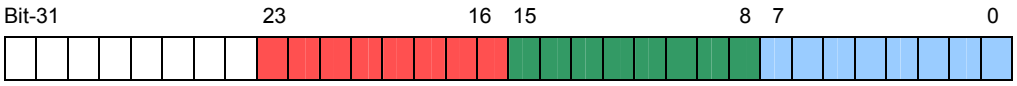
A4. Output data package format (RGB order)

Format	Package
RGBAAA	
RGB888	

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RGB555	
RGB565	
NOTE: All R/G/B data are little-endian type; all the empty bits in the above figure are filled with 0.	

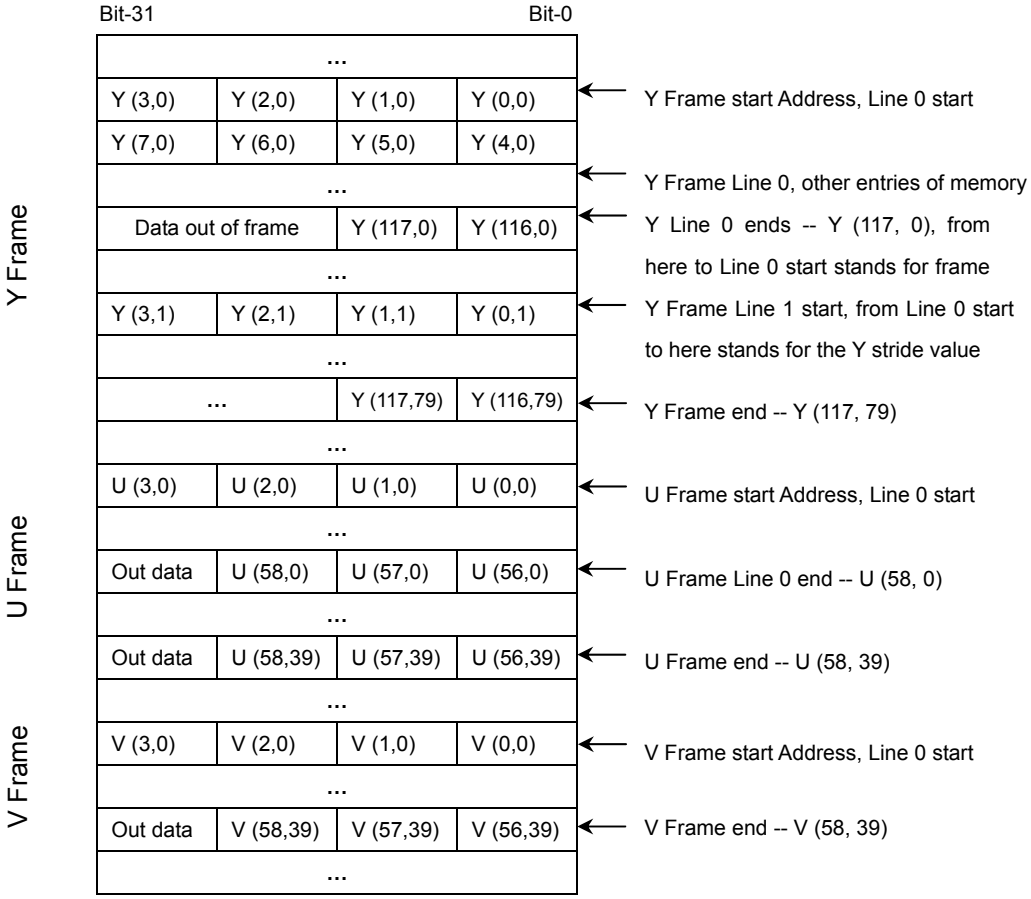
A5. Input data package format (RGB order)

Format	Package
RGBPACK	

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A6. Source Data storing format in external memory (separated YUV Frame)

Example: YUV420 118x80 frame



NOTES:

1 Every line's start address should be word aligned.

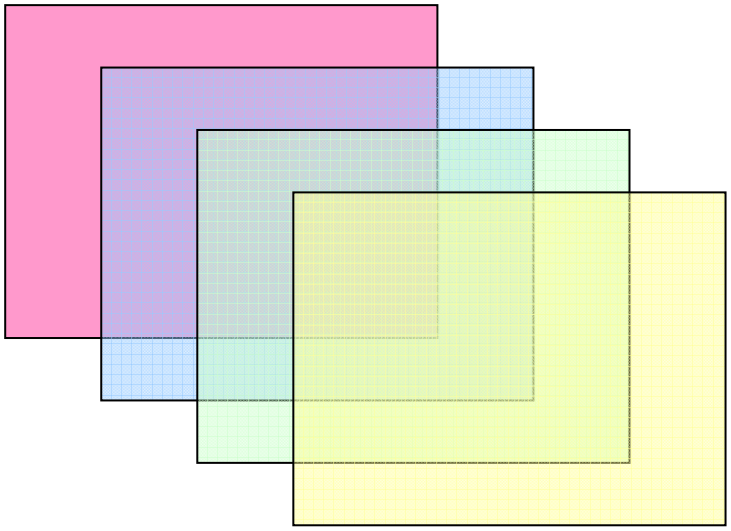
2 All pixel data should be stored as little-endian format.

3 Destination data (RGB) storing format in external memory is similar with above figure, but RGB555 and RGB565 frame's every line start address can be half-word aligned. (RGB888 frame still need word aligned)

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23 Alpha_osd

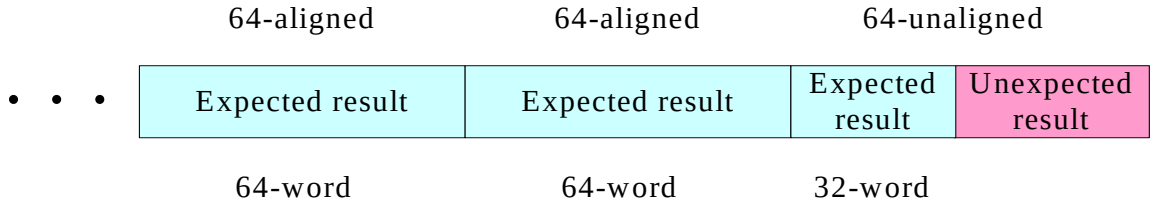
23.1 Overview



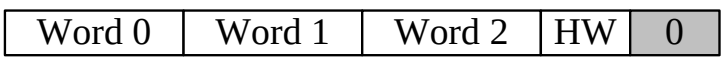
4-level overlay DMA, which can calculate Alpha Blending.

Features:

- Support ARGB8888, RGB565, RGB555 (16'h0000 means total transparent, others mean total overlaid). (this called pixel alpha mode)
- Each layer has an alpha value for all pixels (called frame alpha mode). Those value only use in a special mode, which all pixels in this layer use same alpha value
- Up to 800*480
- Software can change overlay orders
- The level of overlay can be set by software
- Software must make sure the address of source and destination are 64-word aligned. If not, alpha_osd will change the parts unaligned
  For example:

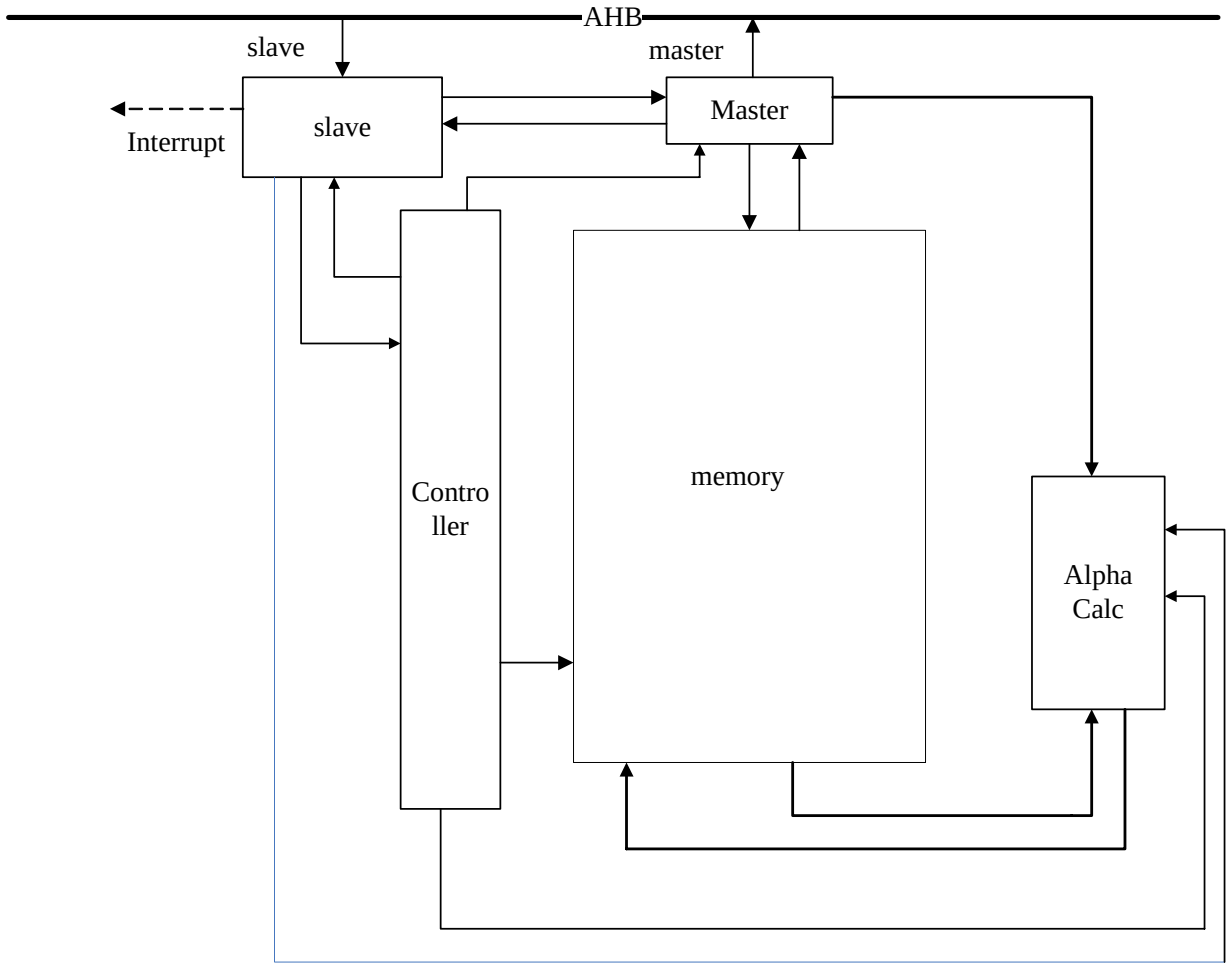


- Support 64-burst in AHB bus
- In RGB656 & RGB555mode, software must make sure each line aligned in word. If not, software need fill the extra half-word with 16'h0000



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23.2 Structure



23.3 Alpha blending function

This function is to calculate the Alpha blending. The blending is between two layers data and has 2 modes. One is the whole graph use one registered Alpha value and the other is each pixel have its own Alpha value. This function has 2 inputs, one (called foreground data in this module) is input foreground 0 data, and the other (called background data in this module) is input foreground 1 our background data determined by the display area. The calculate function is:

$$NewPixel = \frac{[(255 - Alpha) * background + Alpha * Foreground]}{255}$$

The calculate function that we used:

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$$NewPixel = \frac{[(256 - Alpha) * background + Alpha * Foreground + 128]}{256}$$
$$= \frac{[256 * background + Alpha * (Foreground - background) + 128]}{256}$$

Alpha == 255 ? NewPixel = Foreground

For simplify the calculator process, we use 256 to instead the original 255, then add a 128/256 to approach the exact result. In this case we can use a shift register instead of a divider. To change the formula's format, use two full adder (in fact one of them is a subtractor) and one multiplier instead of one full-adder and two multipliers. Notice that 256 * background + 128 do not need adder or multiplier, use one 16-bit register which high 8-bit save the value of background, and low 8-bit is 8'b1000_0000.

In different mode the input, output and the Alpha have different values:

Alpha_osd_enable:

When **alpha is disable**, the output equal to foreground.

When **alpha is enable**, the output is the calculating result.

Alpha_osd_mode and **format mode**:

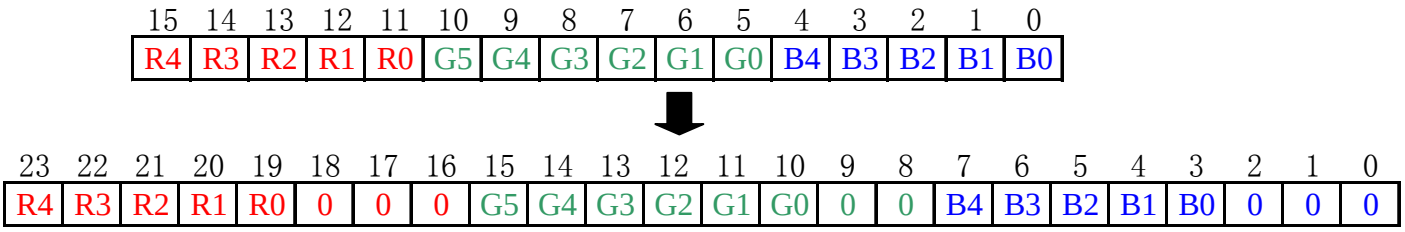
When alpha mode is **pixel alpha blending**:

Output low 24bits equal to the calculating result of CHANNEL0, high 8bits equal to the Alpha of the bottom frame, and alpha value comes from the high 8-bits of foreground multiple the corresponding alpha value form slv_reg_alphavalue register in case **format mode is ARGB8888**; output is decided by whether the value of foreground is 16'b0000 in case **format mode is RGB565 or RGB555**.

When alpha mode is **frame alpha blending**:

Output equal to the calculating result of CHANNEL0 high 8bits equal to the Alpha of the bottom frame, and alpha value comes from the slv_reg_alphavalue register in case **format mode is ARGB8888**; output is compose of results of CHANNEL0 and CHANNEL1, inputs of two channels must do format transforming as shown the figure below, the alpha value comes from the slv_reg_alphavalue register, specially foreground is all zero means total transparent in case **format mode is RGB565 or RGB555**.

RGB565



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RGB555

0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	0	0	0	G4	G3	G2	G1	G0	0	0	0	B4	B3	B2	B1	B0	0	0	0

23.4 Register Description

In this section, we will describe the registers in Alpha_osd. Following table lists all the registers definition. All register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
Reg_addr0	Address of DMA channel 0	RW	0x00000000	0x13070000	32
Reg_addr1	Address of DMA channel 1	RW	0x00000000	0x13070004	32
Reg_addr2	Address of DMA channel 2	RW	0x00000000	0x13070008	32
Reg_addr3	Address of DMA channel 3	RW	0x00000000	0x1307000C	32
Reg_waddr	Address of the destination of DMA	RW	0x00000000	0x13070010	32
Reg_addrlen	Length of DMA channel	RW	0x00000000	0x13070014	32
Slv_reg_ alphavalue	Alpha value of 4 frames	RW	0x00000000	0x13070018	32
CTRL*1	Ctrl register	RW	0x00060000	0x1307001C	32
int	Interrupt flag	RW	0x00000000	0x13070020	32
Clk_Gate	Control hclk gate	RW	0x00000001	0x13070048	32

NOTE:

*1: This register must be set at last and please make sure other registers have been set correctly, if not you will get result unexpected.

23.4.1 Reg_addr0 ~Reg_addr3, Reg_waddr

These 5 registers define the address of 4 source frames and the destination respectively.

Reg_addr0 **0x13070000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_addr0																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Reg_addr1 **0x13070004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_addr1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg_addr2 **0x13070008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_addr2																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg_addr3 **0x1307000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_addr3																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg_waddr **0x13070010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_waddr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.4.2 Reg_addrlen

This register defines the length of each frame.

Reg_addrlen **0x13070014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reg_addrlen																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.4.3 Slv_reg_alphavalue

This register defines the alpha values for each frame.

In the case of **ARGB8888 pixel alpha blending mode**, the alpha for calculating is high 8-bits of each foreground pixel multiplying corresponding alpha value in this register;

In the case of **RGB565 and RGB555 pixel alpha blending mode,** this register is unused;

In other cases, the alpha for calculating comes from corresponding alpha value in this register directly.

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Slv_reg_alphavalue 0x13070018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Alpha value for addr3								Alpha value for addr2								Alpha value for addr1								Alpha value for addr0							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.4.4 CTRL

This register is combined by several control bits.

CTRL 0x1307001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												Frmlv		Frm_end	Alpha_start	Int_mask	Channel_level								Alpha mode				Format mode	Alpha enable		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

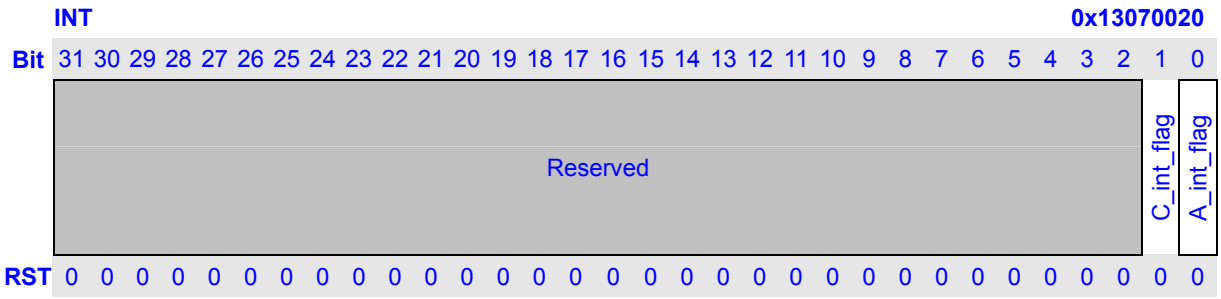
Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:18	Frmlv	[19:18] / Number of frames 00 / invalid 01 / 2 10 / 3 11 / 4	RW
17	Frm_end	1: all frames' alpha blending are finished and send to frame buffer 0: alpha_osd is under working	R
16	Alpha_start	Writing 1 to this bit to start alpha_osd. When alpha_osd start to work, this bit is cleared by hardware automatically.	RW
15	Int_mask	Interrupt mask. 1: enable interrupt 0: disable interrupt	RW
14:7	Channel_level	2bits x 4, 4-layer order form up to down. When Frmlv was 2'b01 , [14:11] is useless; When Frmly was 2'b10, [14:13] is useless. Bits / Description 14:13 / The top frame ID 12:11 / The secondary top frame ID 10:9 / The secondary bottom frame ID 8:7 / The bottom frame ID	RW
6:3	Alpha_mode	1bit x 4, represent alpha mode of each frame corresponded with addr0~addr3.	RW

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<table>
<tr><td></td><td></td><td>0: pixel alpha blending
1: frame alpha blending
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>6</td><td>Alpha mode for addr3 frame</td></tr><tr><td>5</td><td>Alpha mode for addr2 frame</td></tr><tr><td>4</td><td>Alpha mode for addr1 frame</td></tr><tr><td>3</td><td>Alpha mode for addr0 frame</td></tr></table></td><td></td></tr>
<tr><td>2:1</td><td>Format mode</td><td><table><tr><th>[2:1]</th><th>Format</th></tr><tr><td>00</td><td>RGB565</td></tr><tr><td>01</td><td>RGB555</td></tr><tr><td>10</td><td>ARGB8888</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>RW</td></tr>
<tr><td>0</td><td>Alpha_enable</td><td>1: alpha enable
0: alpha disable</td><td>RW</td></tr>
</table>

23.4.5 INT

When frm_end became high, alpha_osd would generate interrupt signal if INT_mask was high, and interrupt would last until software written 1 to this register.



Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	C_Int_flag	Compress end flag. writing 1 to this bit to clear flag. 0:no interrupt; 1:interrupt. ***NOTE:** this flag(c_int_flag) used in compress module.	RW
0	A_Int_flag	Alpha_osd end flag. writing 1 to this bit to clear flag. 0:no interrupt; 1:interrupt.	RW

23.4.6 Clk_Gate

This register set hclk gate for aosd_comp.

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CLK_Gate 0x13070048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															Gate_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	Gate_en	1: Enable hclk gate when controller idle	RW

23.5 Alpha_osd Operation

1 Look at frm_end.
Read CTRL and make sure frm_end is 1.

2 Configuration1.
Set Reg_addr0~Reg_addr3, Reg_waddr, Reg_addrlen and Slv_reg_alphavalue.

3 Configuration2 and start.
Set CTRL. If you want to start alpha_osd, set Alpha_start (CTRL[16]) to 1, if not set it to 0.
Be aware that Frmlv's default value is 2'b01, don't set it to 2'b00.

4 Interrupt handle.
Do configuration1 , configuration2 and start. If you want to start alpha_osd, set Alpha_start (CTRL[16]) to 1, if not set it to 0.
Clear the interrupt flag by writing 1 to Int.

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24 LVDS Controller

24.1 Overview

This product is a single-Link high speed LVDS (Low-Voltage Differential Signaling) transmitter used for digital flat panel display systems. It's compatible with ANSI/TIA/EIA-644-A (LVDS) Standard. The transmitter converts 28bits parallel TTL data into four LVDS data streams. An in-phase transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. It support full HDTV display up to 1920x1080p @ 60 Hz.

Feature:

- 25 to 135 MHz input clock support
- Supports VGA, SVGA, XGA , SXGA and HDTV
- Compatible with TIA/EIA-644 LVDS standard
- Support 24-bit Flat Panel Display
- Support VESA and JEIDA LVDS Data format

24.2 Register Description

In this section, we will describe the registers in LVDS controller. Following table lists all the register definitions. All registers' 32bit addresses are physical addresses. And detailed function of each register will be described below.

Table 24-1 LVDS Register Description

Name	Description	RW	Reset Value	Address	Access Size
TXCTRL	LVDS Transmitter 's Control Register	RW	0x80040060	0x130503C0	32
TXPLL0	LVDS Transmitter's PLL Control Register 0	RW	0x60001304	0x130503C4	32
TXPLL1	LVDS Transmitter's PLL Control Register 1	RW	0x61000000	0x130503C8	32

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24.2.1 TXCTRL (LVDS Transmitter Control Register)

The register TXCTRL is used to control LVDS to work.

TXCTRL **0x130503C0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LVDS_MODEL_SEL	TX_PDB	TX_PDB_CK	Reserved	RESERVE_7	RESERVE_6	RESERVE_5	RESERVE_4	RESERVE_3	RESERVE_2	RESERVE_1	RESERVE_0	Reserved	TX_RSTB	TX_CKBIT_PHA_SEL	TX_CKBYTE_PHA_SEL	TX_CKOUT_PHA_S			TX_CKOUT_SET	TX_OUT_SEL	TX_DLY_SEL			TX_AMP_ADJ	TX_LVDS	TX_CR			TX_CR_CK	TX_OD_S	TX_OD_EN
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
31	LVDS_MODEL_SEL	VESA model or JEIDA model select. 0: JEIDA; 1:VESA.	RW
30	TX _PDB	Data channel Power down. 0: power down.	RW
29	TX_PDB_CK	Clock channel Power down. 0: power down.	RW
28	Reserved	Writing has no effect, read as zero.	R
27	LVDS_RESERVE_7	Reserved.	RW
26	LVDS_RESERVE_6	Reserved.	RW
25	LVDS_RESERVE_5	Reserved.	RW
24	LVDS_RESERVE_4	Reserved.	RW
23	LVDS_RESERVE_3	Reserved.	RW
22	LVDS_RESERVE_2	Reserved.	RW
21	LVDS_RESERVE_1	Reserved.	RW
20	LVDS_RESERVE_0	Reserved.	RW
19	Reserved	Writing has no effect, read as zero.	R
18	TX_RSTB	System reset signal. 0: Reset.	RW
17	TX_CKBIT_PHA_SEL	7x clock sampling edge configuration. 0: Rising edge; 1: Falling Edge.	RW
16	TX_CKBYTE_PHA_SEL	1x clock sampling edge configuration. 0: Rising edge; 1:Falling Edge.	RW
15:13	TX_CKOUT_PHA_S	Output data start-edge tuning in 1x clock output mode. 000: 0 of T_{7X} 001: 1 of T_{7X} … 111: 7 of T_{7X}	RW
12	TX_CKOUT_SET	TX clock channel output clock frequency set. 0: 1x clock output 1: 7x clock output	RW

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11	TX_OUT_SEL	Transmitter output select. 0: LVDS output; 1: CMOS RGB output.	RW
10:8	TX_DLY_SEL	Input clock edge delay control, for setup/hold time fine tuning.	RW
7	TX_AMP_ADJ	LVDS output swing control. When AMP_ADJ=1, LVDS output swing is adjustable by CR<2:0>.	RW
6	TX_LVDS	Output amplitude tuning in mode of 'TX _AMP_CTRL'='0'. 0b, V_{OD}=200mV; 1b, V_{OD}=350mV.	RW
5:3	TX_CR	Digital logic input used to control output swing level.	RW
2	TX_CR_CK	Additional control bit of output swing level.	RW
1	TX_OD_S	Output level selectable pin.	RW
0	TX_OD_EN	Tx output control functions. 0: Disable ;1: Enable.	RW

24.2.2 TXPLL0 (LVDS Transmitter's PLL Control Register 0)

The register TXPLL0 is used to control PLL to work.

TXPLL0 **0x130503C4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LVDS_PLL_LOCK	PLL_DIS	BG_PWD	Reserved	PLL_SSC_EN	PLL_SSC_MODE	PLL_TEST	Reserved		PLL_POST_DIVA		PLL_POST_DIVB					Reserved	PLL_PLLN							PLL_TEST_DIV		PLL_IN_BYPASS	PLL_INDIV				
RST	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31	LVDS_PLL_LOCK	Lock detection output. 1: Lock.	R
30	PLL_DIS	PLL power down control. 1: power down.	RW
29	BG_PWD	Band-gap power down control. 1: power down.	RW
28	Reserved	Writing has no effect, read as zero.	R
27	PLL_SSC_EN	SSC function enable control. 1: Enable.	RW
26	PLL_SSC_MODE	SSC mode select. 0: Down spread 1: Center spread	RW
25	PLL_TEST	Test enable control. 1:Enable.	RW
24:23	Reserved	Writing has no effect, read as zero.	R

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22:21	PLL_POST_DIVA	Post divider control bits A.	RW
20:16	PLL_POST_DIVB	N/C.	RW
15	Reserved	Writing has no effect, read as zero.	R
14:8	PLL_PLLN[6:0]	PLL feedback divider value configure.	RW
7:6	PLL_TEST_DIV	Output divider ratio control in test mode. 00: 1/2 01: 1/4 10: 1/8 11: 1/16	RW
5	PLL_IN_BYPASS	Input divider bypass.	RW
4:0	PLL_INDIV	Input divider value configure.	RW

24.2.3 TXPLL1 (LVDS Transmitter's PLL Control Register 0)

The register TXPLL1 is used to control PLL to work.

TXPLL1 **0x130503C8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PLL_ICP_SEL			Reserved	PLL_KVCO		PLL_IVCO_SEL		PLL_SSCN							PLL_COUNT													PLL_GAIN			
RST	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	PLL_ICP_SEL	Charge-pump current configure.	RW
28	Reserved	Writing has no effect, read as zero.	R
27:26	PLL_KVCO	VCO gain control.	RW
25:24	PLL_IVCO_SEL	VCO biasing current setup.	RW
23:17	PLL_SSCN	Internal divider for 30KHz clock generation.	RW
16:4	PLL_COUNT	SSC counter.	RW
3:0	PLL_GAIN	SSC counter gain.	RW

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25 Camera Interface Module

25.1 Overview

The camera interface module (CIM) supports commonly available CMOS or CCD type image sensors. The CIM sources the digital image stream through a common 8-bit parallel digital protocol. The CIM can directly connect to external CMOS image sensors and ITU656 standard video decoders.

25.1.1 Features

- Input image size up to 4096x4096 pixels
- Max. VGA for image preview
- Max. VGA for video record
- Integrated DMA
- Supported data format: YCbCr 4:4:4, YCbCr 4:2:2 and other formats
- Output frame format
  - Packaged : for all data format
  - Separated: for YCbCr 4:4:4 and YCbCr 4:2:2
- Supports ITU656 (YCbCr 4:2:2) input
- Configurable CIM_VSYNC and CIM_HSYNC signals: active high/low
- Configurable CIM_PCLK: active edge rising/falling
- 256x33 image data receive FIFO (RXFIFO)
- PCLK max. 80MHz
- Output format: csc mode is YCbCr 4:2:2, bypass mode is the input data format
- Configurable output order

25.1.2 Pin Description

Table 25-1 Camera Interface Pins Description

Name	I/O	Description
CIM_MCLK	O	CIM work clock
CIM_PCLK	I	Pixel clock from Image Sensor
CIM_VSYNC	I	Vertical synchronous from Image Sensor
CIM_HSYNC	I	Horizontal synchronous from Image Sensor
CIM_DATA[7:0]	I	Data bus from Image Sensor

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25.2 CIM Special Register

The special registers are for CIM to configure and control the interface and DMA operation. The table below lists these registers.

Table 25-2 CIM Registers

Name	RW	Reset Value	Address	Access Size
CIMCFG	RW	0x00000000	0x13060000	32
CIMCR	RW	0x00000000	0x13060004	32
CIMST	RW	0x02020202	0x13060008	32
CIMIID	R	0x00000000	0x1306000C	32
CIMDA	RW	0x00000000	0x13060020	32
CIMFA	R	0x00000000	0x13060024	32
CIMFID	R	0x00000000	0x13060028	32
CIMCMD	R	0x00000000	0x1306002C	32
CIMSIZE	RW	0x00000000	0x13060030	32
CIMOFFSET	RW	0x00000000	0x13060034	32
CIMYFA	R	0x00000000	0x13060038	32
CIMYCMD	R	0x00000000	0x1306003C	32
CIMCBFA	R	0x00000000	0x13060040	32
CIMCBCMD	R	0x00000000	0x13060044	32
CIMCRFA	R	0x00000000	0x13060048	32
CIMCRCMD	R	0x00000000	0x1306004C	32
CIMCR2	RW	0x00000000	0x13060050	32

25.2.1 CIM Configuration Register (CIMCFG)

CIMCFG **0x13060000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EEOFEN	EXP	RF_TRIG						BW			SEP	ORDER		DF		INV_DAT	VSP	HSP	PCP	BURST_TYPE		DUMMY	E_VSYNC	LM	PACK			FP	BYPASS	DSM	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	EEOFEN	Early EOF Mode Enable. 0: EEOF mode is disabled 1: When CIMCR.EEOF_LINE lines data has been transferred of a frame, the EEOF flag will be set, and the EEOF interrupt will occur	RW

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<table>
<tr><td>30</td><td>EXP</td><td>Expand mode for CIM_DATA width.
0: CIM_DATA width = 8
1: CIM_DATA width > 8</td><td></td></tr>
<tr><td>29:24</td><td>RF_TRIG</td><td>Specifies the trigger value of RXFIFO.
<table>
<tr><th>CIMCFG.BURST_TYPE</th><th>RF_TRIG = n</th></tr>
<tr><td>INCR4</td><td>Trigger value is (n + 1) * 4</td></tr>
<tr><td>INCR8</td><td>Trigger value is (n + 1) * 8</td></tr>
<tr><td>INCR16</td><td>Trigger value is (n + 1) * 16</td></tr>
<tr><td>INCR32</td><td>Trigger value is (n + 1) * 32</td></tr>
</table></td><td>RW</td></tr>
<tr><td>23:22</td><td>BW</td><td>Bus width of CIM_DATA Interface.
When BW is n, the bus width is (n+9) bits.</td><td>RW</td></tr>
<tr><td>20</td><td>SEP</td><td>Separate frame format enable.
Used in output data format of YCbCr 4:4:4 and YcbCr 4:2:2.
0: Output is packaged frame format
1: Output is separated frame format</td><td>RW</td></tr>
<tr><td>19:18</td><td>ORDER</td><td>Input data stream order.
<table>
<tr><td></td><td>YCbCr 4:4:4</td><td>ITU656/YCbCr 4:2:2</td></tr>
<tr><td>00</td><td>YCbCr</td><td>Y_0CbY_1Cr</td></tr>
<tr><td>01</td><td>YCrCb</td><td>Y_0CrY_1Cb</td></tr>
<tr><td>10</td><td>CbCrY</td><td>CbY_0CrY_1</td></tr>
<tr><td>11</td><td>CrCbY</td><td>CrY_0CbY_1</td></tr>
</table></td><td>RW</td></tr>
<tr><td>17:16</td><td>DF</td><td>Input data format.
00: reserved
01: YCbCr 4:4:4
10: YCbCr 4:2:2
11: ITU656 YCbCr 4:2:2</td><td>RW</td></tr>
<tr><td>15</td><td>INV_DAT</td><td>Inverse every bit of input data.
0: not inverse; 1: inverse.</td><td>RW</td></tr>
<tr><td>14</td><td>VSP</td><td>VSYNC polarity selection. When VSYNC signal is input from pin CIM_VSYNC, this bit specifies the VSYNC signal active level and leading edge. When VSYNC is retrieved from SAV&EAV, this bit is ignored.
0: VSYNC signal active high, VSYNC signal leading edge is rising edge
1: VSYNC signal active low, VSYNC signal leading edge is falling edge</td><td>RW</td></tr>
<tr><td>13</td><td>HSP</td><td>Specifies the HSYNC signal active level and leading edge.
0: HSYNC signal active high, HSYNC signal leading edge is rising edge
1: HSYNC signal active low, HSYNC signal leading edge is falling edge</td><td>RW</td></tr>
<tr><td>12</td><td>PCP</td><td>Specifies the PCLK working edge.
0: Data is sampled by PCLK rising edge
1: Data is sampled by PCLK falling edge</td><td>RW</td></tr>
<tr><td>11:10</td><td>BURST_
TYPE</td><td>DMA burst type.
00: INCR4
01: INCR8</td><td>RW</td></tr>
</table>

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		10: INCR16 11: INCR32	
9	DUMMY	DUMMY zero function. When DUMMY is 1, CIM hardware adds one byte zero to every 3 input data bytes to form 32-bit data. 0: DUMMY zero function disabled 1: DUMMY zero function enabled	RW
8	E_VSYNC	External / internal VSYNC selection. When DSM is ITU656Progressive Mode, VSYNC can be external (provided by sensor) or internal (retrieved from SAV&EAV). This bit only valid for ITU656Progressive Mode; In other DSM modes, this bit should always be 0. 0: Internal VSYNC mode, pin CIM_VSYNC is ignored 1: External VSYNC mode, VSYNC is provided by image sensor via pin CIM_VSYNC	RW
7	LM	Line Mode for ITU656. 0: EAV is before SAV in each line 1: SAV is before EAV in each line	RW
6:4	PACK	Data packing mode, pack 8-bit input data into 32-bit data for FIFO. **PACK** / **Bypass Mode** / **CSC Mode** 3'b000 / 0x 11 22 33 44 / 0x Y_0 Cb Y_1 Cr 3'b001 / 0x 22 33 44 11 / 0x Cb Y_1 Cr Y_0 3'b010 / 0x 33 44 11 22 / 0x Y_1 Cr Y_0Cb 3'b011 / 0x 44 11 22 33 / 0x Cr Y_0 Cb Y_1 3'b100 / 0x 44 33 22 11 / 0x Cr Y_1 Cb Y_0 3'b101 / 0x 33 22 11 44 / 0x Y_1 Cb Y_0 Cr 3'b110 / 0x 22 11 44 33 / 0x Cb Y_0 Cr Y_1 3'b111 / 0x 11 44 33 22 / 0x Y_0 Cr Y_1 Cb In this table, 0x11, 0x22, 0x33 and 0x44 mean the received data from the sensor, 0x11 is received first and 0x44 is received last, and Y0 is received before Y1.	6:4
3	FP	Field flag polarity selection. When ITU656 progressive stream is input, this bit specifies the field flag active level. When other modes are used, this bit is ignored. 0: Field flag active low 1: Field flag active high	RW
2	BYPASS	0: enable CIM CSC 1: disable CIM CSC	RW
1:0	DSM	Data sample mode. Please refer to the table below.	RW

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			DSM	Description		
			2'b00	ITU656Progressive Mode		
			2'b01	ITU656Interlace Mode		
			2'b10	Gated Clock Mode		
			2'b11	Reserved		

25.2.2 CIM Control Register (CIMCR)

CIMCR **0x13060004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EEOF_LINE												FRC				DMA_EEOFM	WINE	VDDM	DMA_SOFM	DMA_EOFM	DMA_STOPM	RF_TRIGM	RF_OFM	DMA_SYNC	Reserved	H_SYNC	PPW		DMA_EN	RF_RST	ENA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	EEOF_LINE	When EEOF_LINE lines data has been transferred of a frame, the EEOF flag will be set, and the EEOF interrupt will occur.	RW
19:16	FRC	CIM frame rate control. If FRC = n, CIM sampling one frame from every (n+1) frames from the sensor.	RW
15	DMA_EEOFM	The control bit to enable EEOF interrupt.	RW
14	WINE	To enable window-image. Used to indicate whether the registers CIMSIZE and CIMOFFSET work or not. 0: the value in CIMSIZE and CIMOFFSET will be ignored 1: the value in CIMSIZE and CIMOFFSET will be used	RW
13	VDDM	The control bit to enable VDD interrupt. 0: disable; 1: enable.	RW
12	DMA_SOFM	The control bit to enable DMA_SOF interrupt. 0: disable; 1: enable.	RW
11	DMA_EOFM	The control bit to enable DMA_EOF interrupt. 0: disable; 1: enable.	RW
10	DMA_STOPM	The control bit to enable DMA_STOP interrupt. 0: disable; 1: enable.	RW
9	RF_TRIGM	The control bit to enable RXF_TRIG interrupt. 0: disable; 1: enable.	RW
8	RF_OFM	The control bit to enable RX_OF interrupt. 0: disable; 1: enable.	RW
7	DMA_SYNC	The control bit to enable DMA synchronization. 0: The valid data input to CIM will be transferred by DMA to	RW

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		external memory 1: When a new descriptor-DMA transfer starts with writing CIMDA, a frame synchronization will be done, and the data in RXFIFO will be ignored	
6	Reserved	Writing has no effect, read as zero.	R
5	H_SYNC	Horizontal Sync Enable. 0: disable 1: enable It is only used when CIMCFG.SEP is 1.	RW
4:3	PPW	Pixels per Word. Only used when WINE is 1. 00: 2 pixels per 1 word 01: 1 pixel per 1 word 10: 1 pixel per 2 word 11: reserved	RW
2	DMA_EN	Enable / disable the DMA function. 0: disable DMA; 1: enable DMA.	RW
1	RF_RST	RXFIFO software reset. Setting 1 to RXF_RST can reset RXFIFO immediately. Setting 0 to RXF_RST can stop resetting RXFIFO. After reset, RXFIFO is empty.	RW
0	ENA	Enable / disable the CIM module. Setting 1 to ENA can enable CIM. When CIM is working, clear ENA to 0 can stop CIM immediately. 0: CIM is not enabled, or disable CIM immediately 1: CIM is enabled, or enabling CIM	RW

25.2.3 CIM Control Register 2 (CIMCR2)

CIMCR **0x13060050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										OP		Reserved	OPE	EMM	APM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R

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<table>
<tr><td>5:4</td><td>OP</td><td>Optional Priority Configuration. Only used when OPE is set to 1.

<table><tr><th>PG</th><th>CIM AHB Priority</th><th>Number of Data in FIFO</th></tr><tr><td>2’b00</td><td>0
1
2
3</td><td>n <= 8
8 < n <= 16
16 < n <= 32
32 < n</td></tr><tr><td>2’b01</td><td>0
1
2
3</td><td>n <= 16
16 < n <= 32
32 < n <= 64
64 < n</td></tr><tr><td>2’b10</td><td>0
1
2
3</td><td>n <= 32
32 < n <= 64
64 < n <= 96
96 < n</td></tr><tr><td>2’b11</td><td>0
1
2
3</td><td>n <= 64
64 < n <= 96
96 < n <= 128
128 < n</td></tr></table>
It is suggested to use 2’b10.</td><td>RW</td></tr>
<tr><td>3</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>2</td><td>OPE</td><td>Optional Priority Mode Enable Control. Only used when APM is 1.
0: CIM calculates the priority according to the fifo status
1: CIM calculates the priority according to OPG which is configured by software</td><td>RW</td></tr>
<tr><td>1</td><td>EME</td><td>Emergency Mode Enable Control.
0: Emergency Mode Disable
1: Emergency Mode Enable</td><td>RW</td></tr>
<tr><td>0</td><td>APM</td><td>Auto Priority Mode Enable Control.
0: Auto priority mode disable. CIM uses the priority set by arbiter
1: Auto priority mode enable. CIM can use the priority according the fifo status</td><td>RW</td></tr>
</table>

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25.2.4 CIM Status Register (CIMST)

CIMST 0x13060008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Cr_RF_OF	Cr_RF_TRIG	Cr_RF_EMPTY	Reserved					Cb_RF_OF	Cb_RF_TRIG	Cb_RF_EMPTY	Reserved					Y_RF_OF	Y_RF_TRIG	Y_RF_EMPTY	Reserved	DMA_EEOF	DMA_SOF	DMA_EOF	DMA_STOP	RF_OF	RF_TRIG	RF_EMPTY	VDD
RST	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27	Cr_RF_OF	Cr_RXFIFO over flow. When Cr_RXFIFO over flow happens, Cr_RX_OF is set 1. Can generate interrupt if CIMCR.RF_OFM bit is set. Write 0 to this bit to clear.	RW
26	Cr_RF_TRIG	Cr_RXFIFO trigger. Indicates whether Cr_RXFIFO meet the trigger value or not. Can generate interrupt if CIMCR.RF_TRIGM bit is set. 0: Cr_RXFIFO does not meets the trigger value 1: Cr_RXFIFO meets the trigger value	R
25	Cr_RF_EMPTY	Cr_RXFIFO empty. Indicates whether Cr_RXFIFO is empty or not. After reset, RXFIFO is empty, and Cr_RX_EMPTY is 1. 0: Cr_RXFIFO is not empty 1: Cr_RXFIFO is empty	R
24:20	Reserved	Writing has no effect, read as zero.	R
19	Cb_RF_OF	Cb_RXFIFO over flow. When Cb_RXFIFO over flow happens, Cb_RX_OF is set 1. Can generate interrupt if CIMCR.RF_OFM bit is set. Write 0 to this bit to clear.	RW
18	Cb_RF_TRIG	Cb_RXFIFO trigger. Indicates whether Cb_RXFIFO meet the trigger value or not. Can generate interrupt if CIMCR.RF_TRIGM bit is set. 0: Cb_RXFIFO does not meets the trigger value 1: Cb_RXFIFO meets the trigger value	R
17	Cb_RF_EMPTY	Cb_RXFIFO empty. Indicates whether Cb_RXFIFO is empty or not. After reset, Cb_RXFIFO is empty, and Cb_RX_EMPTY is 1. 0: Cb_RXFIFO is not empty 1: Cb_RXFIFO is empty	R
16:12	Reserved	Writing has no effect, read as zero.	R
11	Y_RF_OF	Y_RXFIFO over flow. When Y_RXFIFO over flow happens,	RW

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		Y_RX_OF is set 1. Can generate interrupt if CIMCR.RF_OFM bit is set. Write 0 to this bit to clear.	
10	Y_RF_TRIG	Y_RXFIFO trigger. Indicates whether Y_RXFIFO meet the trigger value or not. Can generate interrupt if CIMCR.RF_TRIGM bit is set. 0: Y_RXFIFO does not meets the trigger value 1: Y_RXFIFO meets the trigger value	R
9	Y_RF_EMPTY	Y_RXFIFO empty. Indicates whether Y_RXFIFO is empty or not. After reset, Y_RXFIFO is empty, and Y_RX_EMPTY is 1. 0: Y_RXFIFO is not empty 1: Y_RXFIFO is empty	R
8	Reserved	Writing has no effect, read as zero.	R
7	DMA_EEOF	When set to 1, indicate the DMA has transferred CIMCTRL.EEOF_LINE lines data of a frame. Write 0 to this bit to clear.	RW
6	DMA_SOF	When set to 1, Indicate the DMA start a transfer from RXFIFO to a frame buffer. Write 0 to this bit to clear.	RW
5	DMA_EOF	When set to 1, indicate the DMA complete a transfer from RXFIFO to a frame buffer. Write 0 to this bit to clear.	RW
4	DMA_STOP	When set to 1, indicate the DMA complete transferring data and stop the operation. Can generate interrupt if CIMCR.DMA_STOPM bit is set. Write 0 to this bit to clear.	RW
3	RF_OF	RXFIFO over flow. When RXFIFO over flow happens, RX_OF is set 1. Can generate interrupt if CIMCR.RF_OFM bit is set. Write 0 to this bit to clear.	RW
2	RF_TRIG	RXFIFO trigger. Indicates whether RXFIFO meet the trigger value or not. When the valid data number in RXFIFO reaches the trig value, RXF_TRIG is set 1; when the valid data number in RXFIFO do not reach the trig value, RXF_TRIG is set 0. Can generate interrupt if CIMCR.RF_TRIGM bit is set. 0: RXFIFO does not meets the trigger value 1: RXFIFO meets the trigger value	R
1	RF_EMPTY	RXFIFO empty. Indicates whether RXFIFO is empty or not. After reset, RXFIFO is empty, and RX_EMPTY is 1. 0: RXFIFO is not empty 1: RXFIFO is empty	R
0	VDD	CIM disable done. Indicate this module is disabled after clear the	RW

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		CIMCR.ENA bit to disable the CIM module. Can generate interrupt if CIMCR.DMA_VDDM bit is set. 0: CIM has not been disabled 1: CIM has been disabled Write 0 to this bit to clear.	

25.2.5 CIM Interrupt ID Register (CIMIID)

CIMIID **0x1306000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID	Interrupt frame ID. Contains a copy of the Frame ID register (CIMFID) from the descriptor currently being processed when a DMA_SOF or DMA_EOF interrupt is generated. CIMIID is written to only when CIMCMD.SOFINT or CIMCMD.EOFINT is high. As such, the register is considered to be sticky and will be overwritten only when the associated interrupt is cleared by writing the CIM state register.	R

25.2.6 CIM Descriptor Address (CIMDA)

CIMIDA **0x13060020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	NDA	Next descriptor physical address in external memory. DMAC gets the next descriptor according to it after finishing the current one. The target address Bits [3:0] must be zero to be aligned to 16-byte boundary.	RW

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25.2.7 CIM Frame buffer Address Register (CIMFA)

CIMIFA																														0x13060024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FPA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FPA	Frame buffer physical address in external memory when CIMCFG. SEP is 0. When starts CIM, DMA transfers data from RXFIFO to frame buffer. This address is increased by hardware automatically. Bits [6:0] must be zero to be aligned to 32-word boundary.	R

NOTE: CIMFA comes from DMA Descriptor, so here it is read-only.

25.2.8 CIM Frame ID Register (CIMFID)

CIMFID																														0x13060028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID	Frame ID. The particular use of this field is up to the software. This ID will be copied to the CIMIID register when an interrupt occurs.	R

NOTE: CIMFID comes from DMA Descriptor, so here it is read-only.

25.2.9 CIM DMA Command Register (CIMCMD)

CIMFID																														0x1306002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOFINT	EOFINT	EEOFINTEn	STOP	Reserved				LEN																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31	SOFINTEn	Interrupt enable for DMA starting a frame-buffer transfer. 1: DMA will set CIMSTATE.DMA_SOF when start of a frame-buffer transfer When one frame uses several buffers, it is suggested to set SOFINTEn of first buffer only.	R
30	EOFINTEn	Interrupt enable for DMA ending a frame-buffer transfer. 1: DMA will set CIMSTATE.DMA_EOF when CIMCMD.LEN is decreased to 0, which means end of a frame-buffer transfer When one frame uses several buffers, it is suggested to set EOFINTEn of last buffer only.	R
29	EEOFINTEn	Interrupt enable for DMA issuing an earlier eof interrupt.	R
28	STOP	DMA stop. When DMA complete transferring data, STOP bit decides whether DMA should loading next descriptor or not. 0: DMA start loading next descriptor 1: DMA stopped, and CIMSTATE.DMA_STOP bit is set 1 by hardware	R
27	OFRCVEN	Auto recovery enable when there is RXFIFO overflow. 0: No auto recovery when overflow occurs, thus the software should do something 1: Auto recovery enable, the hardware will correct the overflow	
26:24	Reserved	Writing has no effect, read as zero.	R
23:0	LEN	Length of transfer in words. Indicate the number of words to be transferred by DMA to a frame buffer. LEN = 0 is not valid. DMA transfers data according to LEN. Each time one or more word(s) been transferred, LEN is decreased automatically.	R

25.2.10 CIM Window-image Size (CIMSIZE)

CIMFID 0x13060030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			LPF													Reserved			PPL												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:16	LPF	Lines per frame for CIM output.	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	PPL	PPL must be multiples of 2. In fact, the number of CIM output data in word is equal to PPL/2.	RW

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NOTE:

When CIMCFG.SEP is 1, the total pixel number of window-size must be multiple of 4 or 8.

- When output data format is YCBCR4:4:4, it must be multiple of 4.
- When output data format is YCBCR4:2:2, it must be multiple of 8.

25.2.11 CIM Image Offset (CIMOFFSET)

CIMFID **0x13060034**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				V_OFFSET												Reserved				H_OFFSET											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	V_OFFSET	Vertical offset.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	H_OFFSET	Horizontal offset. It should be an even number.	RW

25.2.12 CIM Y Frame buffer Address Register (CIMYFA)

CIMIYFA **0x13060038**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	YFPA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	YFPA	Y Frame buffer physical address in external memory when CIMCFG. SEP is 1. When starts CIM, DMA transfers data from Y_RXFIFO to frame buffer. This address is increased by hardware automatically. Bits [6:0] must be zero to be aligned to 32-word boundary.	R

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25.2.13 CIM Y DMA Command Register (CIMYCMD)

CIMYCMD 0x1306003C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOFINT	EOFINT	EEOFINTEn	STOP	Reserved				YLEN																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SOFINTEn	Interrupt enable for DMA starting a frame-buffer transfer. 1: DMA will set CIMSTATE.DMA_SOF when start of a frame-buffer transfer When one frame uses several buffers, it is suggested to set SOFINTEn of first buffer only.	R
30	EOFINTEn	Interrupt enable for DMA ending a frame-buffer transfer. 1: DMA will set CIMSTATE.DMA_EOF when CIMYCMD.YLEN and CIMCbCMD.CbLEN and CIMCrCMD.CrLEN are decreased to 0, which means end of a frame-buffer transfer When one frame uses several buffers, it is suggested to set EOFINTEn of last buffer only.	R
29	EEOFINTEn	Interrupt enable for DMA issuing an earlier eof interrupt.	R
28	STOP	DMA stop. When DMA complete transferring data, STOP bit decides whether DMA should loading next descriptor or not. 0: DMA start loading next descriptor 1: DMA stopped, and CIMSTATE.DMA_STOP bit is set 1 by hardware	R
27	OFRCVEN	Auto recovery enable when there is RXFIFO overflow. 0: No auto recovery when overflow occurs, thus the software should do something 1: Auto recovery enable, the hardware will correct the overflow DMA will do a frame synchronization, and retransfer the current descriptor.	
26:24	Reserved	Writing has no effect, read as zero.	R
23:0	YLEN	Length of transfer in words. Indicate the number of words to be transferred by DMA to a frame buffer. YLEN = 0 is not valid. DMA transfers data according to YLEN. Each time one or more word(s) been transferred, YLEN is decreased automatically.	R

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25.2.14 CIM Cb Frame buffer Address Register (CIMCBFA)

CIMICBFA 0x13060040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CbFPA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CbFPA	Cb Frame buffer physical address in external memory when CIMCFG.SEP is 1. When starts CIM, DMA transfers data from Cb_RXFIFO to frame buffer. This address is increased by hardware automatically. Bits [6:0] must be zero to be aligned to 32-word boundary.	R

25.2.15 CIM Cb DMA Command Register (CIMCBCMD)

CIMCBCMD 0x13060044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CbLEN																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	CbLEN	Cb Length of transfer in words. Indicate the number of words to be transferred by DMA to a frame buffer. CbLEN = 0 is not valid. DMA transfers data according to CbLEN. Each time one or more word(s) been transferred, CbLEN is decreased automatically.	R

25.2.16 CIM Cr Frame buffer Address Register (CIMCRFA)

CIMICRFA 0x13060048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CrFPA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CrFPA	Cr Frame buffer physical address in external memory when CIMCFG.SEP is 1. When starts CIM, DMA transfers data from Cr RXFIFO to frame buffer. This address is increased by hardware automatically. Bits [6:0] must be zero to be aligned to 32-word boundary.	R

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25.2.17 CIM DMA Cr Command Register (CIMCRCMD)

CIMFID 0x1306004C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CrLEN																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	CrLEN	Cr Length of transfer in words. Indicate the number of words to be transferred by DMA to a frame buffer. CrLEN = 0 is not valid. DMA transfers data according to CrLEN. Each time one or more word(s) been transferred, CrLEN is decreased automatically.	R

25.3 CIM Data Sampling Modes

CIM module supports several types of data sampling mode. The modes and the corresponding signals used are shown in the following diagram:

Table 25-3 The modes and the corresponding signals used

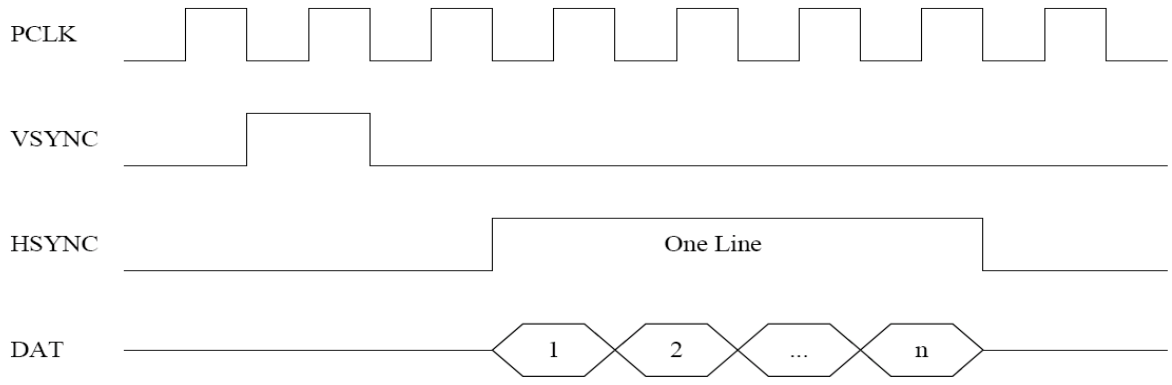
Mode \ Signals	CIM_VSYNC	CIM_HSYNC	CIM_PCLK	CIM_DATA
Gated Clock Mode	Y	Y	Y	Y
ITU656 Interlace Mode	N	N	Y	Y
ITU656 Progressive Mode	N	N	Y	Y

25.3.1 Gated Clock Mode

CIM_VSYNC, CIM_HSYNC, and CIM_PCLK signals are used in this mode.

A frame starts with VSYNC leading edge, then HSYNC goes active and holds the entire line. Data is sampled at the valid edge of PCLK when HSYNC is active; That means, HSYNC functions like “data enable” signal. Please refer to the figure below.

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Gated Clock Input Timing

The VSYNC leading edge, HSYNC active HIGH or LOW, PCLK valid edges are programmable.

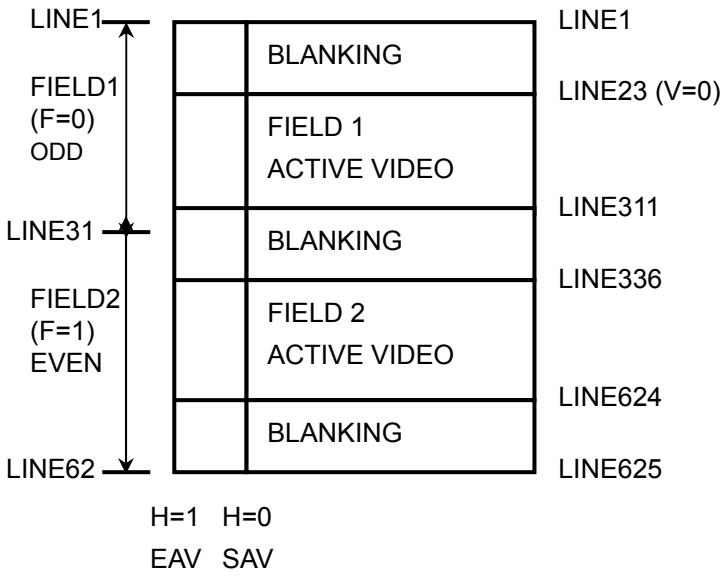
25.3.2 ITU656 Interlace Mode

In this mode, CIM_PCLK and CIM_DAT signals are used, CIM_VSYNC, CIM_HSYNC signals are ignored.

CIM utilizes the SAV & EAV code within ITU656data stream to get active video data.

The following diagrams and tables are quoted from ITU656standard. For more information about ITU656, please refer to ITU656 standard.

25.3.2.1 PAL Timing



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LINE NUMBER	F	V	H (EAV)	H (SAV)	P0, P1, P2, P3
1-22	0 Field 1	1: blanking	1: in EAV, to indicate the end of active video	0: in SAV, to indicate the start of active video	Protection bits
23-310		0: video data			
311-312		1: blanking			
313-335	1 Field 2	1: blanking			
336-623		0: video data			
624-625		1: blanking			

Figure 25-1 Typical BT.656 Vertical Blanking Intervals for 625/50 Video Systems

25.3.2.2 Coding for Protection Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

25.3.3 ITU656 Progressive Mode

CIM_PCLK and CIM_DAT signals are used in this mode. CIM_HSYNC signal is ignored.

CIM_VSYNC is optional in this mode. When the start of frame information is retrieved from SAV and EAV, it is known as internal VSYNC mode. When CIM_VSYNC is provided by sensor directly, it is known as external VSYNC mode. CIM supports both internal and external VSYNC modes.

ITU656Progressive Mode is a kind of Non-Interlace Mode. The image data are encoded within only one field. Most sensors support ITU656Progressive Mode.

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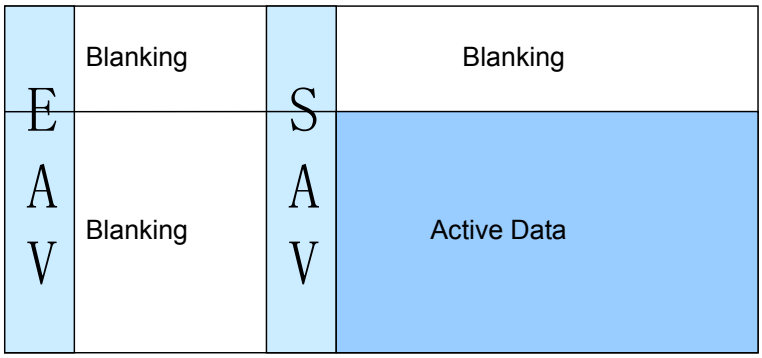


Figure 25-2 ITU656 Progressive Mode

25.4 DMA Descriptors

25.4.1 4-Word Descriptor

Used when output is packaged frame format.

A DMA descriptor is a 4-word block corresponding to the four DMA registers – CIMDA, CIMFA, CIMFID, and CIMCMD, aligned on 4-word (16-byte) boundary, in external memory:

word [0] contains the physical address for next CIMDA
word [1] contains the value for CIMFID
word [2] contains the physical address for CIMFA
word [3] contains the value for CIMCMD

Software must write the physical address of the first descriptor to CIMDA before enabling the CIM. Once the CIM is enabled, the first descriptor is read, and all 4 registers are written by the DMAC. The next DMA descriptor pointed to by CIMDA is loaded into the registers after all data for the current descriptor has been transferred.

25.4.2 8-Word Descriptor

Used when output is separated frame format.

A DMA descriptor is a 8-word block corresponding to the four DMA registers – CIMDA, CIMFA, CIMFID, and CIMCMD, aligned on 8-word (32-byte) boundary, in external memory:

word [0] contains the physical address for next CIMDA
word [1] contains the value for CIMFID
word [2] contains the physical address for CIMYFA
word [3] contains the value for CIMYCMD

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word [4] contains the physical address for CIMCBFA
word [5] contains the value for CIMCBCMD
word [6] contains the physical address for CIMCRFA
word [7] contains the value for CIMCRCMD

Software must write the physical address of the first descriptor to CIMDA before enabling the CIM. Once the CIM is enabled, the first descriptor is read, and all 8 registers are written by the DMAC. The next DMA descriptor pointed to by CIMDA is loaded into the registers after all data for the current descriptor has been transferred.

NOTE: If only one frame buffer is used in external memory, the CIMDA field (word [0] of the DMA descriptor) must point back to itself. That is to say, the value of CIMDA is the physical address of itself.

25.5 Interrupt Generation

CIM has next interrupt sources:

Step 1. RXFIFO FULL Interrupt. (RF_TRIG)
When the valid data number of RXFIFO reaches trigger value, CIMST.RF_TRIG bit is set. At the same time, if RF_TRIGM is 1, RF_TRIG interrupt is generated.

Step 2. RXFIFO Over Flow Interrupt. (RF_OF)
When the valid data number of RXFIFO reaches 32 and one more data are written to RXFIFO, CIMST.RF_OF bit is set. At the same time, if RF_OFM is 1, RF_OF interrupt is generated.

Step 3. DMA Start Of Frame Data Transferring Interrupt. (DMA_SOF)
When the CIMCMD.SOFINT bit is 1 and DMA start transferring the first data from RXFIFO to frame buffer, CIMST.DMA_SOF bit is set. At the same time, if DMA_SOFM is 1, DMA_SOF interrupt is generated.

Step 4. DMA End Of Frame Data Transferring Interrupt. (DMA_EOF)
When the CIMCMD.EOFINT bit is 1 and DMA complete transferring the last data from RXFIFO to frame buffer, CIMST.DMA_EOF bit is set. At the same time, if DMA_EOFM is 1, DMA_EOF interrupt is generated.

Step 5. DMA Stop Transferring Interrupt. (DMA_STOP)
When the CIMCMD.STOP bit is 1 and DMA complete transferring the last data from RXFIFO to frame buffer, CIMST.DMA_STOP bit is set. At the same time, if DMA_STOPM is 1, DMA_STOP interrupt is generated.

Step 6. CIM Disable Done Interrupt. (VDD)

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When disable the module by clearing the CIMCR.ENA, the module should be disabled after transferring current valid data. Then set the CIMST.VDD bit, at the same time, if VDDM is set, VDD interrupt is generated.

25.6 Software Operation

25.6.1 Enable CIM with DMA

Step 1. Configure register CIMCFG.
Step 2. Prepare frame buffer and descriptors.
Step 3. Configure register CIMDA.
Step 4. Clear state register: write 0 to register CIMSTATE.
Step 5. Reset RXFIFO: configure register CIMCTRL with DMA_EN=1, RXF_RST=1, ENA=0.
Step 6. Stop resetting RXFIFO: configure register CIMCTRL with DMA_EN=1, RXF_RST=0, ENA=0.
Step 7. Enable CIM: configure register CIMCTRL with DMA_EN=1, RXF_RST=0, ENA=1.

25.6.2 Enable CIM without DMA

1 Configure register CIMCFG.
2 Clear state register: write 0 to register CIMSTATE.
3 Reset RXFIFO: configure register CIMCTRL with DMA_EN=0, RXF_RST=1, ENA=0.
4 Stop resetting RXFIFO: configure register CIMCTRL with DMA_EN=0, RXF_RST=0, ENA=0.
5 Enable CIM: configure register CIMCTRL with DMA_EN=0, RXF_RST=0, ENA=1.

25.6.3 Disable CIM

Method 1:

Step 1. Configure register CIMCTRL with RXF_RST=0, ENA=0. // quick disable
Step 2. Clear state register: write 0 to register CIMSTATE.

Method 2:

When DMA is enabled, the following sequence is recommended:

Step 1. Configure descriptor with STOP = 1.
Step 2. Wait DMA_STOP interrupt, then write 0 to CIMCTRL.ENA.
Step 3. Clear state register: write 0 to register CIMSTATE.

25.6.4 CIM Priority

There are three methods to use CIM priority to transfer data from receiving fifo to external memory, called bus, module and software mode.

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25.6.4.1 Bus Priority Mode

CIM uses the priority distributed by AHB bus arbiter.

Step:

Set CIMCR2.APM to 1'b0.

25.6.4.2 Module Priority Mode

CIM module chooses the priority automatically, which is according to the receiving fifo status only. It is recommended. It is recommended.

Steps:

1 Set CIMCR2.OPE to 1'b0.

2 Set CIMCR2.APM to 1'b1.

25.6.4.3 Software Priority Mode

CIM module chooses the priority according to the receiving fifo status and CIMCR2.OR.

Steps:

1 Set CIMCR2.OP to the value expected.

2 Set CIMCR2.OPE to 1'b1.

3 Set CIMCR2.APM to 1'b1.

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26 Internal CODEC Interface

26.1 Overview

This chapter describes the embedded audio CODEC in the processor and related software interface.

This embedded CODEC is an I2S audio CODEC. AIC module is an interface to this CODEC in audio data replaying and recording. Several memory mapped registers are used to access this embedded CODEC, and write/read these registers could access the CODEC's internal control and configure registers that is using 12 MHz clock.

26.1.1 Features

The following are internal CODEC features:

- 24 bits ADC and DAC
- Headphone load up to 16 Ohm
- Sample frequency supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, and 96k
- Stereo line input
- DAC to HP path: Power consumption: 6.5mW, THD: 0.06% @13.9mW/16Ohm
- DAC to stereo line output path @10kOhm: SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
- Line input to ADC path: SNR: 90dB A-Weighted, THD: -80dB @FS-1dB
- Separate power-down modes for ADC and DAC path with several shutdown modes
- Reduction of audible glitches systems: Pop Reduction system, Soft Mute mode
- Output short circuit protection

TBD = parameter or document section to be defined later on
TBC = parameter or document section subject to change
TO BE COMPLETED = section to be filled or subject to change

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26.1.2 Signal Descriptions

CODEC has max 13 analog signal IO pins and 4 power pins on chip. They are listed and described in the flowing table.

Table 26-1 CODEC signal IO pin description

Pin Names	IO	Pin Description	Power
MICP1	AI	Microphone mono differential analog input 1 (MIC1), positive pin.	AVDCDC
MICN1	AI	Microphone mono differential analog input 1 (MIC1), negative pin.	AVDCDC
MICP2	AI	Microphone mono differential analog input 2 (MIC2), positive pin.	AVDCDC
MICN2	AI	Microphone mono differential analog input 2 (MIC2), negative pin.	AVDCDC
MICBIAS	AO	Microphone bias.	AVDCDC
AIL	AI	Left line single-ended analog input.	AVDCDC
AIR	AI	Right line single-ended analog input.	AVDCDC
AOLP	AO	Differential line output, positive pin.	AVDCDC
AOLN	AO	Differential line output, negative pin.	AVDCDC
AOHPL	AO	Left headphone single ended analog output.	AVDHP
AOHPR	AO	Right headphone single ended analog output.	AVDHP
AOHPM	AO	Headphone common mode output.	AVDHP
AOHPMS	AI	Headphone common mode sense input.	AVDHP
VCAP	AO	Voltage Reference Output. An 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVDCDC
AVDHP	P	Headphone amplifier power, 2.5V.	-
AVSHP	P	Headphone amplifier ground.	-
AVDCDC	P	CODEC analog power, 2.5V, inter signal VREFP.	-
AVSCDC	P	CODEC analog ground, inter signal VREFN.	-
HPSENSE	AI	Headphone jack sense.	AVDHP
DMIC_IN	DI	Digital microphone data input pin.	AVDCDC
DMIC_CLK	DO	Digital microphone clock output pin.	AVDCDC

NOTES:

1 AVDHP = 2.5v (typ). AVDCDC= 2.5v (typ).

2 Inter signal VREFP is connected to AVDCDC, inter signal VREFN is connected to AVSCDC.

3 Please refer to data sheet of the chip for details.

4 DMIC_IN is GPIO : PB18 , MIC_CLK is GPIO : PB19. Please refer to GPIO specification for these pins operating.

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26.1.3 Block Diagram

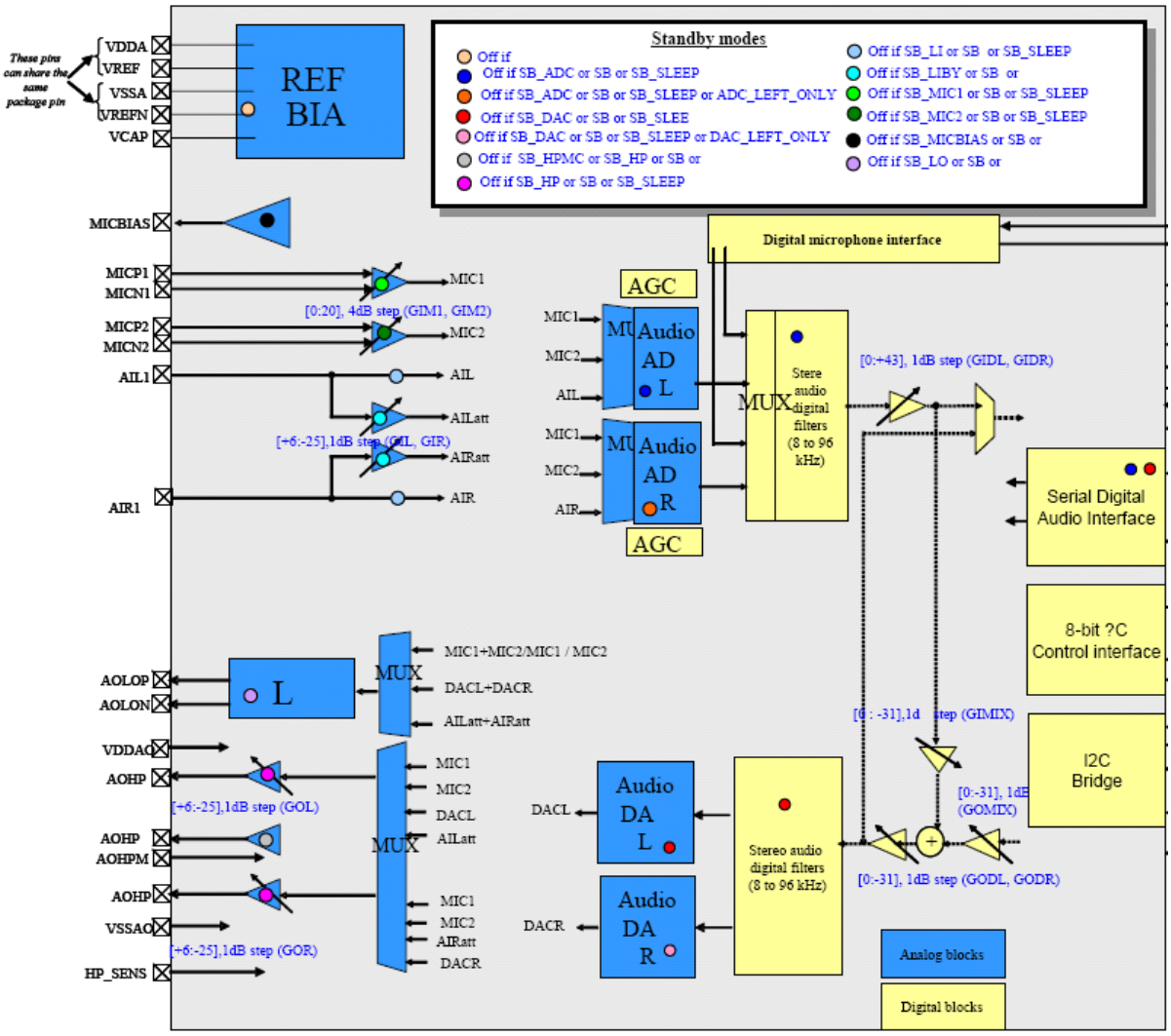


Figure 26-1 CODEC block diagram

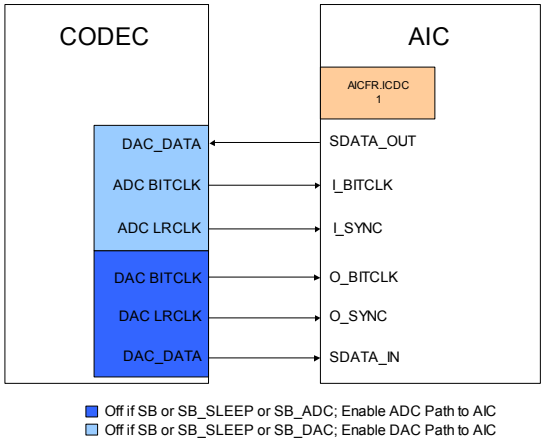


Figure 26-2 Internal CODEC works with AIC

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26.2 Mapped Register Descriptions

The internal CODEC software interface includes 2 registers. They are mapped in IO memory address space of AIC module so that program can access them to control the operations of the CODEC.

Table 26-2 Internal CODEC Mapped Registers Description (AIC Registers)

Name	Description	RW	Reset value	Address	Size
RGADW	Address, data in and write command for accessing to internal registers of internal embedded CODEC.	RW	0x00000000	0x100200A4	32
RGDATA	The read out data and interrupt request status of Internal registers data in the internal embedded CODEC.	R	0x00000000	0x100200A8	32

NOTES:

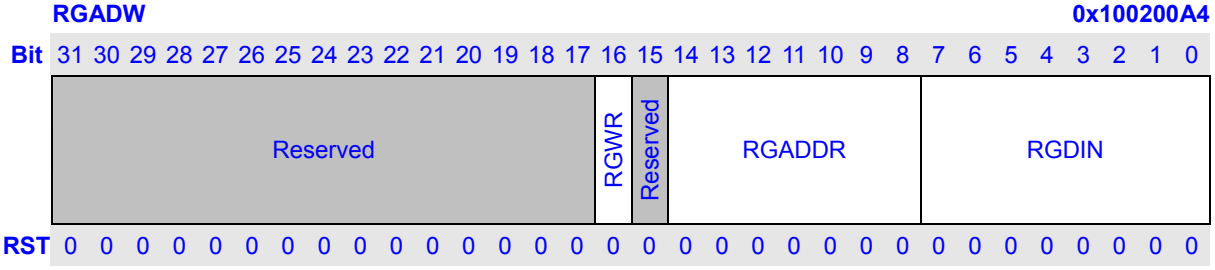
1 All these registers are AIC Registers, because they are mapped in AIC IO memory address.

2 RGADW contains data, address and write command to the internal registers of the internal CODEC.

3 RGDATA returns the internal register value of the internal CODEC and interrupt request status.

26.2.1 CODEC internal register access control (RGADW)

RGADW contains address, data and write command to the internal registers of the internal embedded CODEC.



Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	RGWR	Write 1 to this bit issues writing to CODEC's internal register process. This bit keeps value 1 until the current writing process is finished. A register read or a new register writing process cannot be issued before the previous writing process finished. In another word, it should not write to RGADW before RGADW.RGWR becomes 0. A writing process takes max of 0.17us plus 1 PCLK cycle. Write 0 to this bit is ignored.	RW

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15	Reserved	Writing has no effect, read as zero.	R
14:8	RGADDR	When it issues a writing to CODEC's internal register command, i.e. RGWR=1, this field specifies the register's address. In addition, this field also decides the address of the register's data out at any time.	RW
7:0	RGDIN	When it issues a writing to CODEC's internal register command, i.e. RGWR=1, this field contains the data to be written to the register.	RW

NOTES:

1 It is strong suggesting verifying the data (using read RGDATA below) after writing it to internal register of CODEC. When RGDATA returns the right data which writing to the address, the writing process is finish.

2 Please notice that AIC needs SYS_CLK (refers to AIC spec), when write new value to or read from CODEC internal registers.

26.2.2 CODEC internal register data output (RGDATA)

RGDATA returns the internal register value of the internal embedded CODEC and interrupt request status.

RGDATA **0x100200A8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							IRQ	RGDOUT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zero.	R
8	IRQ	This field returns the internal embedded CODEC's interrupt request. IRQ: 0 — No CODEC's interrupt request found. IRQ: 1 — CODEC's interrupt request is pending.	R
7:0	RGDOUT	This field returns the value of the internal register in internal embedded CODEC. As the RGADW.RGADDR field specifies the register's address.	R

NOTE: AIC needs SYS_CLK (refers to AIC spec), when write new value to or read from CODEC internal registers.

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26.3 Operation

The internal embedded CODEC is controlled its internal registers. These registers can be accessed by through memory-mapped registers, RGADW and RGDATA, just like L3 bus or I2C bus for an external CODEC. AIC's BITCLK and SYNC are from/to the CODEC and is controlled by CKCFG.SELAD register. The audio data transferring, i.e. audio replaying and recording, is down by AIC. AIC still takes the role of I2S controller. We will refer to many AIC operations and registers in the following audio operation descriptions, please reference to AIC spec for the details.

This is a guide for software.

26.3.1 Access to internal registers of the embedded CODEC

The embedded CODEC is controlled through its internal registers. RGADW and RGDATA are used to write to and read from these registers. Here are some examples.

Example 1. Write to a CODEC internal register.

Step 1: RGADW.RGWR == 0.

Step 2: If not, go to step 1.

Step 3: Write to RGADW and make it.

RGADW.RGDIN = <data to be written to the register>.

RGADW.RGADDR = <the register's address >.

Step 4: Write to RGADW to commit the writing operation.

RGADW.RGWR = 1.

Example 2. Read from a CODEC internal register.

Step 1: RGADW.RGWR == 0.

Step 2: If not, go to step 1.

Step 3: write to RGADW and make it.

RGADW.RGWR = 0.

RGADW.RGDIN = <don't care>.

RGADW.RGADDR = <the register's address>.

Step 4: read RGDATA.DOUT, which returns the register's content.

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26.3.2 CODEC controlling and typical operations

This section is some typical operations. We are assumed the power supply of CODEC is on, and CODEC is in STANDBY mode, CRR is configured for audio Ramping system.

Before using any of these operations, make sure AIC is configured properly as list below:

1 Make AIC to use internal CODEC mode:
  AICFR.ICDC = 1; Use internal CODEC.
  AICFR.AUSEL = 1; Use I2S mode.
  AICFR.BCKD = 0; CODEC input BIT_CLK to AIC.
  AICFR.SYNCD = 0; CODEC input SYNC to AIC.
  I2SCR.AMSL = 1; Use I2S operation mode.
  I2SCR.ESCLK = 1; Open SYS_CLK to internal CODEC.(if using PLL Clock)
2 Make sure AICCR.FLUSH = 0; AICFR.RST = 0; AICCR.ENLBF = 0.
3 Clear AICSR.ROR, AICSR.TUR, AICSR.RFS, AICSR.TFS = 0 to 0.
4 Set proper value to AICCR.M2S; AICCR.ENDSW; AICCR.ASVTSU.
5 Set AICFR.ENB to 1; Open AIC.

When using DMA mode, configure AICFR.RFTH, AICCR.RDMS or AICFR.TFTH, AICCR.TDMS.
Configure TX-FIFO and interrupt means setting proper value to AICFR.TFTH, clear AICCR.ETFS to 0, and clear AICCR.ETUR to 0.
Configure RX-FIFO and interrupt means setting proper value to AICFR.RFTH, clear AICCR.ERFS to 0 and clear AICCR.EROR to 0.
When configure interrupt, software must handle all the interrupt. So all interrupt is recommended disabled as shown above.
CODEC shares the interrupt with AIC module.

The register or register bit of CODEC will use the same form as the Mapped registers, but software should use the method in the section "Mapped Register Descriptions" to access this registers.

More details are listed in the CODEC guide.

26.3.3 Power saving

There are many power modes in CODEC. In every working mode, it should close stages (parts) of CODEC for saving power.

The power diagram is shown in "CODEC Power Diagram"; please refer to "CODEC Operating modes".

26.3.4 Pop noise and the reduction of it

Please refre to "Ramping system note" and "Anti-pop operation sequences" for details.

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26.3.4.1 Reference open step

1 Init play.

Step 0: Open DMA and two AIC modules Clocks in CPM.CLKGR.

Step 1: Configure AIC as slave and using inter CODEC mode.

AICFR.ICDC = 1; Use internal CODEC.

AICFR.AUSEL = 1; Use I2S mode.

AICFR.BCKD = 0; CODEC input BIT_CLK to AIC.

AICFR.SYNCD = 0; CODEC input SYNC to AIC.

I2SCR.AMSL = 1; Use I2S operation mode.

I2SCR.ESCLK = 1; Open SYS_CLK to internal CODEC.

Step 2: Configure DMA as slave mode using internal CODEC.

2 Open.

Step 0: Enable DMA Channel Clock.

Step 1: Configure AIC sample size and sample rate. Configure AIC Output FIFO Threshold.

Step 2: Configure DMA.

Step 3: Configure CODEC.

3 Write.

Step 0: Enable DMA Channel Clock.

Step 1: Configure AIC.

Step 2: Configure DMA.

Step 3: Configure CODEC.

4 Read.

Step 0: Enable DMA Channel Clock.

Step 1: Configure AIC.

Step 2: Configure DMA.

Step 3: Configure CODEC.

5 Close.

6 End.

NOTES:

1 SB_DAC Control the internal OBIT_CLK from CODEC to AIC, First turn it on when write data (replay).

2 SB_ADC Control the internal IBIT_CLK from CODEC to AIC, First turns it on when read data (record).

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26.4 Timing parameters

Parameter	Condition	Min.	Typ.	Max.	Unit
Tsbyu	Cext = 10uF/100nF +/-20%		250	500	ms
Tshd_adc	Cext = 10uF/100nF +/-20%		200		ms
Tshd_dac	Cext = 10uF/100nF +/-20%		400	900	ms
Tr, Tf (all inputs)	All modes			5	ns
Tr, Tf (all outputs)	All modes			5	ns

NOTES:

1 Tsbyu is the reference wake-up time after complete power down.

2 Tshd_adc is the ADC wake-up time after sleep mode.

3 Tshd_dac is DAC wake-up time after sleep mode.

26.5 AC & DC parameters

Voltages:

AVSHP and AVSCDC are connected to analog ground.

AVDHP = 2.5v (typ).

AVDCDC= 2.5v (typ).

Currents:

Mode	Currents
1 Complete down (Static)	$I_{AVDCDC} + I_{AVDHP} < 5\mu A$ (TBC)
2 SLEEP mode (Static)	TBD
3 SLEEP mode with SYS_CLK(Static)	TBD
4 Playback to AOHPR/AOHPL(Silence)	$2\ mA < I_{AVDCDC} + I_{AVDHP} < 8\ mA$
5 Record from AIL/AIR(Silence)	$1.5\ mA < I_{AVDCDC} + I_{AVDHP} < 6\ mA$
6 Playback with Record (4 + 5 Silence)	$3\ mA < I_{AVDCDC} + I_{AVDHP} < 10\ mA$
7 Playback to AOHPR/AOHPL(Digital Full Scale)	TBD
8 Record from AIL/AIR(2.8Vpp)	TBD
9 Playback with Record (7 + 8 Full Scale)	TBD

Current value is at AVDCDC = AVDHP = 3.3 V.

Chip pin Name	MAX Current across I/O @ AVDCDC = AVDHP = 3.3 V
AVDCDC	< 20 mA in normal working mode
AVSCDC	< 20 mA in normal working mode

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AVDHP	< 160 mA in normal working mode
	< 1400 mA in case of short circuit
AVSHP	< 160 mA in normal working mode
	< 1400 mA in case of short circuit
VCAP	< 2 mA in normal working mode
MICP1, MICN1	< 2 mA in normal working mode
MICP2, MICN2	< 2 mA in normal working mode
MICBIAS	< 5 mA in normal working mode
AOHPL	< 80 mA in normal working mode
	< 1200 mA in case of short circuit
AOHPR	< 80 mA in normal working mode
	< 1200 mA in case of short circuit
AOHPM	< 80 mA in normal working mode
	< 1200 mA in case of short circuit
AOHPMS	< 1 mA in normal working mode
AIL, AIR	< 2 mA in normal working mode
AOLP, AOLN	< 1 mA in normal working mode
HPSENSE	< 1 mA in normal working mode

The current in case of short circuit is the max value. This current is only sink or drawn until the short circuit detection system acts.

Please refer to Chip Datasheet for more details.

26.6 CODEC internal Registers

Register Name	Function	Address	Reset value
SR	Status Register	000000 / 0x0 / 00	h00
AICR_DAC	DAC Audio Interface Control Register	000001 / 0x1 / 01	hC3
AICR_ADC	ADC Audio Interface Control Register	000010 / 0x2 / 02	hC3
CR_LO	differential line-out Control Register	000011 / 0x3 / 03	h90
CR_HP	HeadPhone Control Register	000100 / 0x4 / 04	h98
CR_DAC	DAC Control Register	000110 / 0x6 / 06	h90
CR_MIC	Microphone Control Register	000111 / 0x7 / 07	hB1
CR_LI	Control Register for line inputs	001000 / 0x8 / 08	h11
CR_ADC	ADC Control Register	001001 / 0x9 / 09	h10
CR_MIX	Control Register for digital mixer	001010 / 0xA / 10	h00
CR_VIC	Control Register for the codec	001011 / 0xB / 11	h03
CCR	Clock Control Register	001100 / 0xC / 12	h00
FCR_DAC	DAC Frequency Control Register	001101 / 0xD / 13	h00
FCR_ADC	ADC Frequency Control Register	001110 / 0xE /14	h40
ICR	Interrupt Control Register	001111 / 0xF / 15	h00

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IMR	Interrupt Mask Register	010000 / 0x10 / 16	hFF
IFR	Interrupt Flag Register	010001 / 0x11 / 17	h00
GCR_HPL	left channel headphone Control Gain Register	010010 / 0x12 / 18	h06
GCR_HPR	right channel headphone Control Gain Register	010011 / 0x13 / 19	h06
GCR_LIBYL	left channel bypass line Control Gain Register	010100 / 0x14 / 20	h06
GCR_LIBYR	right channel bypass line Control Gain Register	010101 / 0x15 / 21	h06
GCR_DACL	Left channel DAC Gain Control Register	010110 / 0x16 / 22	h00
GCR_DACR	right channel DAC Gain Control Register	010111 / 0x17 / 23	h00
GCR_MIC1	Microphone 1 Gain Control Register	011000 / 0x18 / 24	h00
GCR_MIC2	Microphone 2 Gain Control Register	011001 / 0x19 / 25	h00
GCR_ADCL	Left ADC Gain Control Register	011010 / 0x1A / 26	h00
GCR_ADCR	Right ADC Gain Control Register	011011 / 0x1B / 27	h00
GCR_MIXADC	ADC Digital Mixer Control Register	011101 / 0x1D / 29	h00
GCR_MIXDAC	DAC Digital Mixer Control Register	011110 / 0x1E / 30	h00
AGC1	Automatic Gain Control 1	011111 / 0x1F / 31	h34
AGC2	Automatic Gain Control 2	100000 / 0x20 / 32	h07
AGC3	Automatic Gain Control 3	100001 / 0x21 / 33	h44
AGC4	Automatic Gain Control 4	100010 / 0x22 / 34	h1F
AGC5	Automatic Gain Control 5	100011 / 0x23 / 35	h00

26.6.1 CODEC internal registers

26.6.1.1 SR: Status Register

Register Name: SR Register Address: 0x0

bit7-R-0	bit6-R-0	bit5-R-0	bit4-R-0	Bit3-R-0	bit2-R-0	bit1-R-0	bit0-R-0
PON_ACK	IRQ_ACK	JACK	Reserved				

Bits	Field	Description
7	PON_ACK	Acknowledge status bit after power on. Read 0 = reset value Read 1 = codec is ready to operate
6	IRQ_ACK	Acknowledge status bit after IRQ sending. Read 0 = reset value Read 1 = codec has requested an interrupt (IRQ signal activated)

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5	JACK	Output Jack plug detection status. Read 0 = no jack Read 1 = output jack present

26.6.1.2 AICR_DAC: Audio Interface Control Register

Register Name: AICR_DAC Register Address: 0x1

bit7-RW-1	bit6-RW-1	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-1	bit0-RW-1
DAC_ADWL		-	-	-	-	DAC_SERIAL	DAC_I2S

Bits	Field	Description
7-6	DAC_ADWL	Audio Data Word Length: for respectively DAC and ADC paths. Read / Write 00: 16-bit word length data 01: 18-bit word length data 10: 20-bit word length data 11: 24-bit word length data
1	DAC_SERIAL	Selection of DAC digital serial audio interface. Read / Write 0: Parallel interface 1: Serial interface
0	DAC_I2S	Working mode of DAC serial mode. (only relevant when serial interface is selected) Read/Write 0: DSP mode; 1: I2S mode.

NOTES:

1 DAC_SERIAL should be configured to 1.

2 DAC_I2S should be configured to 1.

26.6.1.3 AICR_ADC: Audio Interface Control Register

Register Name: AICR_ADC Register Address: 0x2

bit7-RW-1	bit6-RW-1	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-1	bit0-RW-1
ADC_ADWL		-	-	-	-	ADC_SERIAL	ADC_I2S

Bits	Field	Description
7-4	ADC_ADWL	Audio Data Word Length: for respectively DAC and ADC paths. Read / Write 00: 16-bit word length data 01: 18-bit word length data

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		10: 20-bit word length data 11: 24-bit word length data
1	ADC_SERIAL	Selection of the ADC digital serial audio interface. Read / Write 0: Parallel interface 1: Serial interface
0	ADC_I2S	Working mode of the ADC digital serial audio interface. (only relevant when serial interface is selected) Read/Write 0: DSP mode 1: I2S mode

NOTES:

1 ADC_SERIAL should be configured to 1.

2 ADC_I2S should be configured to 1.

26.6.1.4 CR_LO: differential line-out Control Register

Register Name: CR_LO Register Address: 0x3

bit7-RW-1	bit6-RW-0	Bit5-RW-0	bit4-RW-1	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
LO_MUTE	-	-	SB_LO	-	-	LO_SEL	

Bits	Field	Description
7	LO_MUTE	differential line output mute mode. Read/Write 0: mute inactive, Signal applied to line output 1: no signal on line output
4	SB_LO	differential line out conditioning circuitry power-down mode. Read/Write 0: active 1: power-down
1-0	LO_SEL	differential line-output Amplifier input selection. Read/Write If MICSTEREO = 0 00 : Microphone 1 enabled 01 : Microphone 2 enabled 10 : Bypass path enabled 11 : DAC output enabled If MICSTEREO = 1 00 : Microphone 1 & 2 enabled 01 : Microphone 1 & 2 enabled 10 : Bypass path enabled 11 : DAC output enabled

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26.6.1.5 CR_HP: HeadPhone Control Register

Register Name: CR_HP Register Address: 0x4

bit7-RW-1	Bit6-RW-0	Bit5-RW-0	Bit4-RW-1	bit3-RW-1	bit2-RW-0	bit1-RW-0	bit0-RW-0
HP_MUTE	LOAD	-	SB_HP	SB_HPCM	-	HP_SEL	

Bits	Field	Description
7	HP_MUTE	HeadPhone output signal disabled. Read/Write 0: Signal applied to headphone outputs 1: no signal on headphone outputs, acts as a mute signal
6	LOAD	Selection of load impedance value for ramp generation. Read/Write 0: 16 Ohm / 220 uF 1: 10 kOhm / 1 uF
4	SB_HP	headphone output stage power-down mode. Read/Write 0: headphone output stage is active 1: power-down
3	SB_HPCM	headphone output stage common mode buffer power-down mode. Read/Write 0: active (capacitor less headphone output configuration) 1: power-down (line output configuration)
1-0	HP_SEL	Headphone Output Amplifier input selection. Read/Write If MICSTEREO = 0 00: Microphone 1 input to left and right channels 01: Microphone 2 input to left and right channels 10: Bypass path enabled 11: DAC output enabled If MICSTEREO = 1 00: Microphone 1 input to left channel and microphone 2 input to right channel 01: Microphone 2 input to left channel and microphone 1 input to right channel 10: Bypass path enabled 11: DAC output enabled

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26.6.1.6 CR_DAC: Control Register for DAC 3

Register Name: CR_DAC Register Address: 0x6

bit7-RW-1	bit6-RW-0	bit5-RW-0	Bit4-RW-1	bit3-RW-0	bit2-RW-0	Bit1-RW-0	bit0-RW-0
DAC_MUTE	DAC_MONO	DAC_LEFT_ ONLY	SB_DAC	DAC_ LRSWAP	-	-	-

Bits	Field	Description
7	DAC_MUTE	DAC soft mute mode. Read/Write 0: mute inactive, digital input signal transmitted to the DAC 1: puts the DAC in soft mute mode
6	DAC_MONO	Digital stereo-to-mono conversion for DAC path. Read/Write 0: stereo 1: mono When DAC_MONO=1, the left and right channels are mixed in digital part: the result is emitted on both left and right channel of DAC output. It corresponds to the average of left and right channels when DAC_MONO=0.
5	DAC_LEFT_ONLY	Left data only are considered. Read/Write 0: DAC right channel active 1: DAC left data are used for left and right channel To avoid any audible pop, it is required to put the DAC in soft mute mode before modifying the DAC_LEFT_ONLY bit.
4	SB_DAC	DAC power-down mode. Read/Write 0: active 1: power-down
3	DAC_LRSWAP	swap between Left an d right channels. Read/Write 0: left data are sent to right channel, right data to left channel (swap) 1: left data are sent to left channel, right data to left channel (do not swap)

NOTE: DAC_LRSWAP should be configured to 1.

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26.6.1.7 CR_MIC: Control Register for microphone inputs

Register Name: CR_MIC Register Address: 0x7

bit7-RW-1	bit6-RW-0	bit5-RW-1	Bit4-RW-1	bit3-RW-0	bit2-RW-0	Bit1-RW-0	bit0-RW-1
MIC_STEREO	MICIDFF	SB_MIC2	SB_MIC1	-	-	MICBIAS_V0	SB_MICBIAS

Bits	Field	Description
7	MIC_STEREO	Microphone input mode selection. Read/Write 0: Microphone mono inputs 1: Microphone stereo inputs This signal affects IN_SEL, HP_SEL, LO_SEL. Refer to its description.
6	MICIDFF	Microphone input mode selection. Read/Write 0:Microphone single-ended inputs 1: Microphone differential inputs
5	SB_MIC2	Analog MIC2 Input conditioning circuitry power-down mode. Read/Write 0: active 1: power-down
4	SB_MIC1	Analog MIC1 Input conditioning circuitry power-down mode. Read/Write 0: active 1: power-down
1	MICBIAS_V0	B-port MICBIAS stage output voltage in operating mode. Read/Write 0: 5/6*VREF output voltage 1: 4/6*VREF output voltage
0	SB_MICBIAS	Microphone biasing buffer power-down. Read/Write 0: active 1: power-down

26.6.1.8 CR_LI: Control Register for line inputs

Register Name: CR_LI Register Address: 0x8

bit7-RW-0	bit6-RW-0	bit5-RW-0	Bit4-RW-1	bit3-RW-0	bit2-RW-0	Bit1-RW-0	bit0-RW-1
-	-	-	SB_LIBY	-	-	-	SB_LIN

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Bits	Field	Description
4	SB_LIBY	Linein used for bypass path power-down. Read/Write 0: active 1: power-down
0	SB_LIN	Linein used to ADC power-down. Read/Write 0: active 1: power-down

26.6.1.9 CR_ADC: Control Register for ADC

Register Name: CR_ADC Register Address: 0x9

bit7-RW-0	bit6-RW-0	bit5-RW-0	Bit4-RW-1	bit3-RW-0	bit2-RW-0	Bit1-RW-0	bit0-RW-0
DMIC_SEL	ADC_MONO	ADC_LEFT_ ONLY	SB_ADC	ADC_LRSWAP	-	IN_SEL1	

Bits	Field	Description
7	DMIC_SEL	digital filter input selection. Read/Write 0: ADC 1: Digital microphone
6	ADC_MONO	Digital stereo-to-mono conversion for ADC path. Read/Write 0: stereo 1: mono When ADC_MONO=1, the left and right channels are mixed in digital part: the result is emitted on both left and right channel of ADC digital output. It corresponds to the average of left and right channels when ADC_MONO=0.
5	ADC_LEFT_ONLY	Deactivation of ADC right channel. Read/Write 0: ADC right channel active 1: ADC right channel inactive Note that when ADC right channel is deactivated, left channel is emitted on both left and right channel of ADC digital output.
4	SB_ADC	ADC power down mode. Read/Write 0: active 1: power-down
3	ADC_LRSWAP	swap between Left an d right channels.

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		Read/Write 0: left data are sent to right channel, right data to left channel (swap) 1: left data are sent to left channel, right data to right channel (do not swap)
1-0	IN_SEL	selection of the signal converted by the ADC. Read/Write If MICSTEREO = 0 00: Microphone 1 input to left and right channels (codec automatically considers that ADC_LEFT_ONLY equals '1' to optimize power consumption) 01: Microphone 2 input to left and right channels (codec automatically considers that ADC_LEFT_ONLY equals '1' to optimize power consumption) 10 : Line input 11 : Reserved for further use Note that when digital microphone is selected, the ADC_LEFT_ONLY is not automatically modified. If MICSTEREO = 1 00: Microphone 1 input to left channel and microphone 2 input to right channel 01: Microphone 2 input to left channel and microphone 1 input to right channel 10 : Line input 11 : Reserved for test

NOTE: ADC_LRSWAP should be configured to 1.

26.6.1.10 CR_MIX: Control Register for digital mixer

Register Name: CR_MIX Register Address: 0xA

bit7-RW-1	bit6-RW-0	bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	Bit1-RW-0	bit0-RW-0
-	-	-	-	MIX_REC		DAC_MIX	

Bits	Field	Description
3-2	MIX_REC	Mixer mode on ADC Path. Read/Write 00: Record input only 01: Record input + DAC 10: Reserved for further use 11: Reserved for further use
1-0	DAC_MIX	Mixer mode on DAC Path. Read/Write 00: Playback DAC only

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		01: Playback DAC + ADC 10: Reserved for further use 11: Reserved for further use

26.6.1.11 CR_VIC: Control Register for the codec

Register Name: CR_VIC Register Address: 0xB

bit7-RW-0	bit6-RW-0	bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	Bit1-RW-1	bit0-RW-1
-	-	-	-	-	-	SB_SLEEP	SB

Bits	Field	Description
1	SB_SLEEP	sleep mode. Read/Write 0: normal mode (active) 1: sleep mode
0	SB	complete power-down mode. Read/Write 0: normal mode (active) 1: complete power-down

26.6.1.12 CCR: Control Clock Register

Register Name: CCR Register Address: 0xC

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
DMIC_CLKON	-	-	-	CRYSTAL			

Bits	Field	Description
7	DMIC_CLKON	Digital microphone clock (DMIC_CLK) enable. Read/Write 0: clock off 1: clock on, clock frequency varies with DMIC_RATE and MCLK
3-0	CRYSTAL	Selection of the SYS_CLK frequency. Read/Write The sampling frequency value is given in the CRYSTAL table.

MCLK	CRYSTAL	DMIC_CLK frequency
12 MHz	0000	3 MHz
13 MHz	0001	3.25 MHz

CRYSTAL	Master Clock Frequency
0000	12 MHz
0001	13 MHz

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			….	Reserved for further use
			1111	Reserved for further use

NOTE: This register should be configured to 0x00 for setting the internal 12Mhz master clock SYS_CLK (default).

26.6.1.13 FCR_DAC: DAC Frequency Control Register

Register Name: FCR_DAC Register Address: 0xD

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	-	DAC_FREQ			

Bits	Field	Description
3-0	DAC_FREQ	Selection of the DAC sampling rate (Fs). Read/Write The sampling frequency value is given in the FREQ table.

NOTE: Please refer to section Sample frequency: FREQ.

26.6.1.14 FCR_ADC: ADC Frequency Control Register

Register Name: FCR_ADC Register Address: 0xE

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	ADC_HPF	-	-	ADC_FREQ			

Bits	Field	Description
6	ADC_HPF	ADC High Pass Filter enable. Read/Write 0: inactive 1: enables the ADC High Pass Filter
3-0	ADC_FREQ	Selection of the ADC sampling rate (Fs). Read/Write The sampling frequency value is given in the FREQ table.

NOTE: Please refer to section Sample frequency: FREQ.

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26.6.1.15 ICR: Interrupt Control Register

Register Name: ICR Register Address: 0xF

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
INT_FORM		-	-	-	-	-	-

Bits	Field	Description
7-6	INT_FORM	Waveform and polarity of the IRQ signal. Read/Write 00: The generated IRQ is a high level 01: The generated IRQ is a low level 10: The generated IRQ is a high level pulse with an 8 SYS_CLK cycles duration 11: The generated IRQ is a low level pulse with an 8 SYS_CLK cycles duration

NOTE: Please refer to section Sample frequency: FREQ.

26.6.1.16 IMR: Interrupt Mask Register

Register Name: IMR Register Address: 0x10

bit7-RW-1	bit6-RW-1	Bit5-RW-1	bit4-RW-1	bit3-RW-1	bit2-RW-1	bit1-RW-1	bit0-RW-1
-	SCLR_MASK	JACK_MASK	SCMC_MASK	RUP_MASK	RDO_MASK	GUP_MASK	GDO_MASK

Bits	Field	Description
6	SCLR_MASK	Mask for the SCLR flag. Read/Write 0: interrupt enabled 1: interrupt masked (no IRQ generation)
5	JACK_MASK	Mask for the JACK_EVENT flag. 0: interrupt enabled 1: interrupt masked (no IRQ generation)
4	SCMC_MASK	Mask for the SCMC flag. 0: interrupt enabled 1: interrupt masked (no IRQ generation)
3	RUP_MASK	Mask for the RUP flag. 0: interrupt enabled 1: interrupt masked (no IRQ generation)
2	RDO_MASK	Mask for the RDO flag. 0: interrupt enabled 1: interrupt masked (no IRQ generation)
1	GUP_MASK	Mask for the GUP flag.

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		0: interrupt enabled 1: interrupt masked (no IRQ generation)
0	GDO_MASK	Mask for the GDO flag. 0: interrupt enabled 1: interrupt masked (no IRQ generation)

NOTES:

1 When an interrupt is masked, the event do not generates any change on the IRQ signal, but the corresponding flag value is set to '1' in the IFR register.

2 When the IRQ signal is active on level, the IRQ signal is set to the inactive level while the bits IFR & (!IMR) equals '0'.

3 When the IRQ signal is a pulse, the IRQ signal is set to the inactive state until a new non-masked event occurs in IFR or until a masked event is unmasked.

4 SYS_CLK must not be stopped in order to propagate IRQ signal.

26.6.1.17 IFR: Interrupt Flag Register

Register Name: IFR Register Address: 0x11

bit7-RW-0	Bit6-R-0	bit5-RW-0	bit4-R-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	SCLR	JACK_EVENT	SCMC	RUP	RDO	GUP	GDO

Bits	Field	Description
6	SCLR	Left or Right Output short circuit detection status. Read 0 : no event 1 : event detected (due to JACK flag change to '0' or '1') Write 1 to Reset of the flag.
5	JACK_EVENT	Event on output Jack plug detection status. Read 0: no event 1: event detected (due to JACK flag change to '0' or '1'). Write 1 to Reset of the flag.
4	SCMC	Common mode buffer output short circuit detection status. Read 0: inactive 1: indicates that a short circuit has been detected by the output stage Write 1 to Update of the flag.
3	RUP	End of output stage ramp up flag. Read 1: the ramp-up sequence is completed (output stage is active). Write 1 to Reset of the flag.
2	RDO	End of output stage ramp down flag.

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		Read 1: the ramp-down sequence is completed (output stage in stand-by mode) Write 1 to Reset of the flag.
1	GUP	End of mute gain up sequence flag. Read 1: the mute sequence is completed; the DAC input signal is transmitted to the DAC path Write 1 to Reset of the flag.
0	GDO	End of mute gain down sequence flag. Read 1: the mute sequence is completed, a 0 DC signal is transmitted to the DAC path Write 1 to Reset of the flag.

NOTES:

1 The flags RUP, RDO, GUP and GDO can be reset after 4 cycles of SYS_CLK.

2 Interpretation of any unspecified point is absolutely up to the designer of analog part, so it is need to pay an attention to using this flags in section "Anti-pop operation sequences".

26.6.1.18 GCR_HPL: left channel headphone Control Gain Register

Register Name: GCR_HPL Register Address: 0x12

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-1	Bit1-RW-1	bit0-RW-0
LRGO	-	-	GOL				

Bits	Field	Description
7	LRGO	HP amplifier gain coupling. Read/Write 0: Left and right channels gains are independent 1: Left and right channels gain track left channel gain
4-0	GOL	Left channel HP amplifier gain programming value.

NOTE: Please refer to section "Programmable attenuation: GO" for more details.

26.6.1.19 GCR_HPR: right channel headphone Control Gain Register

Register Name: GCR_HPR Register Address: 0x13

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-1	Bit1-RW-1	bit0-RW-0
-	-	-	GOR				

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Bits	Field	Description
4-0	GOR	Right channel HP amplifier gain programming value.

NOTE: Please refer to section "Programmable attenuation: GO" for more details.

26.6.1.20 GCR_LIBYL: left channel bypass line Control Gain Register

Register Name: GCR_LIBYL Register Address: 0x14

bit7-RW-0	bit6-RW-0	Bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-1	bit1-RW-1	bit0-RW-0
LRGI	-	-	GIL				

Bits	Field	Description
7	LRGI	analog bypass gain coupling. Read/Write 0: Left and right channels gains are independent 1: Left and right channels gain track left channel gain
4-0	GIL	Left channel Line in gain programming value.

NOTE: Please refer to section "Programmable Bypass path attenuation: GI" for more details.

26.6.1.21 GCR_LIBYR: right channel bypass line Control Gain Register

Register Name: GCR_LIBYR Register Address: 0x15

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-1	bit1-RW-1	bit0-RW-0
-	-	-	GIR				

Bits	Field	Description
4-0	GIR	Left channel Line in gain programming value.

NOTE: Please refer to section "Programmable Bypass path attenuation: GI" for more details.

26.6.1.22 GCR_DACL: Left channel DAC Gain Control Register

Register Name: GCR_LIBYL Register Address: 0x16

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
RLGOD	-	-	GODR				

Bits	Field	Description
7	RLGOD	DAC digital gain coupling. Read/Write

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		0: Left and right channels gains are independent 1: Left and right channels gain track left channel gain
4-0	GODL	Left channel DAC digital gain programming value.

NOTE: Please refer to section "Programmable digital attenuation: GOD" for more details.

26.6.1.23 GCR_DACR: right channel DAC Gain Control Register

Register Name: GCR_DACR Register Address: 0x17

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	GODR				

Bits	Field	Description
4:0	GODR	Right channel DAC digital gain programming value.

NOTE: Please refer to section "Programmable digital attenuation: GOD" for more details.

26.6.1.24 GCR_MIC1: Microphone 1 Gain Control Register

Register Name: GCR_MIC1 Register Address: 0x18

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	-	-	GIM1		

Bits	Field	Description
2:0	GIM1	Microphone 1 boost stage gain programming value.

NOTE: Please refer to section "Programmable boost gain: GIM".

26.6.1.25 GCR_MIC2: Microphone 2 Gain Control Register

Register Name: GCR_MIC2 Register Address: 0x19

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	-	-	GIM2		

Bits	Field	Description
2:0	GIM2	Microphone 2 boost stage gain programming value.

NOTE: Please refer to section "Programmable boost gain: GIM".

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26.6.1.26 GCR_ADCL: Left ADC Gain Control Register

Register Name: GCR_ADCL Register Address: 0x1A

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
LRGID	-	GIDL					

Bits	Field	Description
7	LRGID	ADC digital gain coupling. Read/Write 0: Left and right channels gains are independent 1: Left and right channels gain track left channel gain
5-0	GIDL	Left channel ADC digital gain programming value.

NOTE: Please refer to the section "Programmable input attenuation amplifier: GID".

26.6.1.27 GCR_ADCR: Right ADC Gain Control Register

Register Name: GCR_ADCR Register Address: 0x1B

bit7-RW-0	Bit6-RW-0	Bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	GIDR					

Bits	Field	Description
5-0	GIDR	Right channel ADC digital gain programming value.

NOTE: Please refer to the section "Programmable input attenuation amplifier: GID".

26.6.1.28 GCR_MIXADC: ADC Digital Mixer Control Register

Register Name: GCR_MIXADC Register Address: 0x1D

bit7-RW-0	bit6-RW-0	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	GIMIX				

Bits	Field	Description
4-0	GIMIX	Mixer gain for input path. Read/Write 00000 : 0dB 00001 : -1dB … by step of 1dB 11111 : -31dB

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26.6.1.29 GCR_MIXDAC: DAC Digital Mixer Control Register

Register Name: GCR_MIXDAC Register Address: 0x1E

bit7-RW-0	bit6-RW-0	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-	-	-	GOMIX				

Bits	Field	Description
4-0	GOMIX	Mixer gain for DAC path. Read/Write 00000 : 0dB 00001 : -1dB … by step of 1dB 11111 : -31dB

26.6.1.30 AGC1: Automatic Gain Control Register 1

Register Name: AGC1 Register Address: 0x1F

bit7-RW-0	bit6-RW-0	bit5-RW-1	bit4-RW-0	bit3-RW-0	bit2-RW-1	bit1-RW-0	bit0-RW-0
AGC_EN	AGC_STEREO	TARGET				-	-

Bits	Field	Description
7	AGC_EN	selection of the AGC system. Read/Write 0 : inactive 1 : enables the automatic level control
6	AGC_STEREO	selection of the AGC system. Read/Write 0 : same gain applied to Left and Right channel 1 : different gains applied to Left and Right channel
5:2	TARGET	Target output level of the ADC. Read/Write: 0000 : -6dB 0001 : -7.5dB … by step of 1.5 dB 1111 : - 28.5dB

NOTE: Please refer to section "AGC system guide" for more details.

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26.6.1.31 AGC2: Automatic Gain Control Register 2

Register Name: AGC2 Register Address: 0x20

bit7-RW-0	bit6-RW-1	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-1	bit1-RW-1	bit0-RW-1
NG_EN	NG_THR			HOLD			

Bits	Field	Description
7	NG_EN	Selection of the Noise Gate system. Read/Write 0: inactive 1: enables the noise gate system
6-4	NG_THR	Noise Gate Threshold value. Input level (dB) < Noise Gate Level (dB). Read/Write 000: -72 dB 001: -66 dB … by step of 6dB 111: -30 dB
3:0	HOLD	Hold time before starting AGC adjustment to the TARGET value. Read/Write 0000: 0ms 0001: 2 ms 0010: 4 ms … Time Step x2 1111: 32.768s

NOTE: Please refer to section "AGC system guide" for more details.

26.6.1.32 AGC3: Automatic Gain Control Register 3

Register Name: AGC3 Register Address: 0x21

bit7-RW-0	bit6-RW-1	bit5-RW-0	bit4-RW-0	bit3-RW-0	bit2-RW-1	bit1-RW-0	bit0-RW-0
ATK				DCY			

Bits	Field	Description
7-4	ATK	Attack Time - Gain Ramp Down. Read/Write 0000: 32 ms 0001: 64 ms … by step of 32 ms 1111: 512 ms

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3-0	DCY	Decay Time - Gain Ramp up. Read/Write 0000: 32 ms 0001: 64 ms … by step of 32 ms 1111: 512 ms

NOTES:

1 DCY and ATK registers values are delays between each step of gain.

2 Please refer to section "AGC system guide" for more details.

26.6.1.33 AGC4: Automatic Gain Control Register 4

Register Name: AGC4 Register Address: 0x22

Bit7-RW-0	bit6-RW-0	bit5-RW-0	bit4-RW-1	bit3-RW-1	bit2-RW-1	bit1-RW-1	bit0-RW-1
-			AGC_MAX				

Bits	Field	Description
4-0	AGC_MAX	Maximum Gain Value to apply to the ADC path.

NOTES:

1 Please refer below table for AGC_MAX setup.

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AGC_MAX	Gain Value	AGC_MAX	Gain Value	AGC_MAX	Gain Value	AGC_MAX	Gain Value
00000	0	01000	12	10000	23	11000	32
00001	1.5	01001	13.5	10001	23	11001	33.5
00010	3	01010	15	10010	23	11010	35
00011	4.5	01011	16.5	10011	24.5	11011	36.5
00100	6	01100	18	10100	26	11100	38
00101	7.5	01101	19.5	10101	27.5	11101	39.5
00110	9	01110	21	10110	29	11110	41
00111	10.5	01111	22.5	10111	30.5	11111	42.5
AGC_MAX	Gain Value	AGC_MAX	Gain Value	AGC_MAX	Gain Value	AGC_MAX	Gain Value
00000	0	01000	12	10000	23	11000	32
00001	1.5	01001	13.5	10001	23	11001	33.5
00010	3	01010	15	10010	23	11010	35
00011	4.5	01011	16.5	10011	24.5	11011	36.5
00100	6	01100	18	10100	26	11100	38
00101	7.5	01101	19.5	10101	27.5	11101	39.5
00110	9	01110	21	10110	29	11110	41
00111	10.5	01111	22.5	10111	30.5	11111	42.5

2 Please refer to section “AGC system guide” for more details.

26.6.1.34 AGC5: Automatic Gain Control Register 5

Register Name: AGC5 Register Address: 0x23

bit7-RW-0	bit6-RW-0	bit5-RW-0	Bit4-RW-0	bit3-RW-0	bit2-RW-0	bit1-RW-0	bit0-RW-0
-			AGC_MIN				

Bits	Field	Description
4-0	AGC_MIN	Maximum Gain Value to apply to the ADC path.

NOTE:

1 Please refer to below table for AGC_MIN setup.

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AGC_MIN	Gain Value	AGC_ MIN	Gain Value	AGC_ MIN	Gain Value	AGC_ MIN	Gain Value
00000	0	01000	12	10000	23	11000	32
00001	1.5	01001	13.5	10001	23	11001	33.5
00010	3	01010	15	10010	23	11010	35
00011	4.5	01011	16.5	10011	24.5	11011	36.5
00100	6	01100	18	10100	26	11100	38
00101	7.5	01101	19.5	10101	27.5	11101	39.5
00110	9	01110	21	10110	29	11110	41
00111	10.5	01111	22.5	10111	30.5	11111	42.5

2 Please refer to section "AGC system guide" for more details.

26.7 Programmable gains

This section helps you to configure the programmable gain amplifier in the CODEC.
Internal signal VREFP is connected to AVDCDC Pin and internal signal VREFN is connected to AVSCDC Pin.

In this section, VREF equals to (VREFP – VREFN).

26.7.1 Programmable boost gain: GIM

The following table gives the relation between the gain and the input level for the microphone input amplifier when GI = 0000.

GIM	Gain value (dB)	Maximum input amplitude
000	0	0.85*VREF
001	4	0.536*VREF
010	8	0.338*VREF
011	12	0.213*VREF
100	16	0.134*VREF
101	20	0.085*VREF
110	20	0.085*VREF
111	20	0.085*VREF

NOTES:

1 Maximum analog input amplitude value is given in Vpp differential.

2 Maximum analog input amplitude is referenced as Full Scale (FS). After conversion, the corresponding digital code of the output value varies from 0x7FFF down to 0x8000 for a

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16-bit word. When the analog input amplitude is greater than FS, the dynamic characteristics are not guaranteed.

3 When a change occurs on GIDi inputs, data are valid on the digital output after about 64 sample periods. If the HPF is activated, data are valid after about 64 sample periods but the offset cancellation is not still completed at this time due to its internal time constant.

26.7.2 Programmable input gain amplifier: GID

The digital gain of ADC path may be programmed through the registers bits GIDL and GIDR.
The value of the gain is programmable from 0 to 23dB with a pitch of 1dB.

The gain and input levels are obtained according to the following table:

GID	Decimal decoded	Gain (dB)	Maximum input amplitude (Vpp. Differential) (FS)
0 0 0 0 0 0	0	0	0.85*VREF
0 0 0 0 0 1	1	1	0.757*VREF
0 0 0 0 1 0	2	2	0.6021*VREF
…	…		
x y z t u v	i	i	0.85 / {10^(i/20)} * VREF
…	…		
0 1 0 1 1 1	23	23	0.06 * VREF
0 1 1 0 0 0	24	23	0.06 * VREF
…	…		
1 0 1 0 1 0	43	43	0.06 * VREF
1 1 1 1 1 1	63	43	0.06 * VREF

NOTE: The last column of the table gives the maximum analog input to be applied on the MICi inputs. The value is given in Vpp differential. These values refer to the external voltage reference VREF equals to (VREFP – VREFN). The voltage levels depend on the VREF voltage.

26.7.3 Programmable digital attenuation: GOD

The attenuation of DAC output amplifier may be programmed independently for the both channels through the registers bits GODL and GODR.

The value of the gain GODL/R is programmable from +0 to –31dB with 1 dB pitch. The gain and output levels are obtained according to the following table:

GOD	Decimal decoded value	Gain Value (dB)

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0	0	0	0	0	0	0
0	0	0	0	1	1	-1
					…	
0	0	1	1	0	6	-3
					…	
1	1	1	1	0	30	-30
1	1	1	1	1	31	-31

26.7.4 Programmable attenuation: GO

The attenuation of Headphone output amplifier may be programmed independently for the both channels through the registers bits GOL and GOR.

The value of the gain GOL/R is programmable from +6 to –25dB with 1 dB pitch. The gain and output levels are obtained according to the following table:

GO					Decimal decoded value	Gain Value (dB)	Maximal PGAT input amplitude (Vpp)	Maximal PGAT output amplitude (Vpp)
0	0	0	0	0	0	+6	0.425*VREF	0.85*VREF
0	0	0	0	1	1	+5	0.478*VREF	0.85*VREF
					…		…	…
0	0	1	0	1	5	+1	0.757*VREF	0.85*VREF
0	0	1	1	0	6	0	0.85*VREF	0.85*VREF
0	0	1	1	1	7	-1	0.85*VREF	0.757*VREF
					…		…	…
1	1	1	1	0	30	-24	0.85*VREF	0.054*VREF
1	1	1	1	1	31	-25	0.85*VREF	0.048*VREF

NOTES:

1 When headphone driver is loaded by a 16 Ohm load, setting GOL/R = 0 is possible. However, set GOL/R to 9 at maximum to preserve dynamic performances. The output stage is sized to support a 70mA current and no more.

2 The last column of the table gives the analog output voltage delivered on the outputs and corresponding to a digital input at FS (Full Scale). The value is given in Vpp single-ended.

3 These values refer to the external voltage reference VREF equals to (VREFP – VREFN). The voltage levels depend on the VREF voltage.

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26.7.5 Programmable Bypass path attenuation: GI

The analog input gain may be programmed through GIL/R.

The value of the gain is programmable from +6 to -25dB with a pitch of 1dB. The gain and input levels are obtained according to the following table:

GI					Decimal decoded value	Gain value (dB)	Maximum input amplitude (Vpp) (FS)
0	0	0	0	0	0	+6	0.425*VREF
0	0	0	0	1	1	+5	0.478*VREF
0	0	0	1	0	2	+4	0.536*VREF
x	y	z	t	u	i	i+6	0.85/{10^((i+6)/20)}*VREF
0	0	1	1	0	6	0	0.85*VREF
					…		0.85*VREF
1	1	1	1	1	31	-25	0.85*VREF

The last column of the table gives the maximum analog input to be applied on the line inputs. The value is given in Vpp. These values refer to the external voltage reference VREF equals to (VREFP – VREFN). The voltage levels depend on the VREF voltage.

26.7.6 Programmable digital mixer gain: GIMIX and GOMIX

The following table gives the relation between the gain and the input level for the microphone input amplifier when GI = 0000.

GIMIX or GOMIX	Gain value (dB)
00000	0
00001	-1
00010	-2
00011	-3
…	…
11101	-29
11110	-30
11111	-31

26.7.7 Gain refresh strategy

GI* and GO* gains are controlled through the control interface. To avoid sound artifacts, the gain

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increases or decreases each time the gain stage output crosses the zero value. Tcrossout time-out counter forces the gain to be updated if a zero crossing event doesn't occur. After each gain step, zero crossing events are ignored during at least Tcrossmin.

In case that gain coupling between both left and right channels is active (LRGi different of RLGi), gain stepping of each channel is independent from the other depending on zero crossing event occurrence.

The duration of Tcrossout and Tcrossmin are given below:

MCLK (MHz)	Tcrossout (ms)	Tcrossmin (ms)
12	21.8	0.171
13	20.2	0.158

26.8 Configuration of the headphone output stage

In cap-coupled connection, codec uses the LOAD register bit to control the ramping duration. Inappropriate setting will lead to a too long or too fast ramping and will create audio artifacts.

To prevent pop-up noise generation due to floating nodes when no load is plugged in the jack connector, it is required to add some resistor devices that act as pull down function (named Rhpl and Rhpr in section "Headphone connnection" and section "Required external components").

Its value has to be determined as following:

Working Mode	Load resistor and bypass capacitor values	LOAD value	Rhpdo value
Driving Headphone	16 Ohm / 220uF	0	470 Ohm typ.
Driving Lineout	10k Ohm / 1uF	1	4.7k Ohm max.

26.9 Out-of-band noise filtering

An internal analog Low Pass Filter at the DAC output is designed to remove the out-of-band noise generated by the delta sigma modulation (Noise Shaper). The internal LPF reduces the amount of energy contained in the wide band part (> 24 kHz) of the output signal. The out-of-band noise, when not removed, can be damageable in some high quality applications.

This filter is always working and does not need configure.

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26.10 Output short-circuit protection (headphone output)

Analog short-circuit protection in the output stage has been implemented to prevent excessive current from flowing through AOHPL, AOHPR output pins. This prevents the output stage from over-heating. The system detects the following cases:

- Abnormal headphone load.

26.10.1 Indication of the short circuit detection

When such an overload is detected on one of AOHPL, AOHPR output pins,

- An interrupt is sent on the IRQ pin and the SCMC flag in the IFR register is set to ‘1’.
- Internally to codec:

  Automatic power-down of the 2 output amplifiers (AOHPL, AOHPR signals) when a short-circuit is detected on AOHPL or AOHPR pin (SCMC flag set to ‘1’).

26.10.2 Reset of short circuit detection

The following sequence has to be to apply:

1 Mask the interrupt by writing ‘1’ in the Interrupt Control Register.

2 Handle the cause of short-circuit according to the events presented in following paragraphs (Capacitor-coupled headphone connection).

3 Update the short-circuit flag by writing ‘1’ in the Interrupt Flag Register.

4 Check the reset of flag by reading the Interrupt Flag Register. The bit must be equal to ‘0’. If it remains at '1', that means that short-circuit is not resolved.

5 Enable the interrupt by writing ‘0’ in the Interrupt Control Register.

26.10.3 Capacitor-coupled headphone connection

It is up to the application to put the output stage in power down mode (SB_HP = ‘1’), to put codec in sleep or complete power-down mode, to reset it.

The short-circuit will be solved by the following events:

- Removal of the inserted jack. (needs the use of HPSENSE pins)
- Reset of codec. (NRST signal)
- Putting the output stage in power-down mode. (SB_HP=1)
- Putting codec in sleep mode. (SB_SLEEP=1)
- Putting codec in complete power-down mode. (SB=1)

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26.11 Sampling frequency: FREQ

The sampling frequency value is given in the FREQ table below.

FREQ	Sampling Rate (Fs)
0000	96kHz
0001	48kHz
0010	44.1kHz
0011	32kHz
0100	24kHz
0101	22.05kHz
0110	16kHz
0111	12kHz
1000	11.025kHz
1001	8kHz
1010	Reserved for further use
….	….
1111	Reserved for further use

26.12 Programmable data word length

The Data Word Length block (DWL) allows selecting the length of the input data and of the output data between 24-/20-/18-/16-bit thanks to AICR.DAC_ADWL and AICR.ADC_ADWL (respectively for the DAC and ADC paths) in accordance with the following table:

ADWL	Word length
0 0	16-bit word length data
0 1	18-bit word length data
1 0	20-bit word length data
1 1	24-bit word length data

The size of the buses is always 24 bits, but the input/output data only use the number of MSB programmed with ADWL. The LSB are considered as ‘0’ in input and set to ‘0’ in output.

The capability to use a data word length of 16 bits is kept for compatibility with standard applications.

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26.13 Ramping system note

An internal mechanism is used to reduce output glitches when the headphone stage enters or leaves the power-down mode.

When the SB_HP is set to '1', the headphone output voltages (AOHPL, AOHPR) are slowly decreased in the same time from AVDHP/2 down to 0.

When the SB_HP is set to '0', the headphone output voltages (AOHPL, AOHPR) are slowly increased in the same time from 0 to AVDHP/2.

After power supplies ramp up, the CODEC start its internal initialization sequence and set SR.ACK_PON register bit once completed.
An interrupt request is sent when the ramp completes.

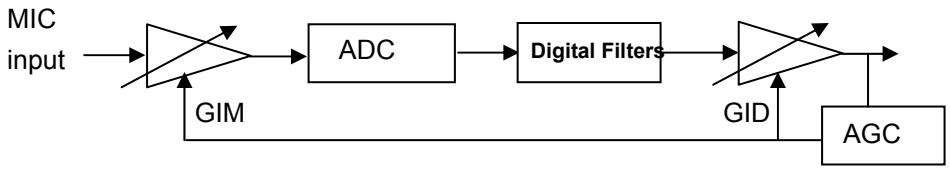
Do not change the level of SB_HP as long as the sequence due to the previous change is not complete or working not guaranteed.

In order to prevent audible glitch, it is required to power-down the output stage (SB_HP=1) before changing the output load with CR1.LOAD.

Please refer to "Anti-pop operation sequences" for details.

26.14 AGC system guide

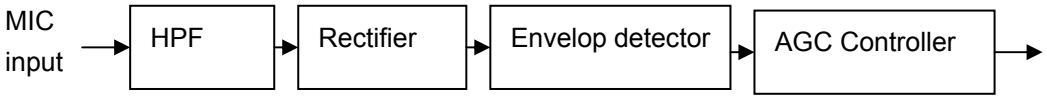
For the microphone input to ADC path, an Automatic Gain Control (AGC) system allows to optimize the signal swing at the input of the ADC.



The AGC circuit compares the output of the ADC to a level and increases or decreases the gain of the microphone preamplifier and the digital gain to compensate. The full dynamic range of the ADC can be used automatically if the audio from the microphone is to be output digitally through the ADC.

The AGC_EN register bit enables the AGC system, in this case INSEL must be equal to "00" or "01".

AGC Block Diagram:



The AGC system is used at the MIC input.

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The HPF filter characteristics: Cut Frequency =300 Hz.
In the in AGC mode, the system of gain control will directly assign the values of the gains GIDL, GIDR and GIM1 (or GIM2).

26.14.1 AGC operating mode

TARGET sets the desired ADC output range level. The AGC system adapts the gain stages (GID and GIM) in order to best reach this target. AGC_MAX and AGC_MIN fix the limits of the gain variation.
Please refer to "CODEC Operating modes" for the AGC System diagram in the "CODEC Power Diagram".

In order that the AGC system should not alter the dynamic content of the signal (voice "tonic" for instance) by continuously adapting the gain to fit the target level, the time between two consecutives gain adjustments is modifiable by the HOLD register value.

After this delay:

- If the output level is lower than TARGET, the gain is increased step by step in accordance to the DCY register value.
- If the output level is higher than TARGET, the gain is decreased step by step in accordance to the ATK register value.

The following figure illustrates the behavior of AGC system:

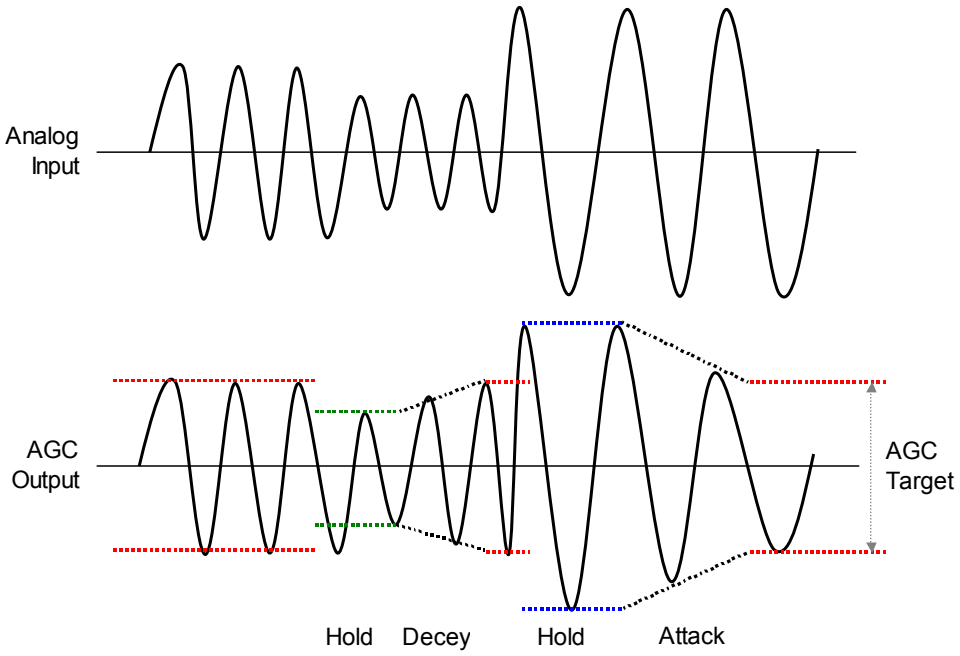


Figure 26-3 AGC adjusting waves

A noise-gating feature, enabled by the NG_EN register bit, prevents gain increases when no signal or

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small signal is present at the input. The noise gate threshold is set by the NG_THR register value.
The following graph shows a more detailed application.
The following graph summarizes the operations and shows more details.

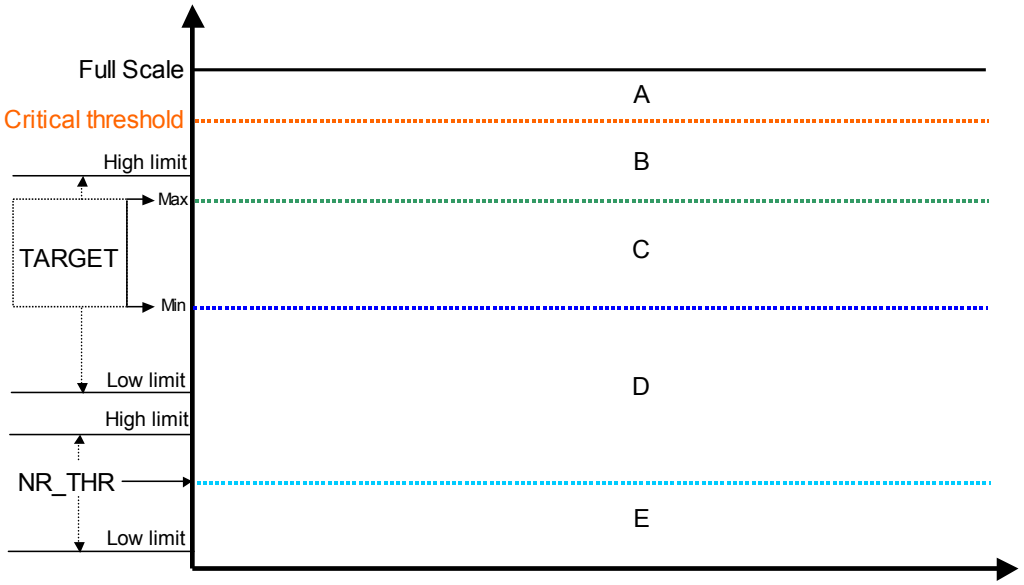


Figure 26-4 AGC adjust areas

The areas from A to E are deferent working area of AGC system, which is listing below:

A: If the signal level is in this critical area: the AGC system decreases quickly the gain at the input of the ADC until the signal goes under the critical threshold.

B: If the signal level remains in this area after the HOLD delay: the AGC system decreases the gain at the input of the ADC until the signal reaches the target area with a slope defined by AGC3.ATK register value.

C: If the signal level is in this area: the AGC system does not perform gain adjustment.

D: If the signal level remains in this area after the HOLD delay: the AGC system increases gain at the input of the ADC until the signal reach the target area with a slope defined by AGC3.DCY register value.

E: If the signal level is in this range: the AGC system considers the signal as noise and does not perform gain adjustment.

26.15 Digital Mixer description

CODEC includes a digital mixer which provides a loopback of the ADC output to the DAC and Headphone output and a loopback of the mixer output to the record path.

Two gains GIMIX and GOMIX control each input of the mixer to adapt the amplitude of the mixed signal. A zero-crossing detection is included on each gain stage to minimize the zipper noise.

A digital multiplexer allows choosing between the ADC signal and the mixer output signal on the record path.

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Another digital multiplexer allows choosing between the DAC signal and the mixer output signal on the playback path.

Please refer to “CODEC Operating modes” for the digital mixer diagram in the “CODEC Power Diagram”.

26.16 Digital microphone interface

CODEC accepts bitstream from digital microphone and converts it into audio data at the sample rate (Fs) selected in FCR_ADC register. CODEC provides a clock (DMIC_CLK) and receives data on DMIC_IN at the same frequency. DMIC_CLK frequency depends on MCLK frequency selection in CCR register.

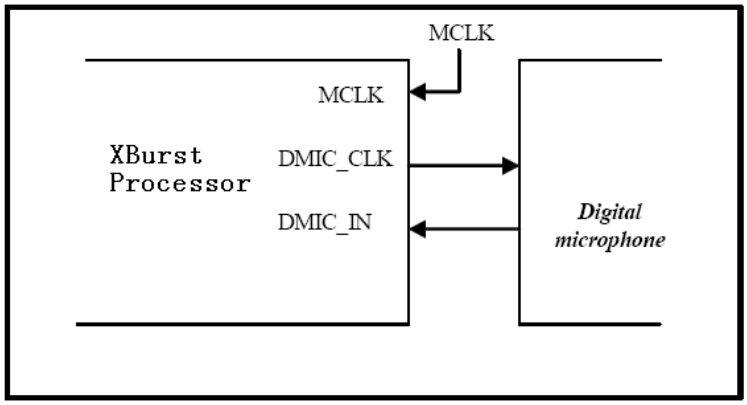


Figure 26-5 Digital microphone interface connection

After conversion, the corresponding digital code of the output value varies from 0x7FFF down to 0x8000 for a 16-bit word, coded in 2's complement.

CODEC can receive simultaneously data from two digital microphones.

26.16.1 Chronogram

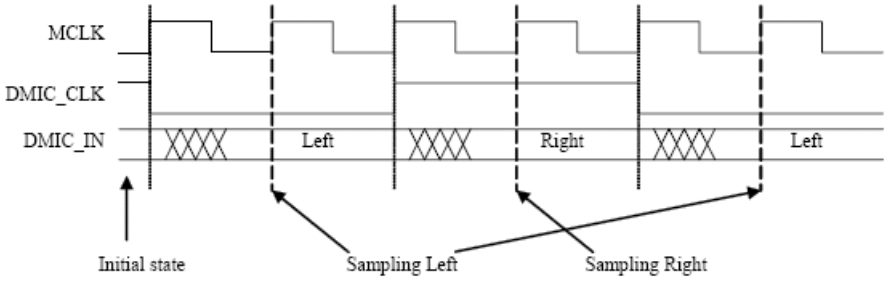
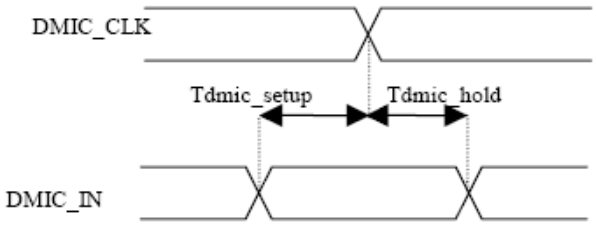


Figure 26-6 Digital microphone timing diagram at MCLK = 12 MHz

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(DMIC_CLK = 3 MHz) and MCLK = 13 MHz (DMIC_CLK = 3.25 MHz)

26.16.2 Timings



Parameter	Symbol	Min	Typ	Max	Unit
DMIC_CLK frequency	F_{dmic_clk}	3	-	3.25	MHz
DMIC_CLK duty cycle	D_{dmic_clk}	0.4	0.5	0.6	-
DMIC_IN setup time	T_{dmic_setup}	T_{MCLK} + 10	-	-	ns
DMIC_IN hold time	T_{dmic_hold}	0	-	-	ns

26.16.3 Noise template (TBC)

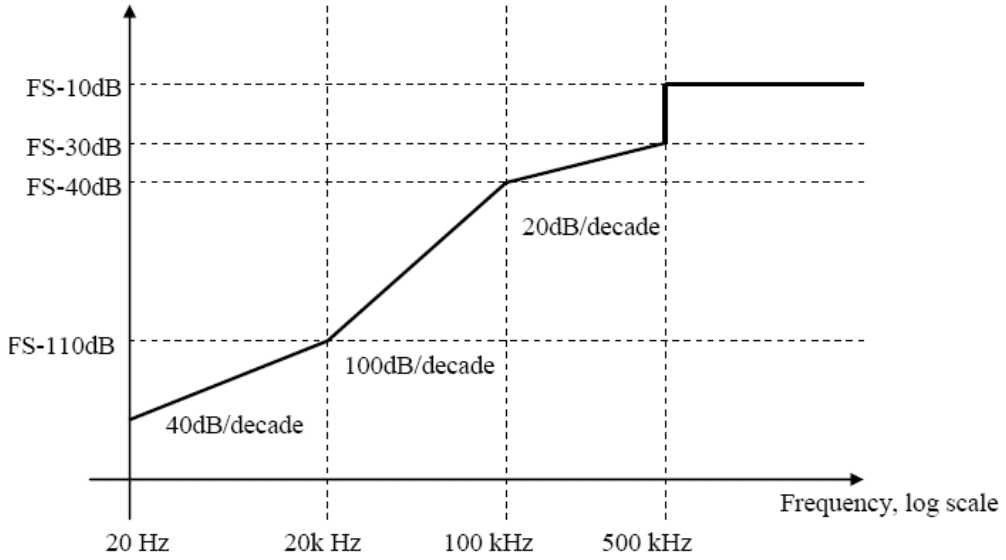


Figure 26-7 Digital microphone modulation noise reference spectrum

(with FFT resolution = 20 Hz and 7 terms Blackman-Harris windowing)

If the noise at the digital microphone output is higher than the reference in the [20 Hz – 20 kHz] bandwidth, the SNR will be limited by the digital microphone in-band noise.

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If the noise at the digital microphone output is higher than the reference for frequencies beyond 20 kHz, the SNR will be limited by the aliasing of the digital microphone quantization noise.

26.17 CODEC Operating modes

Different operating modes are available:

- Power-up mode: During power on time, CODEC is in this mode.
- Reset mode: When NRST is low, CODEC is in this mode.
- Soft mute mode: When DAC_MUTE is 1, CODEC is in this mode.
- Complete Power-down mode: After RESET, CODEC is in this mode.
- SLEEP modes: When SB_SLEEP is 1, CODEC is in this mode.
- Normal mode: When CODEC is not in above mode, it is in this mode. This mode has three modes: RECORD mode, REPLAY mode, RECORD_REPLAY mode.

The power diagram is shown below.

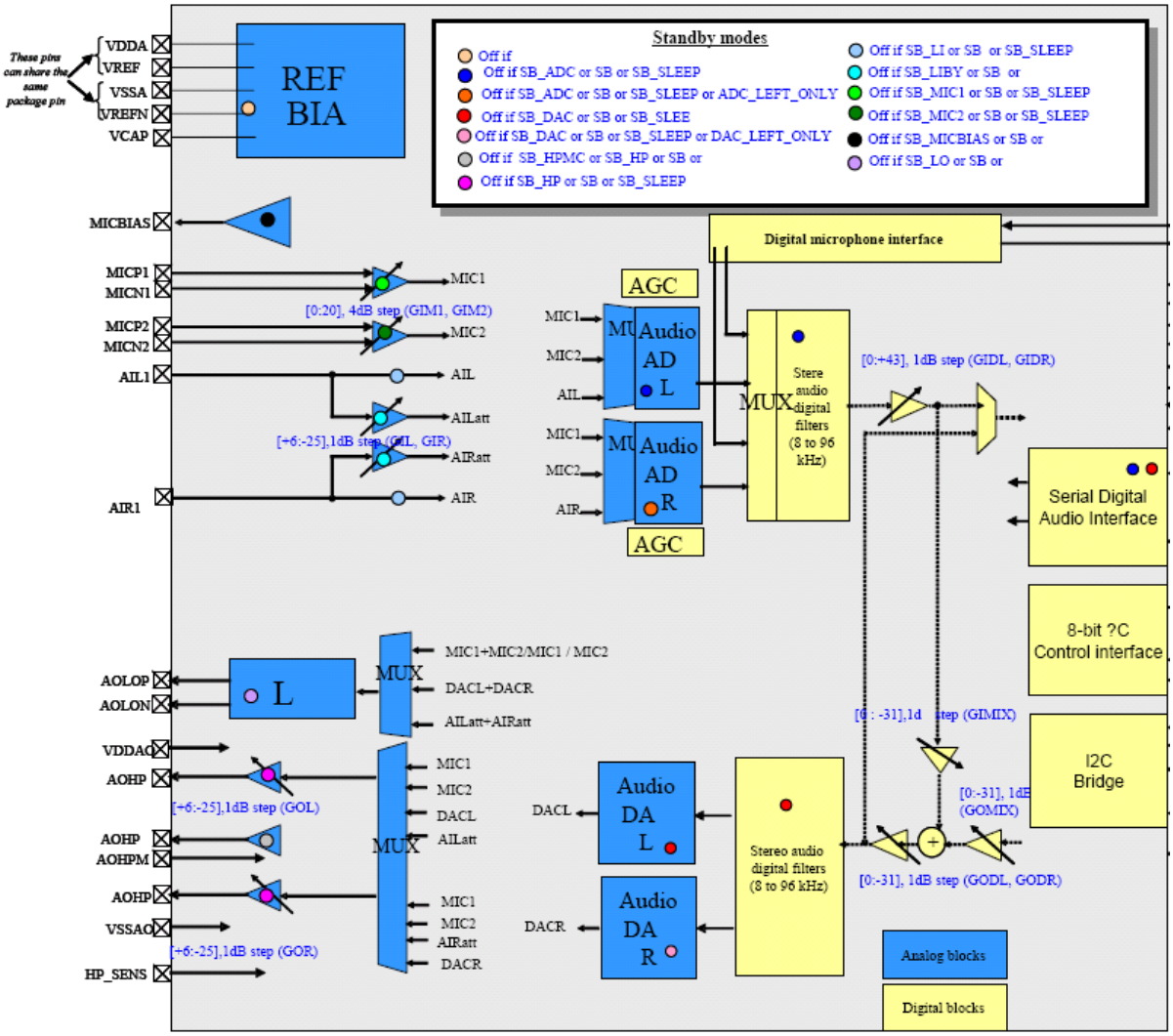


Figure 26-8 CODEC Power Diagram

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There are many power parts of CODEC. Any part could be powered down independently.

26.17.1 Power-On mode and Power-Off mode

When the power supply ramps up, CODEC enters the power-on mode. During the reset, the CODEC is put in stand-by in order to reduce audible pops.

The CODEC doesn't handle the power supply ramp down on itself. The software has to turn the CODEC in complete stand-by mode before the power supply starts to ramp down.

26.17.2 RESET mode

The reset input signal is asynchronous; the reset minimum duration is one SYS_CLK cycle.
During the power-up mode and system reset, the CODEC goes into Reset mode.
After system reset the CODEC will exit Reset mode and go to STANDBY mode.

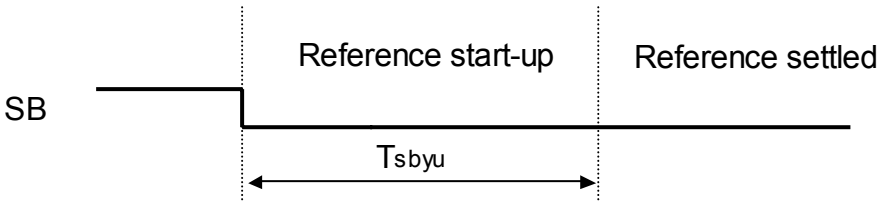
NOTES:

1 Except during the power-up mode, do NOT perform any reset in order to avoid audible pops.
2 Resetting the CODEC during normal operating mode will turn instantaneously the CODEC in STANDBY mode. This will lead to generate a large audible pop.

26.17.3 STANDBY mode

CODEC goes to STANDBY mode when the SB register bit equals 1, and all functions including ADC path, DAC path and analog references will stop and whole CODEC is shutdown for saving power. CODEC is complete down in this mode.

During the STANDBY mode, the power consumption is reduced to a minimum, so it is also called Complete Power-Down mode. When SB is set to '0', CODEC leaves the STANDBY mode. It is necessary to wait some time before the CODEC references settle. This time is called Tsbyu. When CODEC reference settled, it is in SLEEP mode.



Please refer to the section "Timing parameters" for the Tsbyu Value.

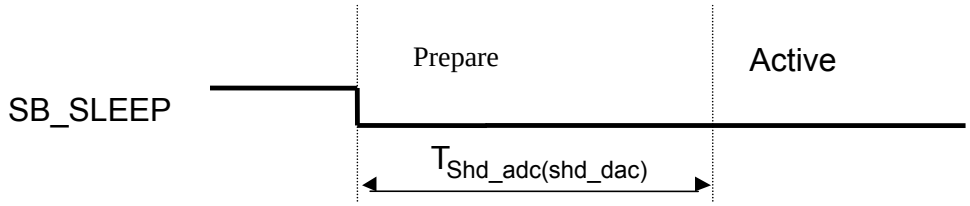
26.17.4 SLEEP mode

When SB_SLEEP is set to 1, CODEC enters in sleep mode. The logical part and the analog functions, except the voltage and biasing references, enter in power-down mode. So, the power consumption is

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reduced without penalizing the start-up time.

When SB_SLEEP falls, CODEC leaves the corresponding STANDBY mode; it is necessary to wait some time before the CODEC reaches the normal mode. Depending on the selected mode, this time is either called Tshd_adc (SB_ADC=0) for the ADC path or Tshd_dac (SB_DAC=0) for the DAC path.



Please refer to the section "Timing parameters" for the Tshd_adc and Tshd_dac Value.

26.17.5 Soft Mute mode

Soft Mute mode is used in order to reduce audible parasites when before the DAC enters or after leaves the Normal mode. Set the DAC_MUTE register bit to 1, it will go to Soft Mute mode.

Set DAC_MUTE to 1 puts the DAC in Soft Mute mode. The CODEC decreases progressively the digital gain from 0dB to -∞. When the gain down sequence is completed, the signal of the DAC is equal to 0 whatever the value of the digital input data is. Then CODEC generates an interrupt and if ICR.GDO_MASK is 0, and set IFR.GDO register bit to 1.

During Soft Mute mode, the DAC is still converting but the output final voltages (AOL, AOR) are equal to VREF/2, so the differential of the Headphone voltage is zero that cause no sound output.

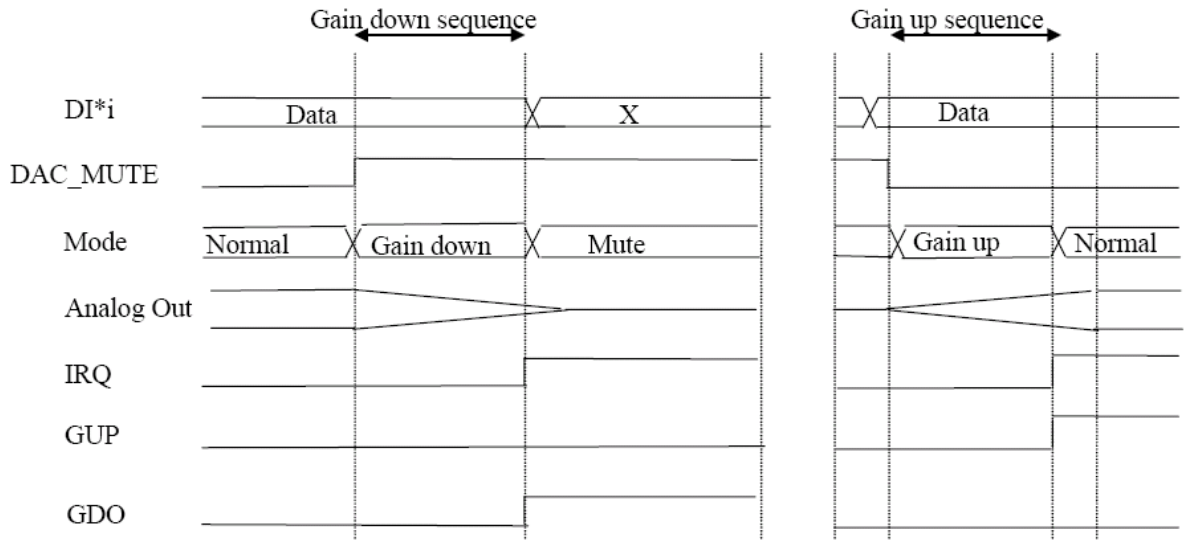


Figure 26-9 Gain up and gain down sequence

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In the opposite, when DAC_MUTE is set to 0, the DAC leaves the Soft Mute mode by increasing progressively the digital gain from -∞ to 0dB. When the gain up sequence is completed, the DAC returns in Normal mode. The CODEC then generates an interrupt and if ICR.GDO_MASK is 0, and set IFR.GDO register bit to 1.
After exiting Soft Mute mode, the DAC output will flow the DAC input data, and there is sound in the Headphone.

The duration of gain down and gain up sequences are nearly independent of Fs and is about 23ms.

NOTES:

1 Do NOT change the value of DAC_MUTE while the effect of the previous change is not reached, or the working is not guaranteed.
2 Do NOT enter in stand-by mode while the gain sequence is not completed, or the working is not guaranteed.

26.17.6 Power-Down mode and ACTIVE mode

Twelve stand-by inputs allow putting independently the different parts of CODEC into Power-Down mode.

When all SB_*=1 except SB=0 and SB_SLEEP=0, the CODEC is in ACTIVE mode, it's ready for play sound or record sound. But still need follow the anti-pop start or stop sequence. Please refer to "Start up sequence" and "Shutdown sequence".

26.17.7 Working modes summary

Different working modes are sum-up in the following table (non exhaustive table):

Mode	SB	SB_SLEEP	SB_DAC	SB_HP	SB_LO	SB_ADC	SB_MICBIAS	SB_MIC1	SB_MIC2	SB_LIN	SB_LIBY	IN_SEL	HP_SEL	LO_SEL	MIC_STEREO	DAC_LEFT_ONLY	ADC_LEFT_ONLY	DAC__MUTE	HP_MUTE	LO_MUTE
Reset mode (complete power-down mode)	1	1	1	1	1	1	1	1	1	1	1	00	00	00	1	0	0	1	1	1
Complete power-down mode	1	x	x	x	x	x	x	x	x	x	x	xx	xx	xx	x	x	x	x	x	x
Sleep mode	0	1	x	x	x	x	x	x	x	x	x	xx	xx	xx	x	x	x	x	x	x
Record Mode																				
Mono MIC1 input	0	0	x	x	x	0	x	0	x	x	x	00	xx	xx	0	x	x	x	x	x
Mono MIC2 input	0	0	x	x	x	0	x	x	0	x	x	01	xx	xx	0	x	x	x	x	x
Record Mode, stereo MIC																				

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inputs,																				
MIC1 to left channel	0	0	x	x	x	0	x	0	x	x	x	00	xx	xx	1	x	0	x	x	x
MIC2 to left channel	0	0	x	x	x	0	x	x	0	x	x	01	xx	xx	1	x	0	x	x	x
Record Mode, Line input	0	0	x	x	x	0	x	x	x	0	x	10	xx	xx	x	x	0	x	x	x
Playback mode, DAC to HP	0	0	0	0	x	x	x	x	x	x	x	xx	11	xx	x	0	x	0	0	x
Playback mode, DAC to LO	0	0	0	x	0	x	x	x	x	x	x	xx	xx	11	x	x	x	x	x	0
Bypass mode, Line to HP	0	0	x	0	x	x	x	x	x	x	0	xx	10	xx	x	x	x	x	0	x
Bypass mode, Line to LO	0	0	0	x	0	x	x	x	x	x	x	xx	xx	10	x	x	x	x	x	0
Sidetone mode,																				
Mono MIC1 input to HP	0	0	x	0	x	x	x	0	x	x	x	xx	00	xx	0	x	x	x	0	x
Mono MIC2 input to HP	0	0	x	0	x	x	x	x	0	x	x	xx	01	xx	0	x	x	x	0	x
Sidetone mode, stereo MIC to HP,																				
MIC1 to left channel	0	0	x	0	x	x	x	0	x	x	x	xx	00	xx	1	x	x	x	0	x
MIC2 to left channel	0	0	x	0	x	x	x	x	x	x	x	xx	01	xx	1	x	x	x	0	x
Sidetone mode,																				
Mono MIC1 input to LO							0	x	x	x		xx	xx	00	0	x	x	x	x	0
Mono MIC2 input to LO	0	0	x	x	0	x	x	x	0	x	x	xx	xx	01	0	x	x	x	x	0
MIC1+MIC2 to LO	0	0	x	x	0	x	x	0	0	x	x	xx	xx	0x	1	x	x	x	x	0

26.18 SYS_CLK turn-off and turn-on

The main clock of CODEC is called SYS_CLK, which is generated in CPM module and called MCLK. During the SLEEP mode and the complete power-down mode, the main clock SYS_CLK may be stopped to reduce the power consumption to the leakage currents only. In other modes, the main clock SYS_CLK must not be stopped.

The main clock SYS_CLK must not be stopped until CODEC has reached the complete power-down mode and must be restarted before leaving the power-down mode.

After SYS_CLK restarts, it is required to wait 4 SYS_CLK cycles before reading or writing the registers.

When SYS_CLK is turned off (SB_SLEEP=1 or SB=1), writing on register values are not taken into account, register values are not up to date when read and interrupts not generated until SYS_CLK turns on.

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26.19 Requirements on outputs and inputs selection and power-down modes

The following rules must be respected in order not to damage performances and to keep the functionality:

- If SB_MIC1 is set to 1, MICSTEREO must be equal to 0, IN_SEL, HP_SEL and LO_SEL must not be equal to ‘00’.
- If SB_MIC2 is set to 1, MICSTEREO must be equal to 0, IN_SEL, HP_SEL and LO_SEL must not be equal to ‘01’.
- If SB_LINE is set to 1, IN_SEL must not be equal to ‘10’.
- If SB_LIBY is set to 1, HP_SEL and LO_SEL must not be equal to ‘10’.
- If SB_DAC is set to 1, HP_SEL and LO_SEL must not be equal to ‘11’.

26.20 Anti-pop operation sequences

The main idea of this section is to describe the sequences to perform to minimize the audible pop to the minimum for the headphone output.

Due to the large number of stand-by combinations and to be the most flexible, the handling of the sequence from one working mode to another is left to the software. So for helping the software designer in this task, some specific sequences are automatically performed by CODEC and an interrupt mechanism (IRQ signal and associated registers) warns the application when these sequences end.

26.20.1 Initialization and configuration

To use the embedded CODEC with AIC, several AIC registers should be set up the below register of AIC before start the CODEC:

AICFR.ICDC = 1
AICFR.AUSEL = 1
AICFR.BCKD = 0
AICFR.SYNCD = 0
I2SCR.AMSL = 0
I2SCR.ESCLK = 1

26.20.2 Start up sequence (DAC)

This sequence is from Power-on mode to CODEC REPLAY mode.
The output sound is driving by DAC.
The intent of the following sequence is to prevent for large audible glitches due to the system start-up with the CODEC.

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Before this sequence, setup the AIC properly.

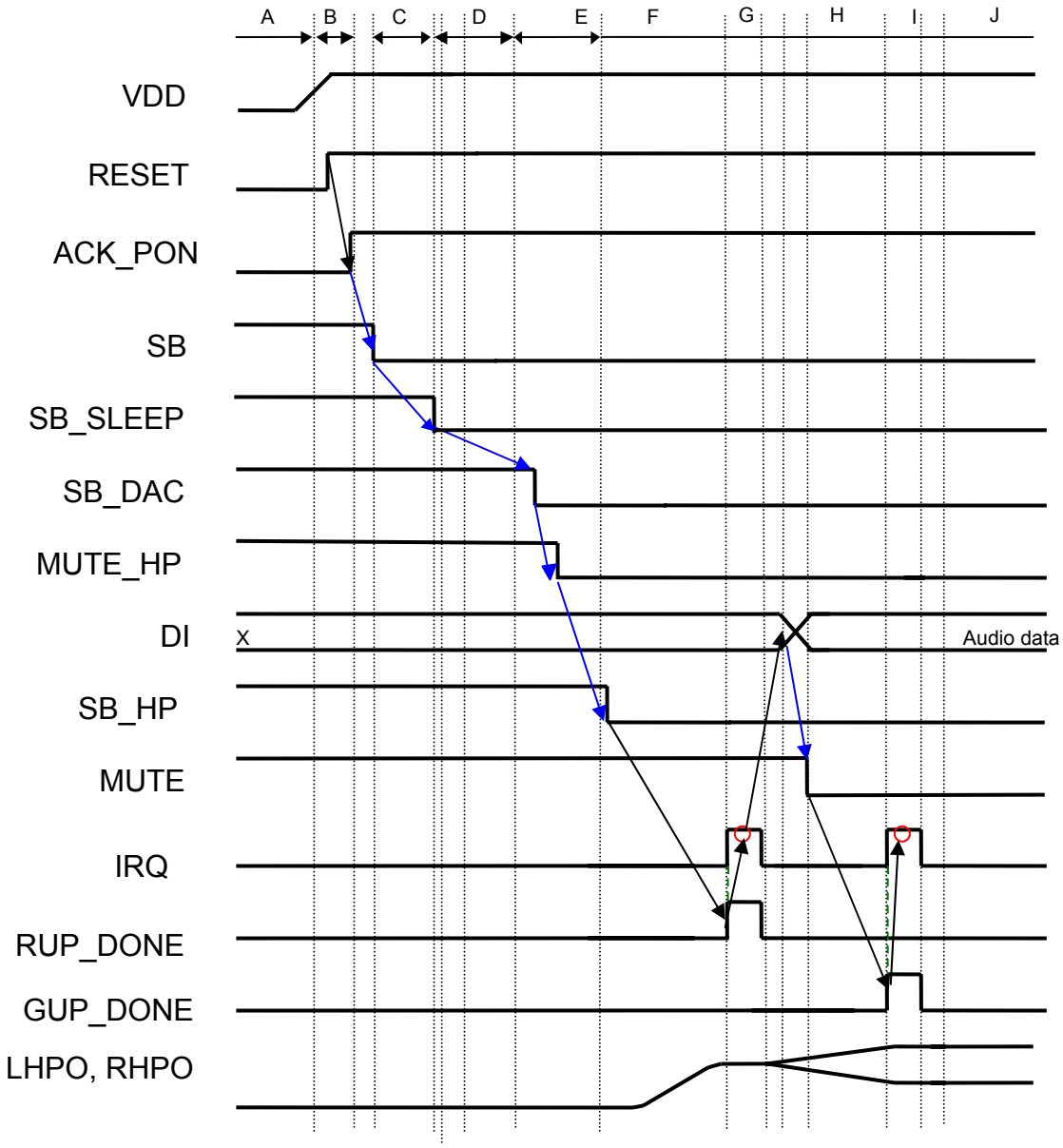


Figure 26-10 Start up sequence

NOTES:

1 The sequences in **blue** are manually handled by the software.

2 The sequences in **black** are automatically handled by the CODEC.

3 **Red** circles are interrupts automatically generated by the CODEC.

SEQUENCE:

A Initial state.
The power supply is off.

B Power supply ramp up.

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The RESET of CODEC is '0' during system reset. The CODEC starts its internal initialization sequence and set ACK_PON register bit once completed.

C Starting of CODEC reference.
The software turns the CODEC on SLEEP mode by clearing SB register bit to 0. The duration equals Tsbyu. After waiting the Tsbyu duration (for example, on event generated by a timer at the application level), the CODEC is in SLEEP mode, the ADC and DAC path are ready to be turn to active mode.

D Go from SLEEP mode to active.
The application turns on the DAC by clearing SB_SLEEP register bits to 0.

E Turn on DAC.
Once after leaving SLEEP mode, the application turns on the DAC (SB_DAC=0) and after 0.5 ms switch the analog mute signal of the port to activate to 0 (MUTE_HP=0) .

F Ramp up cycle.
After waiting 1 ms, the application turns on the headphone output stage (SB_HP=0).

G Ramp up IRQ generation.
Once the ramp up cycle completes, the CODEC sets the RUP_DONE flag to 1 and generates an interrupt.

H IRQ handling and gain up cycle.
The application handles the interrupt, resets the RUP_DONE flag by writing 1 on it and releases the mute of the DAC (DAC_MUTE=0). In the same time, the application sends valid audio data to the CODEC DAC.

I Gain up IRQ generation.
Once the gain up cycle completes, the CODEC sets the GUP_DONE flag to 1 and generates an interrupt.

J IRQ handling and DAC active mode.
The application handles the interrupt and resets the GUP_DONE flag by writing 1 on. The CODEC DAC path is now fully activated.

26.20.3 Shutdown sequence (DAC)

This sequence is from CODEC REPLAY mode to STANDBY mode.
The output sound is driving by DAC.

The intent of the following sequence is to prevent for large audible glitches due to the system shutdown with the CODEC.

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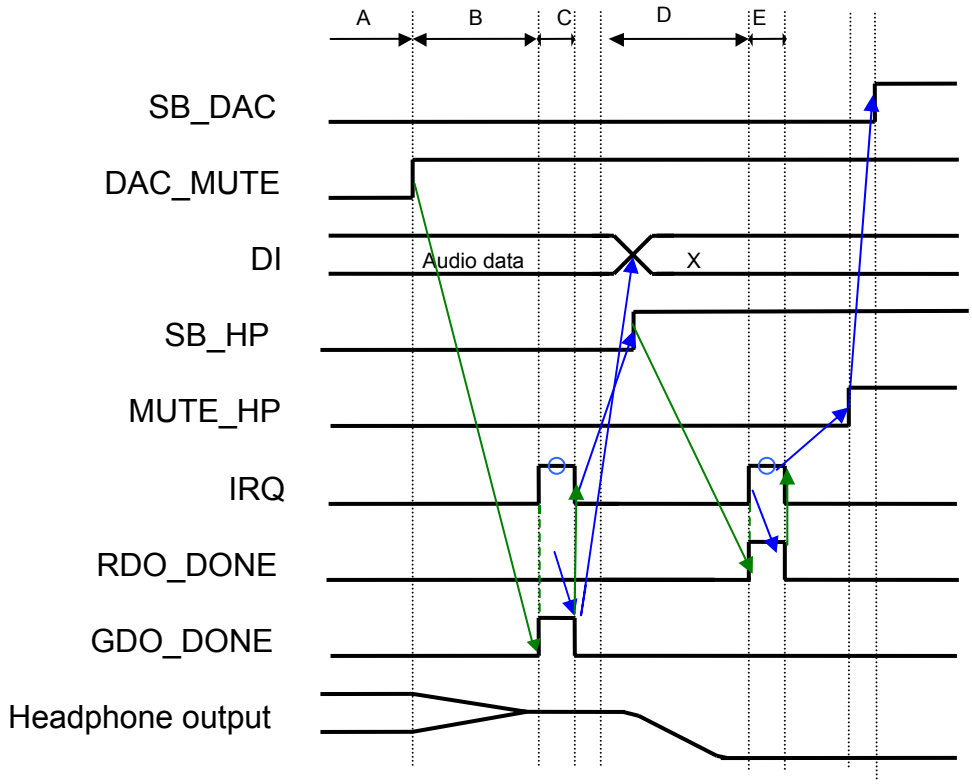


Figure 26-11 Shutdown sequence

NOTES:

1 The sequences in blue are handled by the software.

2 The sequences in black are automatically handled by the CODEC.

SEQUENCE:

A Initial state.

The power supply is on, CODEC DAC path is fully activated.

B Gain down cycle.

The application activates the mute of the DAC (DAC_MUTE=1). Once the gain down cycle completes, the CODEC sets the GDO_DONE flag to 1 and generates an interrupt.

C Gain down IRQ handling and ramp down cycle.

The application handles the interrupt and resets the GDO_DONE flag by writing 1 on it. The application can then stop sending audio data and turns off the headphone output stage (SB_HP=1).

D Ramp down IRQ generation.

Once the ramp down cycle completes, the CODEC sets the RDO_DONE flag to 1 and generates an interrupt.

E IRQ handling.

The application handles the interrupt and resets the RDO_DONE flag by writing 1 on it. Then, the application can activate the analog mute (MUTE_HP=1). Finally, the application turns off

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the DAC path (SB_DAC=1) to be in sleep mode or turn off the CODEC (SB_SLEEP=1, SB=1).

26.20.4 Start up sequence (Line input)

This sequence is from Power-on mode to CODEC REPLAY mode.
The output sound is driving by Line input.
The intent of the following sequence is to prevent for large audible glitches due to the system start-up with the CODEC.

SEQUENCE:

A initial state.
DAC or Line in channel is already in use, valid analog audio signals are available at the input of the switch matrix.

B initializing output port.
The application first set the line in and headphone gain stages to their minimum value (gain automatically forced when the port is in power-down mode). This setting is taken into account in few clocks cycles. Set the MUTE_HP=0, Then the application turns on the headphone output stages (SB_HP = 0).

C Ramp up IRQ generation.
Once the ramp up cycle completes, the CODEC sets the RUP_DONE flag to 1 and generates an interrupt.

D Ramp up IRQ handling and line in stage gain up.
The application handles the interrupt and resets the RUP_DONE flag by writing 1 on it. The application then set the line in gain stage to the wished value.
The maximum duration of the gain ramping equals Trlinemax:

$$Trlinemax = N1 * Tcrossout$$

N1 is the number of line in gain steps.
Please Refer to section "Gain refresh strategy" for the value of Tcrossout.

E Headphone stage gain up.
The application set the headphone gain stage to the wished value. The maximum duration of the gain ramping equals Troutmax:

$$Troutmax = N2 * Tcrossout$$

N2 is the number of headphone gain steps.

F active mode.
The signal path is now fully activated.

26.20.5 Shutdown sequence (Line input)

This sequence is from CODEC REPLAY mode to STANDBY mode.
The output sound is driving by Line input.

The intent of the following sequence is to prevent for large audible glitches due to the system

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shutdown with the CODEC.

SEQUENCE:

A active mode.
The signal path is now fully activated.

B headphone stage gain down.
The application set the headphone gain stage to the minimum value. The maximum duration of the gain ramping equals Tdoutmax:

Tdoutmax = N3 * Tcrossout

N3 is the number of headphone gain steps.
Please Refer to section "Gain refresh strategy" for the value of Tcrossout.

C line in stage gain down.
The application set the line in gain stage to the minimum value. The maximum duration of the gain ramping equals Tdlinemax:

Tdlinemax = N4 * Tcrossout

N4 is the number of headphone gain steps.

D Ramp down cycle.
Then, the application can activate the analog mute (MUTE_HP=1) and turns off the headphone output stages (SB_HP=1).

E Ramp down IRQ generation.
Once the ramp up cycle completes, the CODEC sets the RDO_DONE flag to '1' and generates an interrupt.

F Ramp down IRQ handling.
The application handles the interrupt and resets the RDO_DONE flag by writing '1' on it. The signal path is now off.

26.21 Circuits design suggestions

This section lists a few PCB design suggestions with difference using mode.

26.21.1 Avoid quiet ground common currents

26.21.1.1 References pins

To work properly, CODEC requires few additional external components.

CODEC includes an internal voltage reference. To insure a correct common mode biasing of the internal components, an additional voltage VCAP is used. This requires connecting two decoupling capacitors (Cext) between the pin VCAP and AVSCDC. One 10uF low ESR (ceramic or tantalum) and one 100nF ceramic have to be used. The ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch).

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26.21.1.2 Power supply pins

CODEC analog power supplies require external decoupling capacitors.

For each power supply pin, one 100nF ceramic capacitor has to be used. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch). One low ESR (ceramic or tantalum) capacitor has to be used to decouple the analog power supply provided to the CODEC. Its value depends on the power supply generator; its typical value is between 1uF and 10uF. Ideally use separate ground planes for analog and digital parts.

Connect all ground pins with thick traces to power plane in order to ensure lowest impedance connections.

AVSCDC must be connected to the PCB analog single point reference (star connection) ground (AGND).

26.21.2 Headphone connection (Capacitor-coupled)

Capacitor-coupled headphone and line connection

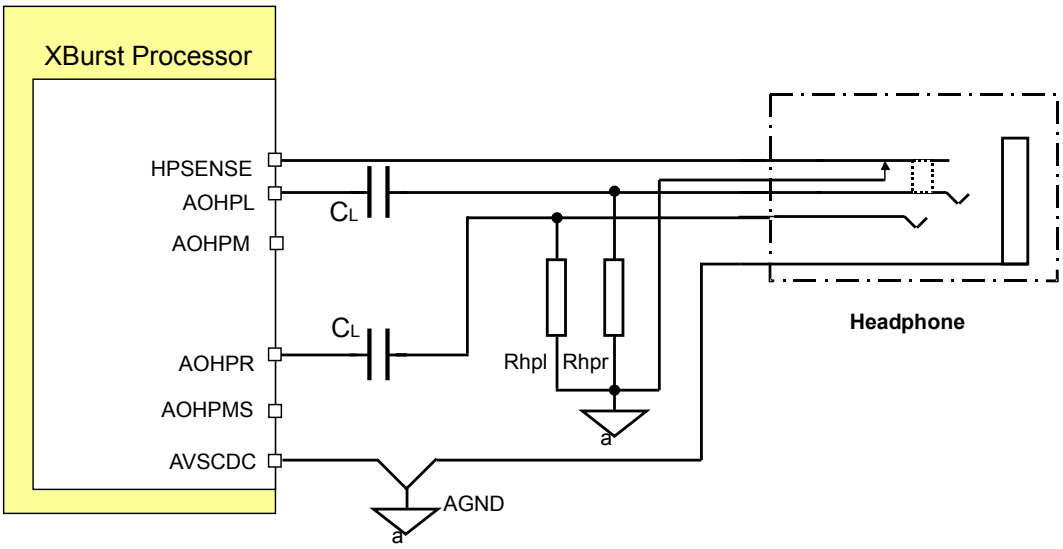


Figure 26-12 Capacitor-coupled connection

The AOHPL and AOHPR pins are connected to the headphone through an external bypass capacitor which is a DC blocking capacitors.

This capacitor is called C_L. When the headphone resistance R_L is 16 Ohm, The tantalum blocking capacitor C_L is 220 uF.

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The DC value of the signal AOHPL or AOHPR equals to AVDCDC/2.

The ground of the headphone is connected to AGND, which is the PCB analog single point reference (star connection) ground.

Capacitor-less headphone connection

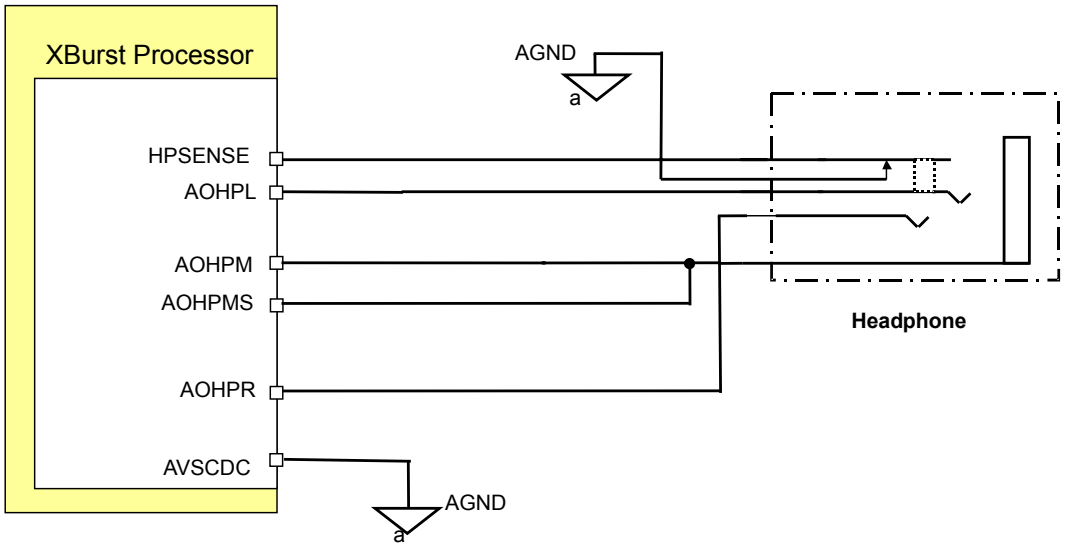


Figure 26-13 Capacitor-less connection

The signals AOHPL and AOHPR from chip are applied directly to the loads. The ground of the headphone is connected to AOHPM. The DC value of the signal AOHPi equals to VREF/2.
The measurement ground reference corresponds to the physical interconnection of AOHPM and AOHPMS.
The measurement is done between AOHPL/R and the measurement ground reference.

NOTE: If you want to use headphone as the antenna for FM , you had better choose this mode.

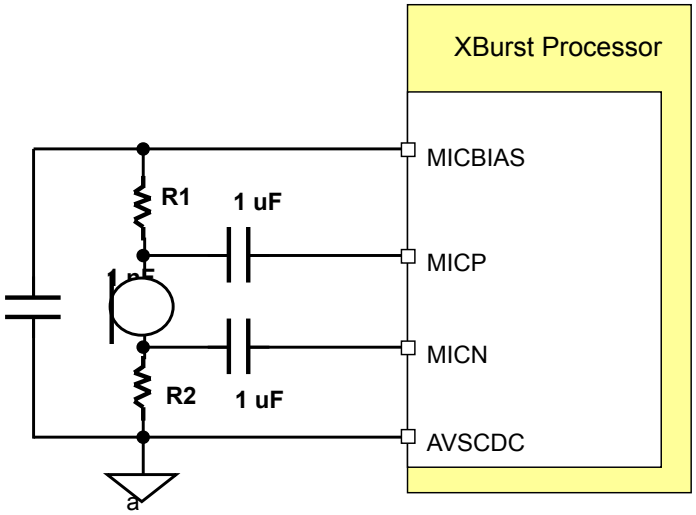
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26.21.3 Microphone connection

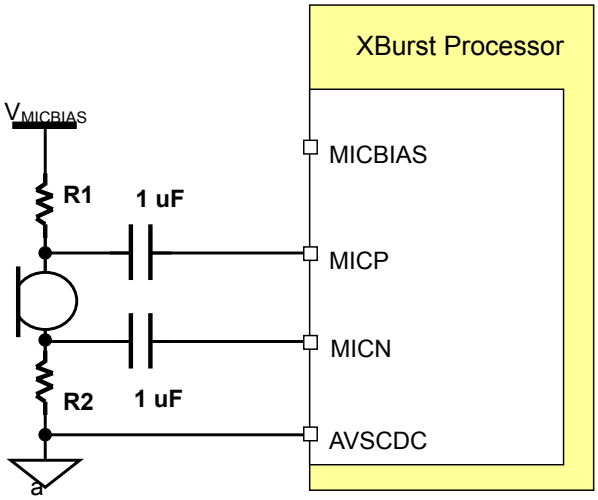
The optimal performance for the SNR is obtained in differential Microphone inputs with a FS input level corresponding to the following values: the peak-to-peak amplitude of the signal is 0.2125V, corresponding to 0.085*VREF Vpp.

We recommend customer to use differential MIC input for better performance.

Application schematic with differential MIC input (using MICBIAS pin):

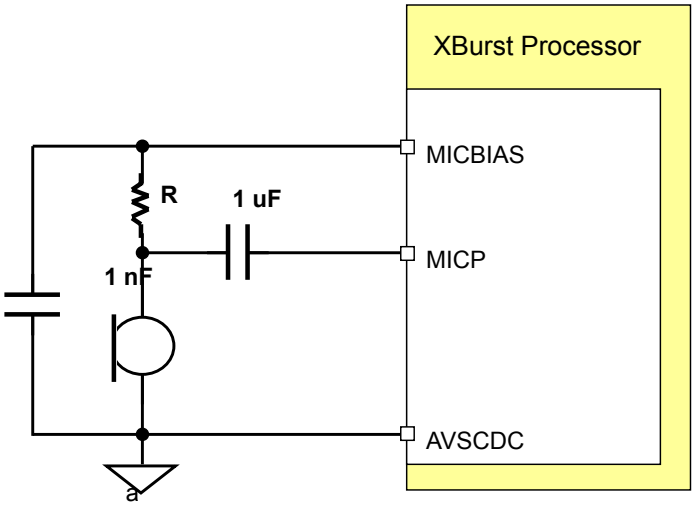


Application schematic with differential MIC input (Vmicbias generated on board):

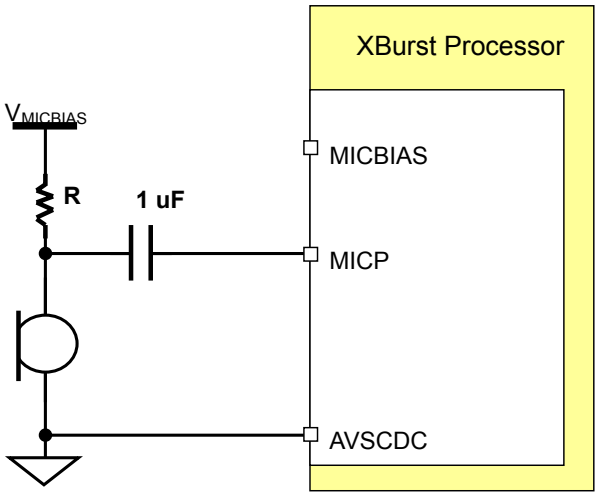


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Application schematic with single-ended MIC input (using MICBIAS pin):



Application schematic with single-ended MIC input (Vmicbias generated on board):



In single-ended connection, one external resistor (R) has to be used to bias the electret microphone. In differential connection, a pair of external resistor (R1, R2) has to be used to bias the electret microphone. The resistors value relation between them is R1 = R2 = R/2.

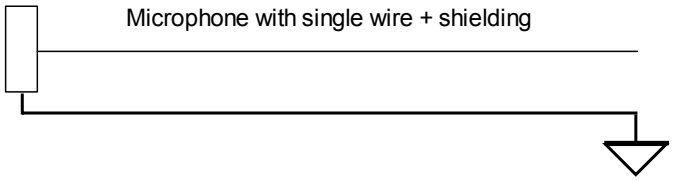
Specific value of resistor (R, commonly from 2.2k Ohm to 4.7k Ohm) and Vmicbias (if generated on board, usually from 1 to 2V or more) depends on the selected EC (Electret Condenser) microphone. The 1nf decoupling capacitance used in MICBIAS pin removes high frequency noise of the chip.

Setting SB_MIC1/SB_MIC2 to 1 will close microphone input path for saving power, also setting SB_MICBIAS to 1 will close MICBIAS stage and the MICBIAS output voltage will be zero.

MICBIAS output voltage scales with AVDCDC, equals to 5/6*AVDCDC (typical 2.08V).
MICBIAS output current is 4mA max.
MICBIAS output noise is 40uVrms max.

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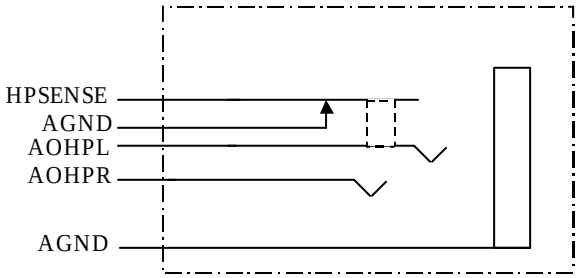
This configuration is better suited for microphone with single wire + shielding.



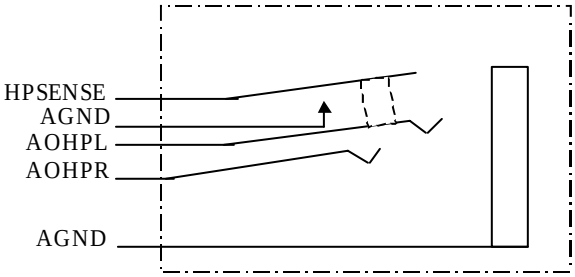
The AVSCDC Pin is connected the analog quiet reference ground in the chip (refers to Grounds and analog signal references). So the ground of MIC must be connected to AVSCDC using a star connection.

26.21.4 Description of the connections to the jack

When the jack is inserted, “sense” and “ground” are disconnected.



No jack plugged: the switch acts as a short-circuit.



Jack plugged: the switch acts as an open circuit.

26.21.4.1 Grounds and analog signal references

In order to limit the parasitic disturbances from the AVSHP output power supplies to inter VREFN analog quiet ground(which is using AVSCDC pin), should use the following principle to distribute the grounds.

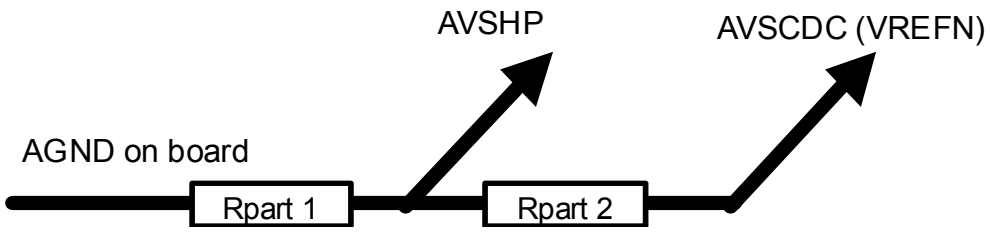


Figure 26-14 Ground distributing

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Minimize the values of the connections parasitic resistance Rpar1, Rpar2.

Take a special care for Rpar1 in order to limit the disturbance from the output stages (AVSHP) to the signal reference (VREFN).

The reference of the input signals must be connected to VREFN (internal quiet ground which using the AVSCDC pin) using a star connection.

26.21.5 PCB considerations

To work properly, CODEC analog power supplies require external decoupling capacitors.

In the VCAP pin, one 10uF low ESR (ceramic or tantalum) called C2 and one 100nF ceramic called C1 have to be used. The ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch).

For each power supply pin, one 100nF ceramic capacitor has to be used. The capacitor used in AVDCDC pin is called C4, the capacitor used in AVDHP pin is C6. These ceramic capacitors have to be kept as close as possible to IC package (closer than 0.2 inch).

One low ESR (ceramic or tantalum) capacitor called C3 has to be used to decouple the analog power supply provided to the CODEC. Its value depends on the power supply generator; its typical value is between 1uF and 10uF. Ideally use separate ground planes for analog and digital parts.

C1, C2, C3, C4, C5, C6 and C7 are defined in section "Required external components".

The reference PCB design is shown below:

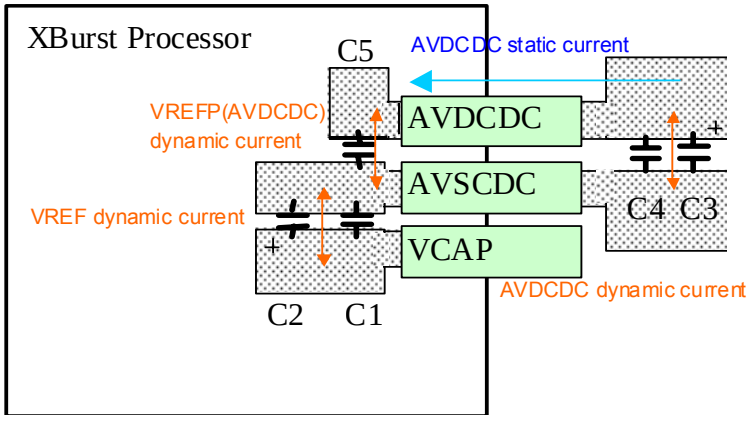


Figure 26-15 the bottom corner of chip PCB Layer

This is just an example reference diagram. You should change and select the PCB layer and route with

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your design constraints.

26.21.5.1 Required external components

The following table summarizes the external components required for a proper working of CODEC, except those used for the analog input and output signals.

Name	Description	Typical Value	Unit
C1	Ceramic reference decoupling capacitor. Cext.	100	nF
C2	Tantalum reference decoupling capacitor. Cext.	10	uF
C3	Tantalum analog power supply decoupling capacitor.	1 to 10	uF
C4	Ceramic AVDCDC decoupling capacitor.	100	nF
C5	Ceramic inter signal VREFP decoupling capacitor (can be shared with C4).	100	nF
C6	Ceramic AVDHP decoupling capacitor. Not shown in section PCB considerations.	100	nF
C8	MICBIAS decoupling capacitor, Refer to section "Microphone connection".	1	nF
C9, C10	External bypass capacitor, for DC blocking, Refer to section "Headphone connection (Capacitor-coupled)".	220	uF
Rhpl, Rhpr	Headphone jack pull-down resistors, Refer to section "Headphone connection (Capacitor-coupled)".	470 or 4.7K	Ohm
R	In single-ended connection, one external resistor (R) has to be used to bias the electret microphone. Refer to section "Headphone connection (Capacitor-coupled)".	2.2K ~ 4.7K	Ohm

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27 AC97/I2S/SPDIF Controller

27.1 Overview

This chapter describes the AIC (AC'97 and I^2S Controller) included in this processor.

The AIC supports the Audio Codec '97 Component Specification 2.3 for AC-link format and I2S or IIS (for inter-IC sound), a protocol defined by Philips Semiconductor. Both normal I2S and the MSB-justified I2S formats are supported by AIC.

AIC consists of buffers, status registers, control registers, serializers, and counters for transferring digitized audio between the processor's system memory and an internal I2S CODEC, an external AC97 or I2S CODEC. AIC can record digitized audio by storing the samples in system memory. For playback of digitized audio or production of synthesized audio, the AIC retrieves digitized audio samples from system memory and sends them to a CODEC through the serial connection with AC-link or I2S formats. The internal or external digital-to-analog converter in the CODEC then converts the audio samples into an analog audio waveform. The audio sample data can be stored to and retrieved from system memory either by the DMA controller or by programmed I/O.

The AC-link is a synchronous, fixed-rate serial bus interface for transferring CODEC register control and status information in addition to digital audio. Where both normal I2S and MSB-justified-I2S work with a variety of clock rates, which can be obtained either by dividing the PLL clock by two programmable dividers or from an external clock source.

For I2S systems that support the L3 control bus protocol, additional pins are required to control the external CODEC. CODECs that use an L3 control bus require 3 signals: L3_CLK, L3_DATA, and L3_MODE for writing bytes into the L3 bus register. The AIC supports the L3 bus protocol via software control of the general-purpose I/O (GPIO) pins. The AIC does not provide hardware control for the L3 bus protocol.

To control the internal CODEC, internal CODEC Spec can be referenced.

SPDIF (Sony/Philips Digital Interconnect Format) is a digital audio interface. The transmission medium can be either electrical or optical. Supports IEC60958 two-channel PCM audio and IEC61937 multi-channel compressed audio (Dolby Digital, DTS, etc.).

This chapter describes the programming model for the AIC. The information in this chapter requires an understanding of the AC'97 specification, Revision 2.3.

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27.1.1 Block Diagram

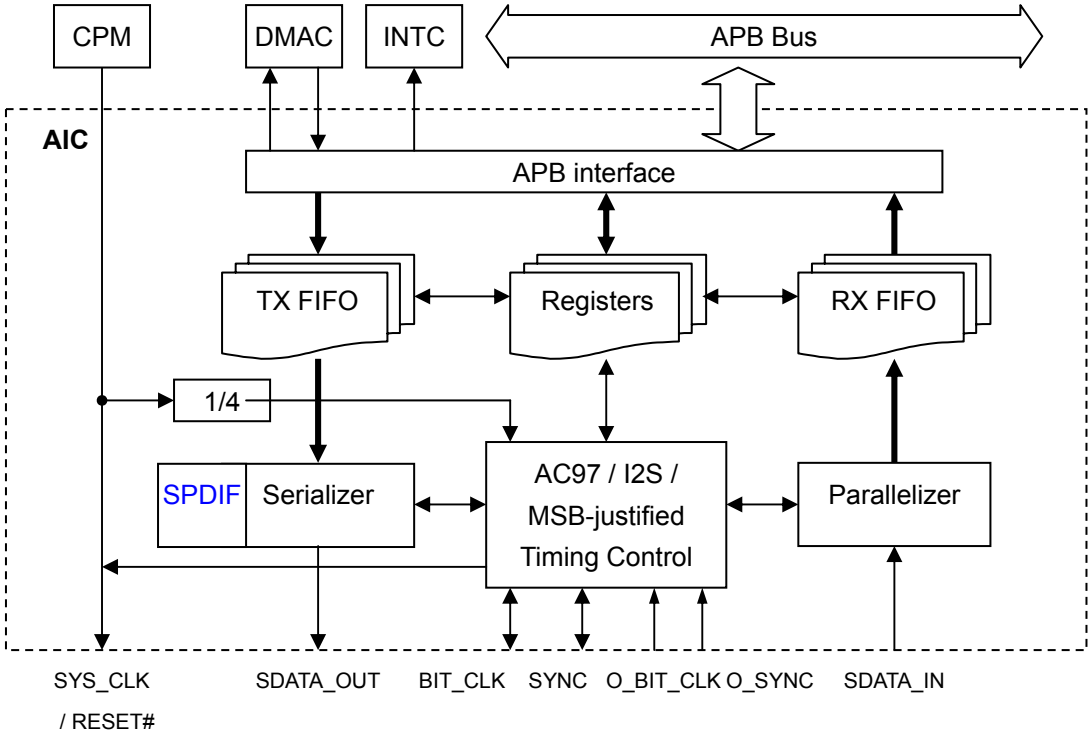


Figure 27-1 AIC Block Diagram

The O_BIT_CLK and O_SYNC ports are only used by inter CODEC.

27.1.2 Features

AIC support following AC97/I2S/SPDIF features:

AC-link (AC97) features

- Up to 20 bit audio sample data sizes supported
- DMA transfer mode supported
- Stop serial clock supported
- Programmable Interrupt function supported
- Support mono PCM data to stereo PCM data expansion on audio play back
- Support endian switch on 16-bits normal audio samples play back
- Support variable sample rate in AC-link format
- Multiple channel output and double rated supported for AC-link format
- Power Down Mode and two Wake-Up modes Supported for AC-link format

I2S features

- 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
- Up to 8 channels sample data supported

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- DMA transfer mode supported
- Stop serial clock supported
- Programmable Interrupt function supported
- Support mono PCM data to stereo PCM data expansion on audio play back
- Support endian switch on 16-bits normal audio samples play back
- Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
- Internal I2S CODEC supported
- Two FIFOs for transmit and receive respectively

SPDIF features

- 8, 16, 18, 20 and 24 bit audio sample data sizes supported
- DMA transfer mode supported
- Stop serial clock supported
- Programmable Interrupt function supported
- Support IEC60958 two-channel PCM audio
- Support IEC61937 multi-channel compressed audio
- Support consumer mode and only support transmitter mode
- Profession mode is not supported
- The User data bit is ‘0’as it is not supported in the chip
- Support sampling frequency from 32kHz to 192kHz

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27.1.3 Interface Diagram

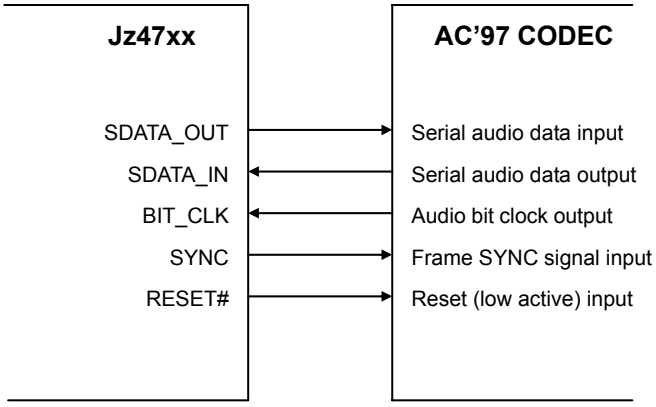


Figure 27-2 Interface to an External AC'97 CODEC Diagram

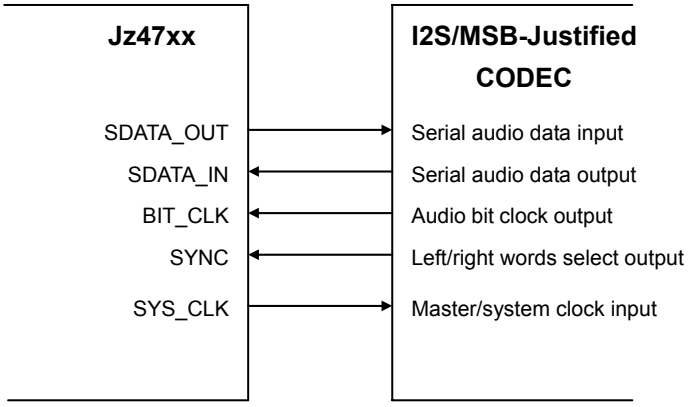


Figure 27-3 Interface to an External Master Mode I2S/MSB-Justified CODEC Diagram

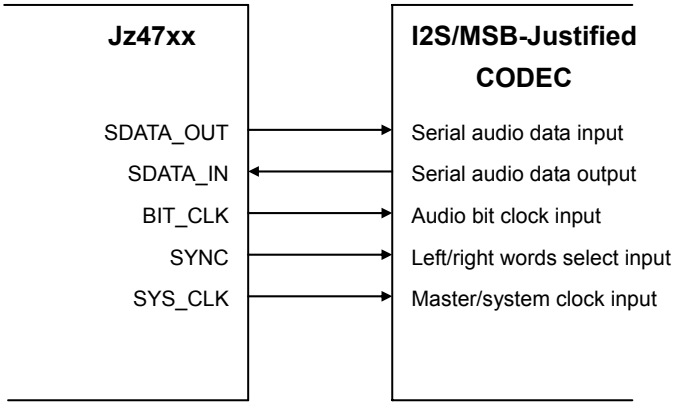


Figure 27-4 Interface to an External Slave Mode I2S/MSB-Justified CODEC Diagram

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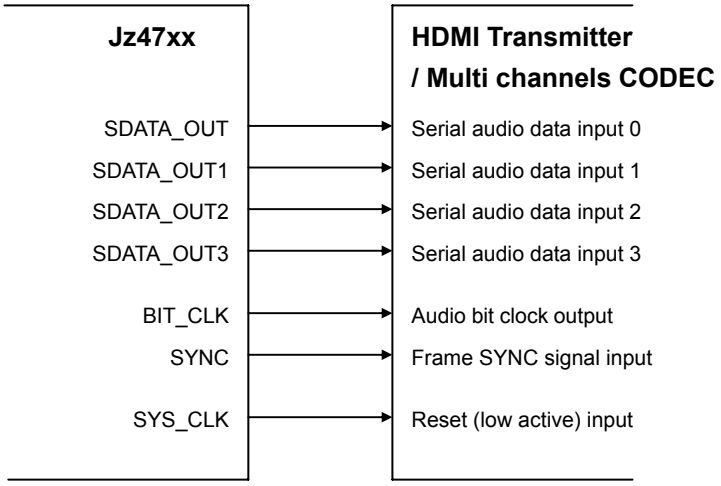


Figure 27-5 Interface to a HDMI Transmitter via I2S Diagram

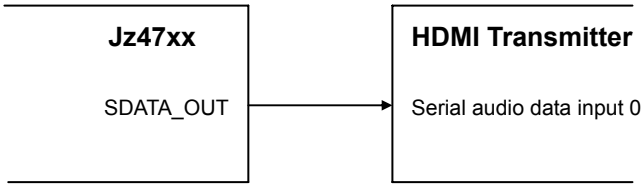


Figure 27-6 Interface to a HDMI Transmitter via SPDIF Diagram

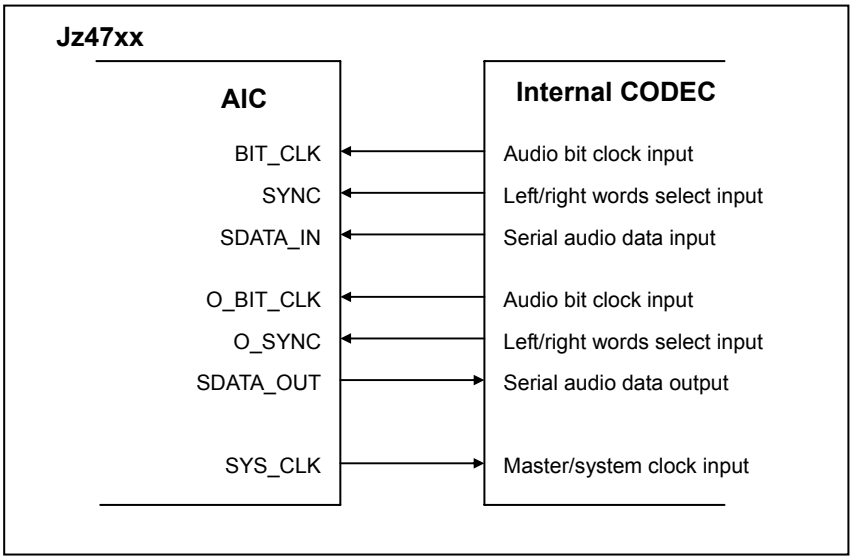


Figure 27-7 Interface to an internal Master Mode I2S CODEC Diagram

Please refer to the related CODEC specification for the details.

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27.1.4 Signal Descriptions

There are all 5 pins used to connect between AIC and an external audio CODEC device. If an internal CODEC is used, these pins are not needed. Please refer to Chip Spec. They are listed and described in Table 27-1.

Table 27-1 AIC Pins Description

Function Name	PIN Name	I/O	Description
RESET# **SYS_CLK**	SCLK_RSTN	O	RESET#: AC-link format, active-low CODEC reset. SYS_CLK: I2S/MSB-Justified formats, supply system clock to CODEC.
IBIT_CLK	BCLK_AD	I/O	Sample rate dependent bit-rate clock input/output for I2S/MSB-Jistified, only input AD channel.
ISYNC	SYNC_AD	O	48-kHz frame indicator and synchronizer for AC-link format, only input AD channel.
SDATA_IN	SDATI	I	Serial audio input data from CODEC.
BIT_CLK	BCLK	I I/O	12.288 MHz bit-rate clock input for AC-link, and sample rate dependent bit-rate clock input/output for I2S/MSB-Jistified.
SYNC	SYNC	O	48-kHz frame indicator and synchronizer for AC-link format.
		I/O	Indicates the left- or right-channel for I2S/MSB-Justified format.
SDATA_OUT	SDATO	O	Serial audio output data to CODEC / I2S line 0 / SPDIF output.
SDATA_OUT1	SDATO1	O	Serial audio output data I2S line 1.
SDATA_OUT2	SDATO2	O	Serial audio output data I2S line 2.
SDATA_OUT3	SDATO3	O	Serial audio output data I2S line 3.

The O_BIT_CLK and O_SYNC signals are not connected to any pin for only using by internal CODEC.

27.1.4.1 RESET# / SYS_CLK Pin

RESET# is AC97 active-low CODEC reset, which outputs to CODEC. The CODEC's registers are reset when this RESET# is asserted. This pin is useful only in AC-link format. If AIC is disabled, it retains the high.

SYS_CLK outputs the system clock to CODEC. This pin is useful only in I2S/MSB-justified format. It generates a frequency between approximately 2.048 MHz and 24.576 MHz by dividing down the PLL clock with a programmable divisor. This frequency can be 256, 384, 512 and etc. times of the audio sampling frequency. Or it can be set to a wanted frequency. If AIC is disabled, it retains the high.

27.1.4.2 BIT_CLK Pin

BIT_CLK is the serial data bit rate clock, at which AC97/I2S data moves between the CODEC and the processor. One bit of the serial data is transmitted or received each BIT_CLK period. It is fixed to

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12.288 MHz in AC-link format, which inputs from the CODEC. In I2S and MSB-justified format it inputs from the CODEC in slave mode and outputs to CODEC in master mode. In the master mode, the clock is generated internally that is 64 times the sampling frequency. Table 27-7 lists the available sampling frequencies based on an internal clock source. If AIC is disabled, AICFR.AUSEL and AICFR.BCKD determine the direction. And it retains the low if it is output and the state is undefined if it is input.

The IBIT_CLK is for the SDATA_IN signal on division CLOCK function.

27.1.4.3 SYNC Pin

In AC-link format, SYNC provides frame synchronization, fixed to 48kHz, by specifying beginning of an audio sample frame and outputs to CODEC. In I2S/MSB-Justified formats, SYNC is used to indicate left- or right-channel sample data and toggled in sample rate frequency. It outputs to CODEC in master mode and inputs from CODEC in slave mode. If AIC is disabled, AICFR.AUSEL and AICFR.BCKD determine the direction. And it retains the low if it is output and the state is undefined if it is input.

The ISYNC is for the SDATA_IN signal on division CLOCK function.

27.1.4.4 SDATA_OUT Pin

SDATA_OUT is AIC output data pin, which outputs AC97/I2S serial audio data, SPDIF serial data or data of AC97 CODEC register control to an external audio CODEC device.
If in multi channels mode, it outputs the first two channels serial data.
If AIC is disabled, it retains the low.

SDATA_OUTn (n = 1,2,3) is AIC output data pin, which outputs multi channels serial audio data.

27.1.4.5 SDATA_IN Pin

SDATA_IN is AIC inputs data pin, which inputs serial audio data or data of AC97 CODEC register status from an external audio CODEC device. If AIC is disabled, its state is undefined.

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27.2 Register Descriptions

AIC software interface includes 13 registers and 1 FIFO data port. They are mapped in IO memory address space so that program can access them to control the operation of AIC and the outside CODEC.

Table 27-2 AIC Registers Description

Name	Description	RW	Reset value	Address	Size
AICFR	AIC Configuration Register	RW	0x07100000	0x10020000	32
AICCR	AIC Common Control Register	RW	0x01240000	0x10020004	32
ACCR1	AIC AC-link Control Register 1	RW	0x00000000	0x10020008	32
ACCR2	AIC AC-link Control Register 2	RW	0x00000000	0x1002000C	32
I2SCR	AIC I2S/MSB-justified Control Register	RW	0x00000000	0x10020010	32
AICSR	AIC FIFO Status Register	RW	0x00000008	0x10020014	32
ACSR	AIC AC-link Status Register	RW	0x00000000	0x10020018	32
I2SSR	AIC I2S/MSB-justified Status Register	RW	0x00000000	0x1002001C	32
ACCAR	AIC AC97 CODEC Command Address Register	RW	0x00000000	0x10020020	32
ACCDR	AIC AC97 CODEC Command Data Register	RW	0x00000000	0x10020024	32
ACSAR	AIC AC97 CODEC Status Address Register	R	0x00000000	0x10020028	32
ACSDR	AIC AC97 CODEC Status Data Register	R	0x00000000	0x1002002C	32
I2SDIV	AIC I2S/MSB-justified Clock Divider Register	RW	0x00000003	0x10020030	32
AICDR	AIC FIFO Data Port Register	RW	0x????????	0x10020034	32
SPENA	SPDIF Enable Register	RW	0x00	0x10020080	8
SPCTRL	SPDIF Control Register	RW	0x0003	0x10020084	16
SPSTATE	SPDIF Status Register	RW	0x0000	0x10020088	16
SPCFG1	SPDIF Configure 1 Register	RW	0x00000000	0x1002008C	32
SPCFG2	SPDIF Configure 2 Register	RW	0x00000000	0x10020090	32
SPFIFO	SPDIF FIFO Register	W	0x????????	0x10020094	32
CKCFG	Clock Configure for the embedded CODEC to AIC	RW	0x00000000 0x00000002	0x100200A0	32
RGADW	Address, data in and write command for accessing to internal registers of embedded CODEC	RW	0x00000000	0x100200A4	32
RGDATA	The read out data and interrupt request status of Internal registers	R	0x00000000	0x100200A8	32

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	data in the embedded CODEC				

1 AICFR is used to control FIFO threshold, AC-link or I2S/MSB-justified selection, AIC reset, master/slave selection, and AIC enable.
2 AICCR is used to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.
3 ACCR1 is used to reflect/control valid incoming/outgoing slots of AC97.
4 ACCR2 is used to control interrupt enable, output/input sample size, and alternative control of RESET#, SYNC and SDATA_OUT pins in AC-link.
5 I2SCR is used to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified.
6 AICSR is used to reflect FIFOs status.
7 ACSR is used to reflect the status of the connected external CODEC in AC-link.
8 I2SSR is used to reflect AIC status in I2S/MSB-justified.
9 ACCAR and ACCDR are used to hold address and data for AC-link CODEC register read/write.
10 ACSAR and ACSDR are used to receive AC-link CODEC registers address and data.
11 I2SDIV is used to set clock divider for BIT_CLK generating in I2S/MSB-justified format.
12 AICDR is act as data input/output port to/from transmit/receive FIFO when write/read.
13 CKCFG, RGADW and RGDATA are used to access internal CODEC, please refer to CODEC Spec.

27.2.1 AIC Configuration Register (AICFR)

AICFR contains bits to control FIFO threshold, AC-link or I2S/MSB-justified selection, AIC reset, master/slave selection, and AIC enable.

AICFR **0x10020000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				RFTH				Reserved			TFTH					Reserved						IBCKD	ISYNCD	DMODE	Reserved	LSMP	ICDC	AUSEL	RST	BCKD	SYNCD	ENB
RST	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:24	RFTH	Receive FIFO threshold for interrupt or DMA request. The RFTH valid value is 0 ~ 15. This value represents a threshold value of (RFTH + 1) * 2. When the sample number in receive FIFO, indicated by AICSR.RFL, is great than or equal to the threshold value, AICSR.RFS is set. Larger RFTH value provides lower DMA/interrupt request frequency but have more risk to	RW

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<table>
<tr><td></td><td></td><td>involve receive FIFO overflow. The optimum value is system dependent.</td><td></td></tr>
<tr><td>23:21</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>20:16</td><td>TFTH</td><td>Transmit FIFO threshold for interrupt or DMA request. The TFTH valid value 0 ~ 31.
This value represents a threshold value of TFTH * 2. When the sample number in transmit FIFO, indicated by AICSR.TFL, is less than or equal to the threshold value, AICSR.TFS is set. Smaller TFTH value provides lower DMA/interrupt request frequency but have more risk to involve transmit FIFO underflow. The optimum value is system dependent.</td><td>RW</td></tr>
<tr><td>15:11</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>10</td><td>IBCKD</td><td>The IBIT_CLK Direction. This bit specifies input/output direction of BIT_CLK. It is only valid in I2S/MSB-justified format. When AC-link format is selected, BIT_CLK is always input and this bit is ignored. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).
This is only available when DMODE = 1.
<table>
<tr><th>BCKD</th><th>BIT_CLK Direction</th></tr>
<tr><td>0</td><td>BIT_CLK is input from an external source.</td></tr>
<tr><td>1</td><td>BIT_CLK is generated internally and driven out to the CODEC.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>9</td><td>ISYNCD</td><td>ISYNC Direction. This bit specifies input/output direction of SYNC in I2S/MSB-justified format. When AC-link format is selected, SYNC is always output and this bit is ignored. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).
This is only available when DMODE = 1.
<table>
<tr><th>SYNCD</th><th>SYNC Direction</th></tr>
<tr><td>0</td><td>SYNC is input from an external source.</td></tr>
<tr><td>1</td><td>SYNC is generated internally and driven out to the CODEC.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>8</td><td>DMODE</td><td>The Division Clock Mode control.
<table>
<tr><th>BCKD</th><th>BIT_CLK Direction</th></tr>
<tr><td>0</td><td>Disable. Shared clock mode.
The BIT_CLK, SYNC, SDATA_IN and SDATA_OUT are configured to one two direction shared clock I2S channel.</td></tr>
<tr><td>1</td><td>Enable. Spilt clock mode.
The BIT_CLK, SYNC and SDATA_OUT are configured to one output I2S channel.
The IBIT_CLK, ISYNC and SDATA_IN are configured to one input I2S channel.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>7</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>6</td><td>LSMP</td><td>Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better</td><td>RW</td></tr>
</table>

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<table>
<tr><td></td><td></td><td>be changed while audio replay is stopped.<table><tr><th>LSMP</th><th>CODEC used</th></tr><tr><td>0</td><td>Play ZERO sample when TX FIFO underflow.</td></tr><tr><td>1</td><td>Play last sample when TX FIFO underflow.</td></tr></table></td><td></td></tr>
<tr><td>5</td><td>ICDC</td><td>Internal CODEC used. Select between internal or external CODEC.<table><tr><th>ICDC</th><th>CODEC used</th></tr><tr><td>0</td><td>External CODEC.</td></tr><tr><td>1</td><td>Internal CODEC.</td></tr></table></td><td>RW</td></tr>
<tr><td>4</td><td>AUSEL</td><td>Audio Unit Select. Select between AC-link and I2S/MSB-justified. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).<table><tr><th>AUSEL</th><th>Selected</th></tr><tr><td>0</td><td>Select AC-link format.</td></tr><tr><td>1</td><td>Select I2S/MSB-justified format.</td></tr></table></td><td>RW</td></tr>
<tr><td>3</td><td>RST</td><td>Reset AIC. Write 1 to this bit reset AIC registers and FIFOs except AICFR and I2SDIV register. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>2</td><td>BCKD</td><td>BIT_CLK Direction. This bit specifies input/output direction of BIT_CLK. It is only valid in I2S/MSB-justified format. When AC-link format is selected, BIT_CLK is always input and this bit is ignored. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).<table><tr><th>BCKD</th><th>BIT_CLK Direction</th></tr><tr><td>0</td><td>BIT_CLK is input from an external source.</td></tr><tr><td>1</td><td>BIT_CLK is generated internally and driven out to the CODEC.</td></tr></table></td><td>RW</td></tr>
<tr><td>1</td><td>SYNCD</td><td>SYNC Direction. This bit specifies input/output direction of SYNC in I2S/MSB-justified format. When AC-link format is selected, SYNC is always output and this bit is ignored. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).<table><tr><th>SYNCD</th><th>SYNC Direction</th></tr><tr><td>0</td><td>SYNC is input from an external source.</td></tr><tr><td>1</td><td>SYNC is generated internally and driven out to the CODEC.</td></tr></table></td><td>RW</td></tr>
<tr><td>0</td><td>ENB</td><td>Enable AIC function. This bit is used to enable or disable the AIC function.<table><tr><th>ENB</th><th>Description</th></tr><tr><td>0</td><td>Disable AIC Controller.</td></tr><tr><td>1</td><td>Enable AIC Controller.</td></tr></table></td><td>RW</td></tr>
</table>

The BCKD bit (bit 2) and SYNCD bit (bit 1) configure the mode of I2S/MSB-justified interface. This is compliant with I2S specification.

BCKD	SYNCD	Description
0 (input)	**0 (input)**	**AIC roles the slave of I2S/MSB-justified interface.**

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	1 (output)	**AIC roles the master with external serial clock source of I2S/MSB-justified interface.**
1 (output)	**0 (input)**	**Reserved.**
	1 (output)	**AIC roles the master of I2S/MSB-justified interface.**

27.2.2 AIC Common Control Register (AICCR)

AICCR contains bits to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.

AICCR **0x10020004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		Reserved	PACK16	Reserved	CHANNEL			Reserved		OSS			ISS			RDMS	TDMS	Reserved		M2S	ENDSW	ASVTSU	TFLUSH	RFLUSH	EROR	ETUR	ERFS	ETFS	ENLBF	ERPL	EREC
RST	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29	Reserved	Keep this value to 0 in normal use.	R
28	PACK16	Output Sample data 16bit packed mode select. This bit reflects that one word contains two sample data or only one sample data with LSB align. The packed mode is only support 16bit sample size. **PACK16** / **Sample Size** 0: Unpacked data mode. One word only contains one 16bit sample data aligned LSB. 1: Packed data mode. One word contains two 16 bit sample data.	RW
27	Reserved	Writing has no effect, read as zero.	R
26:24	CHANNEL	Output Channel Number Select. These bits reflect output data channels from AIC to device. The data supported are: 1(mono), 2(stereo), 4, 6 and 8 channels. The sample data is LSB-justified in memory/register. **CHANNEL** / **Sample Size** 0x0: 1 channel, mono, Only SDATA0 used. 0x1: 2 channels, stereo, Only SDATA0 used. 0x2: Reserved. 0x3: 4 channels, SDATA0 and SDATA1 used.	RW

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			0x4	Reserved.
			0x5	6 channels, SDATA0 to SDATA2 used.
			0x6	Reserved.
			0x7	8 channels, , SDATA0 to SDATA3 used.
23:22	Reserved	Writing has no effect, read as zero.		R
21:19	OSS	Output Sample Size. These bits reflect output sample data size from memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.		RW
		OSS	**Sample Size**	
		0x0	8 bit.	
		0x1	16 bit.	
		0x2	18 bit.	
		0x3	20 bit.	
		0x4	24 bit.	
		0x5~0x7	Reserved.	
18:16	ISS	Input Sample Size. These bits reflect input sample data size to memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.		RW
		ISS	**Sample Size**	
		0x0	8 bit.	
		0x1	16 bit.	
		0x2	18 bit.	
		0x3	20 bit.	
		0x4	24 bit.	
		0x5~0x7	Reserved.	
15	RDMS	Receive DMA enable. This bit is used to enable or disable the DMA during receiving audio data.		RW
		RDMS	**Receive DMA**	
		0	**Disabled.**	
		1	**Enabled.**	
14	TDMS	Transmit DMA enable. This bit is used to enable or disable the DMA during transmit audio data.		RW
		TDMS	**Transmit DMA**	
		0	**Disabled.**	
		1	**Enabled.**	
13:12	Reserved	Writing has no effect, read as zero.		R
11	M2S	Mono To Stereo. This bit control whether to do mono to stereo sample expansion in play back. When this bit is set, every outgoing sample data in the steam plays in both left and right channels. This bit should only be set in 2 channels configuration. It takes effective immediately when the bit is changed. Change this before replay started.		RW
		M2S	**Description**	

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			0 **No mono to stereo expansion.** 1 **Do mono to stereo expansion.**	
10	ENDSW	Endian Switch. This bit control endian change on outgoing 16-bits size audio sample by swapping high and low bytes in the sample data. **ENDSW** / **Description** 0 **No change on outgoing sample data.** 1 **Swap high and low byte for outgoing 16-bits size sample data.**		RW
9	ASVTSU	Audio Sample Value Transfer between Signed and Unsigned data format. This bit is used to control the signed ←→unsigned data transfer. If it is 1, the incoming and outgoing audio sample data will be transferred by toggle its most significant bit. **ASVTSU** / **Description** 0 **No audio sample value signed ←→unsigned transfer.** 1 **Do audio sample value signed ←→unsigned transfer.**		RW
8	TFLUSH	Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.		W
7	RFLUSH	Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.		W
6	EROR	Enable ROR Interrupt. This bit is used to control the ROR interrupt enable or disable. **EROR** / **ROR Interrupt** 0 **Disabled.** 1 **Enabled.**		RW
5	ETUR	Enable TUR Interrupt. This bit is used to control the TUR interrupt enable or disable. **ETUR** / **TUR Interrupt** 0 **Disabled.** 1 **Enabled.**		RW
4	ERFS	Enable RFS Interrupt. This bit is used to control the RFS interrupt enable or disable. **ERFS** / **RFS Interrupt** 0 **Disabled.** 1 **Enabled.**		RW
3	ETFS	Enable TFS Interrupt. This bit is used to control the TFS interrupt enable or disable. **ETFS** / **TFS Interrupt**		RW

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			0 **Disabled.** 1 **Enabled.**	
2	ENLBF	Enable AIC Loop Back Function. This bit is used to enable or disable the internal loop back function of AIC, which is used for test only. When the AIC loop back function is enabled, normal audio replay/record functions are disabled. **ENLBF** / **Description** 0 AIC Loop Back Function is Disabled. 1 AIC Loop Back Function is Enabled.		RW
1	ERPL	Enable Playing Back function. This bit is used to disable or enable the audio sample data transmitting. **ERPL** / **Description** 0 **AIC Playing Back Function is Disabled.** 1 **AIC Playing Back Function is Enabled.**		RW
0	EREC	Enable Recording Function. This bit is used to disable or enable the audio sample data receiving. **EREC** / **Description** 0 **AIC Recording Function is Disabled.** 1 **AIC Recording Function is Enabled.**		RW

27.2.3 AIC AC-link Control Register 1 (ACCR1)

ACCR1 contains bits to reflect/control valid incoming/outgoing slots of AC97. It is used only in AC-link format.

ACCR1 **0x10020008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						RS										Reserved						XS									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	RS	Receive Valid Slots. These bits are used to indicate which incoming slots are valid. Slot 3 is mapped to bit 16 or RS[0], slot 4 to bit 17 or RS[1] and so on. When write to this field, a bit 1 means we expect a PCM data in the corresponding slot, a bit 0 means the corresponding slot PCM data will be discarded. When read from this field, a bit 1 means we receive an expected valid PCM data in the corresponding slot. This field should be written before record started. **RS[n] Value** / **Description** 0 **Slot n+3 is invalid.**	RW

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			1	**Slot n+3 has valid PCM data.**	
15:10	Reserved	Writing has no effect, read as zero.			R
9:0	XS	Transmit Valid Slots. These bits making up slots map to the valid bits in the AC'97 tag (slot 0 on SDATA_OUT) and indicate which outgoing slots have valid PCM data. Bit 0 or XS[0] maps to slot 3, bit 1 or XS[1] to slot 4 and so on. Setting the corresponding bit indicates to AIC to take an audio sample from transmit FIFO to fill the respective slot. And it indicates to the CODEC that valid PCM data will be in the respective slot. The number of valid bits will designate how many words will be pulled out of the FIFO per audio frame. This field should be written before record and replay started.			RW

XS[n] Value	Description
0	**Slot n+3 is invalid.**
1	**Slot n+3 has valid PCM data.**

27.2.4 AIC AC-link Control Register 2 (ACCR2)

ACCR2 contains bits to control interrupt enable, output/input sample size, and alternative control of RESET#, SYNC and SDATA_OUT pins in AC-link. It is valid only in AC-link format.

ACCR2 **0x1002000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													ERSTO	ESADR	ECADT	Reserved												SO	SR	SS	SA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	ERSTO	Enable RSTO Interrupt. This bit is used to control the RSTO interrupt enable or disable.	RW
17	ESADR	Enable SADR Interrupt. This bit is used to control the SADR interrupt enable or disable.	RW
16	ECADT	Enable CADT Interrupt. This bit is used to control the CADT interrupt enable or disable.	RW

ERSTO	RSTO Interrupt
0	**Disabled.**
1	**Enabled.**

ESADR	SADR Interrupt
0	**Disabled.**
1	**Enabled.**

ECADT	CADT Interrupt

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			0	**Disabled.**
			1	**Enabled.**
15:4	Reserved	Writing has no effect, read as zero.		R
3	SO	SDATA_OUT output value. When SA is 1, this bit controls SDATA_OUT pin voltage level, 0 for low, 1 for high; otherwise, it is ignored.		RW
2	SR	RESET# pin level. When AC-link is selected, this bit is used to drive the RESET# pin.		RW

SR	RESET# Pin Voltage Level
0	High.
1	Low.

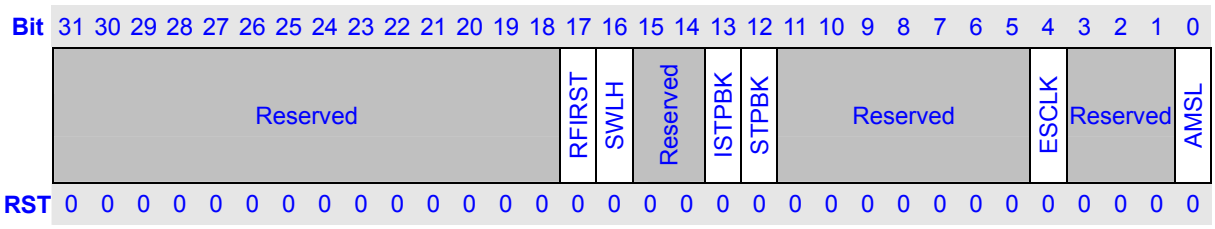
1	SS	SYNC value. When this bit is read, it returns the actual value of SYNC. When SA is 1, write value controls SYNC pin value. When SA is 0, write to it is ignored.	RW
0	SA	SYNC and SDATA_OUT Alternation. This bit is used to determine the driven signal of SYNC and SDATA_OUT. When SA is 0, SYNC and SDATA_OUT being driven AIC function logic; otherwise, SYNC is controlled by the SS and SDATA_OUT is controlled by the SO. The true table of SYNC is described in following.	RW

SA	SS	Description
0	0	When read, indicated SYNC is 0.
		When write, not effect.
	1	When read, indicated SYNC is 1.
		When write, not effect.
1	0	When read, indicated SYNC is 0.
		When write, SYNC is driven to 0.
	1	When read, indicated SYNC is 1.
		When write, SYNC is driven to 1.

27.2.5 AIC I2S/MSB-justified Control Register (I2SCR)

I2SCR contains bits to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified. It is valid only in I2S/MSB-justified format.

I2SCR **0x10020010**



Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R

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<table>
<tr><td>17</td><td>RFIRST</td><td>Send R channel first in stereo mode. This bit should only be set in 2 channels configuration. The frame is LR like or RL like. It takes effective immediately when the bit is changed.
Change this before replay started.
<table><tr><th>RFIRST</th><th>Description</th></tr><tr><td>0</td><td>Send L channel first. (LR)</td></tr><tr><td>1</td><td>Send R channel first. (RL)</td></tr></table></td><td>RW</td></tr>
<tr><td>16</td><td>SWLH</td><td>Switch LR channel in 16bit-packed stereo mode.
This bit control whether the low address data is L or R. This bit should only be set in 2 channels configuration and 16bit-packed mode. That means it can only valid with packed mode (PACK16 =1) and 2 channels (CHANNEL=0x1).
It takes effective immediately when the bit is changed. Change this before replay started.
<table><tr><th>SWLH</th><th>Description</th></tr><tr><td>0</td><td>16 bit LSB and 16bit MSB is not switched.</td></tr><tr><td>1</td><td>16 bit LSB and 16bit MSB is switched.</td></tr></table></td><td>RW</td></tr>
<tr><td>15:12</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>13</td><td>ISTPBK</td><td>Stop BIT_CLK. It is used to stop the BIT_CLK in I2S/MSB-justified format. When AC-link is selected, all of its operations are ignored.
<table><tr><th>STPBK</th><th>Description</th></tr><tr><td>0</td><td>BIT_CLK is not stopped.</td></tr><tr><td>1</td><td>BIT_CLK is stopped.</td></tr></table>
Please set this bit to 1 to stop BIT_CLK when change AICFR.AUSEL and AICFR.BCKD.</td><td>RW</td></tr>
<tr><td>12</td><td>STPBK</td><td>Stop BIT_CLK. It is used to stop the BIT_CLK in I2S/MSB-justified format. When AC-link is selected, all of its operations are ignored.
<table><tr><th>STPBK</th><th>Description</th></tr><tr><td>0</td><td>BIT_CLK is not stopped.</td></tr><tr><td>1</td><td>BIT_CLK is stopped.</td></tr></table>
Please set this bit to 1 to stop BIT_CLK when change AICFR.AUSEL and AICFR.BCKD.</td><td>RW</td></tr>
<tr><td>11:5</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>4</td><td>ESCLK</td><td>Enable SYSCLK output. When this bit is 1, the SYSCLK outputs to chip outside is enabled. Else, the clock is disabled.</td><td>RW</td></tr>
<tr><td>3:1</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>0</td><td>AMSL</td><td>Specify Alternate Mode (I2S or MSB-Justified) Operation.
<table><tr><th>AMSL</th><th>Description</th></tr></table></td><td>RW</td></tr>
</table>

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			0	Select I2S Operation Mode.		
			1	Select MSB-Justified Operation Mode.		

27.2.6 AIC Controller FIFO Status Register (AICSR)

AICSR contains bits to reflect FIFOs status. Most of the bits are read-only except two, which can be written a 0.

AICSR **0x10020014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				RFL				Reserved										TFL						Reserved	ROR	TUR	RFS	TFS	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	RFL	Receive FIFO Level. The bits indicate the amount of valid PCM data in Receive FIFO. RFL Value / Description: 0x00 ~ 0x20: RFL valid PCM data in receive FIFO. 0x21 ~ 0x3F: Reserved.	R
23:14	Reserved	Writing has no effect, read as zero.	R
13:8	TFL	Transmit FIFO Level. The bits indicate the amount of valid PCM data in Transmit FIFO. TFL Value / Description: 0x00 ~ 0x20: TFL valid PCM data in transmit FIFO. 0x21 ~ 0x3F: Reserved.	R
7	Reserved	Writing has no effect, read as zero.	R
6	ROR	Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. ROR / Description: 0: When read, indicates over-run has not been found. When write, clear itself. 1: When read, indicates data has even been written to full receive FIFO. When write, not effects.	RW
5	TUR	Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. TUR / Description: 0: When read, indicates under-run has not been found. When write, clear itself.	RW

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		1	When read, indicates data has even been read from empty transmit FIFO. When write, not effects.	
4	RFS	Receive FIFO Service Request. This bit indicates that receive FIFO level is or not below receive FIFO threshold, which is controlled by AICFR.RFTH. When RFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting. **RFS** / **Description** 0 / Receive FIFO level below RFL threshold. 1 / Receive FIFO level at or above RFL threshold.		R
3	TFS	Transmit FIFO Service Request. This bit indicates that transmit FIFO level is below Transmit FIFO threshold, which is controlled by AICFR.TFTH. When TFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting. **TFS** / **Description** 0 / Transmit FIFO level exceeds TFL threshold. 1 / Transmit FIFO level at or below TFL threshold.		R
2:0	Reserved	Writing has no effect, read as zero.		R

27.2.7 AIC AC-link Status Register (ACSR)

ACSR contains bits to reflect the status of the connected external CODEC in AC-link format. Bits in this register are read-only in general, except some of them can be written a 0.

ACSR **0x10020018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SLTERR	CRDY	CLPM	RSTO	SADR	CADT	Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
21	SLTERR	Hardware detects a Slot Error. This bit indicates an error in SLOTREQ bits on incoming data from external CODEC is detected. The error can be: (1) find 1 in a SLOTREQ bit, which corresponding to an inactive slot; (2) all active slots should be request in the same time by SLOTREQ, but an exception is found. All errors are accumulated to ACSR.SLTERR by hardware until software clears it. Software writes 0 clear this bit and write 1 has no effect.	RW
20	CRDY	External CODEC Ready. This bit is derived from the CODEC Ready bit of Slot 0 in SDATA_IN, and it indicates the external AC97 CODEC is ready or not.	R

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		CRDY: 0 — CODEC is not ready. CRDY: 1 — CODEC is ready.	
19	CLPM	External CODEC Low Power Mode. This bit indicates the external CODEC is switched to low power mode or BIT_CLK is active from CODEC after wake up. CLPM: 0 — BIT_CLK is active. CLPM: 1 — CODEC is switched to low power mode.	R
18	RSTO	External CODEC Registers Read Status Time Out. This bit indicates that the read status time out is detected or not. It is set to 1 if the data not return in 4 frames after a CODEC registers read command issued. RSTO: 0 — When read, indicates time out has not occurred. RSTO: 1 — When read, indicates read status time out found. Write 0 clear this bit and write 1 is ignored. When RSTO is 1, it may trigger an interrupt depends on the interrupt enable setting.	RW
17	SADR	External CODEC Registers Status Address and Data Received. This bit indicates that address and data of an external AC '97 CODEC register has or has not been received. SADR: 0 — When read, indicates no register address/data received. SADR: 1 — When read, indicates address/data received. Write 0 clear this bit and write 1 is ignored. When SADR is 1, it may trigger an interrupt depends on the interrupt enable setting.	RW
16	CADT	Command Address and Data Transmitted. This bit indicates that a CODEC register reading/writing command transmission has completed or not. CADT: 0 — When read, indicates the command has not done. CADT: 1 — When read, indicates the command has done. Write 0 clear this bit and write 1 is ignored. When CADT is 1, it may trigger an interrupt depends on the interrupt enable setting.	RW
15:0	Reserved	Writing has no effect, read as zero.	R

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27.2.8 AIC I2S/MSB-justified Status Register (I2SSR)

I2SSR is used to reflect AIC status in I2S/MSB-justified. It is a read-only register.

I2SSR 0x1002001c

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CHBSY	TBSY	RBSY	BSY	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
5	CHBSY	AIC Transmitter busy in I2S/MSB-justified format.(Multi-channel status) CHBSY: 0 – AIC Transmitter part is idle or disabled. CHBSY: 1 – AIC Transmitter part currently is transmitting or receiving a frame.	R
4	TBSY	AIC Transmitter busy in I2S/MSB-justified format. TBSY: 0 – AIC Transmitter part is idle or disabled. TBSY: 1 – AIC Transmitter part currently is transmitting or receiving a frame.	R
3	RBSY	AIC Receiver busy in I2S/MSB-justified format. RBSY: 0 – AIC Receiver part is idle or disabled. RBSY: 1 – AIC Receiver part currently is transmitting or receiving a frame.	R
2	BSY	AIC busy in I2S/MSB-justified format. BSY: 0 – AIC controller is idle or disabled. BSY: 1 – AIC controller currently is transmitting or receiving a frame.	R
1:0	Reserved	Writing has no effect, read as zero.	R

27.2.9 AIC AC97 CODEC Command Address & Data Register (ACCAR, ACCDR)

ACCAR and ACCDR are used to hold register address and data for external AC-link CODEC register read/write operation through SDATA_OUT. The format of ACCAR.CAR and ACCDR.CDR is compliant with AC'97 Component Specification 2.3 where ACCAR.CAR[19] of "1" specifies CODEC register read operation, of "0" specifies CODEC register write operation. The write access to ACCAR and ACCDR signals AIC to issue this operation. Please reference to 27.4.4 for software flow. These registers are valid only in AC-link. It is ignored in I2S/MSB-justified format.

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ACCAR **0x10020020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												CAR																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	CAR	Command Address Register. This is used to hold 20-bit AC '97 CODEC register address transmitted in SDATA_OUT slot 1. After this field is write, it should not be write again until the operation is finished.	RW

ACCDR **0x10020024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												CDR																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	CDR	Command Data Register. This is used to hold 20-bit AC'97 CODEC register data transmitted in SDATA_OUT slot 2. After this field is write, it should not be write again until the operation is finished.	RW

27.2.10 AIC AC97 CODEC Status Address & Data Register (ACSAR, ACSDR)

ACSAR and ACSDR are used to receive the external AC-link CODEC registers address and data from SDATA_IN. When AIC receives CODEC register status from SDATA_IN, it set ACSR.SADR bit and put the address and data to ACSAR.SAR and ACSDR.SDR. Please reference to 27.4.4 for software flow. These registers are valid only in AC-link format and are ignored in I2S/MSB-justified format.

ACSAR **0x10020028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												SAR																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	SAR	CODEC Status Address Register. This is used to receive 20-bit AC '97 CODEC status address from SDATA_IN slot 1. Which reflect the register index for which data is being returned. The write operation is ignored.	R

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ACSDR **0x1002002C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												SDR																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	SDR	CODEC Status Data Register. This is used to receive 20-bit AC ’97 CODEC status data from SDATA_IN slot 2. The register data of external CODEC is returned. The write operation is ignored.	R

27.2.11 AIC I2S/MSB-justified Clock Divider Register (I2SDIV)

I2SDIV is used to set clock divider to generated BIT_CLK from SYS_CLK in I2S/MSB-justified format.

I2SDIV **0x10020030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				IDV				Reserved				DV			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

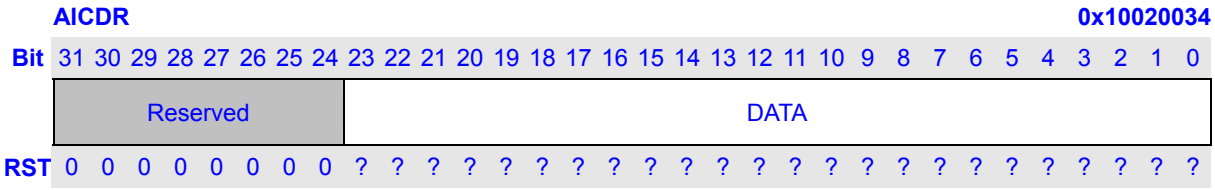
Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:8	IDV	Audio IBIT_CLK clock divider value minus 1. I2SDIV.IDV is used to control the generating of IBIT_CLK from dividing SYS_CLK. The dividing value should be even and I2SDIV.IDV should be set to the dividing value minus 1. So I2SDIV.IDV bit0 is fixed to 1. IBIT_CLK frequency is fixed to 64 f_S in AIC, where f_S is the audio sample frequency. I2SDIV.IDV depends on SYS_CLK frequency f_{SYS_CLK}, which is selected according to external CODEC’s requirement and internal PLL frequency. Please reference to 1.4.10 Serial Audio Clocks and Sampling Frequencies for further description.	RW
7:4	Reserved	Writing has no effect, read as zero.	R
3:0	DV	Audio BIT_CLK clock divider value minus 1. I2SDIV.DV is used to control the generating of BIT_CLK from dividing SYS_CLK. The dividing value should be even and I2SDIV.DV should be set to the dividing value minus 1. So I2SDIV.DV bit0 is fixed to 1. BIT_CLK frequency is fixed to 64 f_S in AIC, where f_S is the audio sample frequency. I2SDIV.DV depends on SYS_CLK frequency f_{SYS_CLK}, which is selected according to external CODEC’s requirement and internal PLL frequency. Please reference to 1.4.10 Serial Audio Clocks and Sampling Frequencies for further description.	RW

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27.2.12 AIC FIFO Data Port Register (AICDR)

AICDR is act as data input port to transmit FIFO when write and data output port from receive FIFO when read, one audio sample every time. The FIFO width is 24 bits. Audio sample with size N that is less than 24 is located in LSB N-bits. The sample size is specified by ACCR2.OASS and ACCR2.IASS in AC-link, and by I2SCR.WL in I2S/MSB-justified. The sample order is specified by ACCR1.XS and ACCR1.RS in AC-link. In I2S/MSB-justified, the left channel sample is prior to the right channel sample.

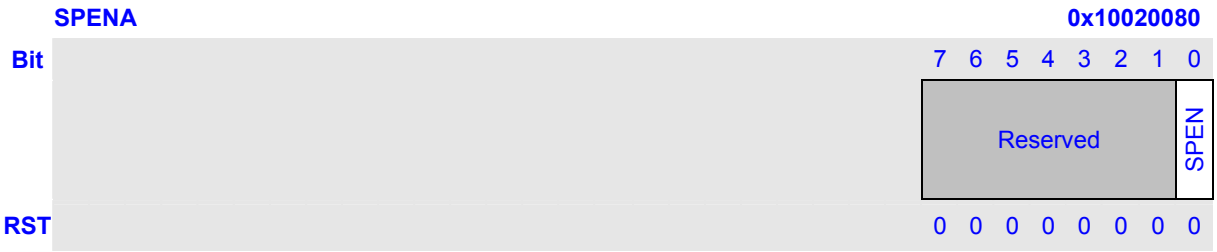
Care should be taken to monitor the status register to insure that there is room for data in the FIFO when executing a program read or write transaction. This is taken care automatically in DMA.



Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	DATA	FIFO port. When write to it, data is push to the transmit FIFO. When read from it, data is pop from the receiving FIFO.	RW

27.2.13 SPDIF Enable Register (SPENA)

The register SPENA is used to trigger SPDIF transmitter to work.



Bits	Name	Description	RW
7:1	Reserved	Writing has no effect, read as zero.	R
0	SPEN	Enable / disable the SPDIF transmitter. 0: SPDIF transmitter is disabled 1: SPDIF transmitter is enabled	RW

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27.2.14 SPDIF Control Register (SPCTRL)

The register SPCTRL is used to control SPDIF to work.

SPCTRL 0x10020084

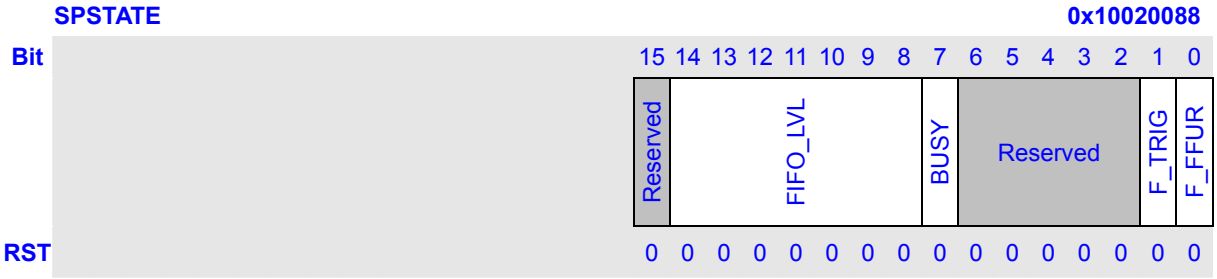
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_EN	D_TYPE	SIGN_N	INVALID	SFT_RST	SPDIF_I2S	Reserved								M_TRIG	M_FFUR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
15	DMA_EN	DMA transmitter enable bit. 0: DMA transmitter disable; 1: DMA transmitter enable.	RW
14	D_TYPE	If the bit number of data is less than16, the data in memory is as follows: 0: XXXXXXXXXXXXXXXX | Data 0 XXXXXXXXXXXXXXXX | Data 1 1: Data 1 | Data 0 Data 3 | Data 2	RW
13	SIGN_N	Signed to unsigned or not. If it is 1, the incoming and outgoing audio sample data will be transferred by toggle its most significant bit. 0: Not transfer; 1: Do transfer.	RW
12	INVALID	Data invalid bit. The data transmitted on SPDIF is valid or not. 0: Valid; 1: Invalid.	RW
11	SFT_RST	SPDIF FIFO software-reset. Set it to 1 and later it will be cleared by hardware auto. When SFT_RST returns back to 0, the FIFO finish reset. 0: Stop reset; 1: Start reset.	RW
10	SPDIF_I2S	Choose SPDIF or I2S. 0: I2S; 1: SPDIF.	
9:2	Reserved	Writing has no effect, read as zero.	R
1	M_TRIG	Trigger interrupt mask. 0: Enabled; 1: Masked.	RW
0	M_FFUR	FIFO underrun interrupt mask. 0: Enabled; 1: Masked.	RW

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27.2.15 SPDIF State Register (SPSTATE)

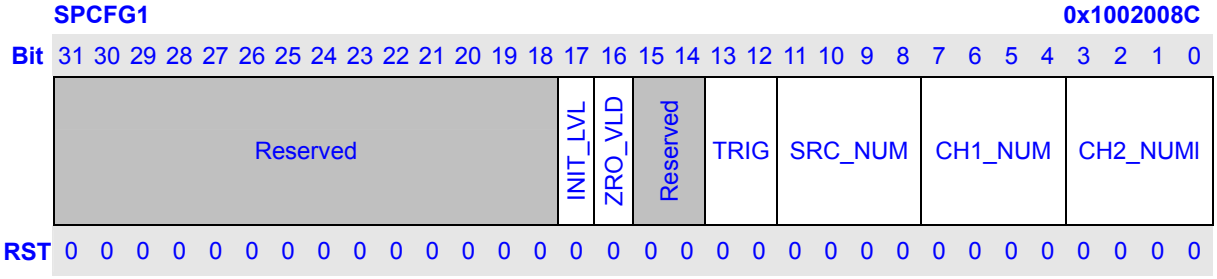
The register SPSTATE is used to keep the state of SPDIF.



Bits	Name	Description	RW
15	Reserved	Writing has no effect, read as zero.	R
14:8	FIFO_LVL	FIFO level. The bits indicate the amount of valid data in FIFO.	R
7	BUSY	SPDIF busy bit. 0: SPDIF is not working; 1: SPDIF is working.	R
6:2	Reserved	Writing has no effect, read as zero.	R
1	F_TRIG	Trigger flag. 0: Not active; 1: Active.	R
0	F_FFUR	FIFO underrun flag. 0: Not active; 1: Active.	RW

27.2.16 SPDIF Configure 1 Register (SPCFG1)

The register SPCFG1 is used to configure SPDIF.



Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	INIT_LVL	Initial level set bit. 0: SPDIF initial level is low; 1: SPDIF initial level is high.	
16	ZRO_VLD	The valid bit of channel state is 0 or 1 when play ZERO sample under FIFO underflow. 0: Valid; 1: Invalid.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:12	TRIG	Specify the trigger value of FIFO.	RW

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			TRIG	**Description**		
			00	Trigger Value is 4.		
			01	Trigger Value is 8.		
			10	Trigger Value is 16.		
			11	Trigger Value is 32.		
11:8	SRC_NUM	Source number. 0000:Unspecified; 0001~1111:1~15.				RW
7:4	CH1_NUM	Channel 1 number. 0000:Unspecified; 0001~1111:A~O.				RW
3:0	CH2_NUM	Channel 2 number. 0000:Unspecified; 0001~1111:A~O.				RW

27.2.17 SPDIF Configure 2 Register (SPCFG2)

The register SPCFG2 is used to configure SPDIF.

SPCFG2 **0x10020090**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				FS				ORG_FRQ				SAMPL_WL		MAX_WL	CLK_ACU					CAT_CODE						CH_MD		Reserved			PRE	COPY_N	AUDIO_N	CON_PRO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:26	FS	Sampling frequency. 0000:44.1kHz 0010:48kHz 0011:32kHz 1010:96kHz 1110:192kHz Others: Reference IEC60958-3	RW
25:22	ORG_FRQ	Original sampling frequency. 1111:44.1kHz 1101:48kHz 1100:32kHz 0101:96kHz 0001:192kHz Others: Reference IEC60958-3	RW
21:19	SAMPL_WL	Sample word length. When MAX_WL=1:	RW

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		001:20 bit 110:21 bit 010:22 bit 100:23 bit 101:24 bit Others: reserved When MAX_WL=0: 001:16 bit 110:17 bit 010:18 bit 100:19 bit 101:20 bit Others: reserved	
18	MAX_WL	Maximum audio sample word length. 0:20 bit 1:24 bit	RW
17:16	CLK_ACU	Clock Accuracy of transmitted clock. 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency	RW
15:8	CAT_CODE	Category code. Reference IEC60958-3 for full details. 00 indicates “general” mode.	RW
7:6	CH_MD	Channel mode choose bit. 00: Mode 0 01~11: Reserved	RW
5:4	Reserved	Writing has no effect, read as zero.	R
3	PRE	Pre-emphasis set bit. 0: None 1: 15us/15us	RW
2	COPY_N	Copyright set bit. 0: Copyright is asserted 1: Copyright is not asserted	RW
1	AUDIO_N	Linear PCM identification bit. 0: Audio sample word represents linear PCM samples 1: Audio sample word used for other purpose	RW
0	CON_PRO	Consumer mode and professional mode choose bit. 0: Consumer mode 1: Professional mode Professional is not supported in the chip.	RW

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27.2.18 SPDIF FIFO Register (SPFIFO)

The register SPCFG1 is used to configure SPDIF.

SPFIFO **0x10020094**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DATA																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	DATA	FIFO port. When write to it, data is push to the transmit FIFO. Read from it as 0.	W

27.3 Serial Interface Protocol

27.3.1 AC-link serial data format

Following figures are AC-link serial data format. Audio data is MSB adjusted, regardless of 8, 16, 18, 20, 24 bits sample size. When a 24-bits sample is transmitted, the LSB 4-bits are truncated. When try to record 24-bits sample, 4-bits of 0 are appended in LSB. Please reference to “AC ’97 Component Specification Revision 2.3, 2002”, provided by Intel Corporation, for details of AC ’97 architecture and AC-link specification.

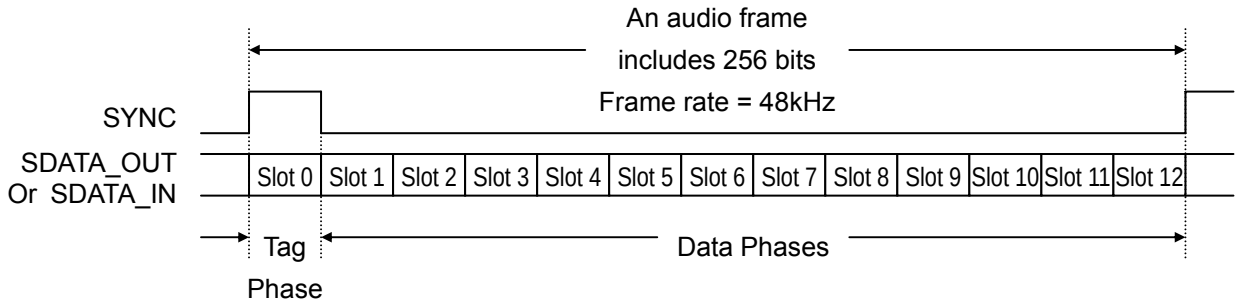


Figure 27-8 AC-link audio frame format

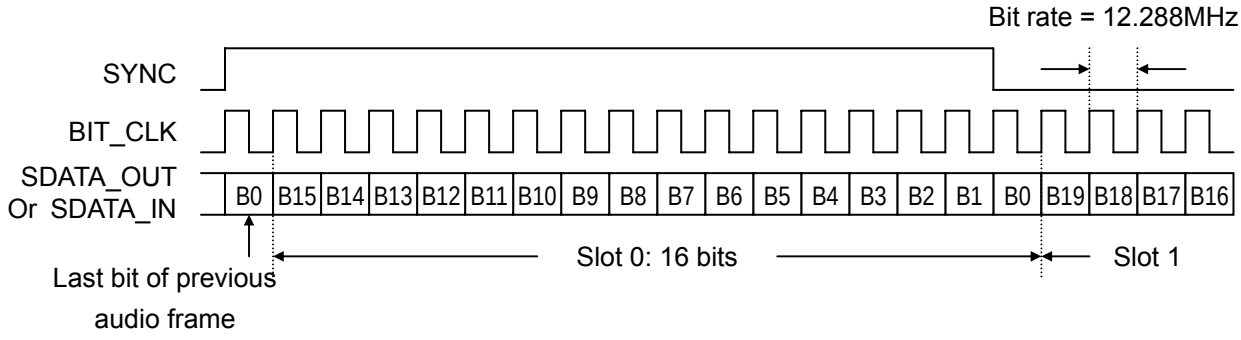


Figure 27-9 AC-link tag phase, slot 0 format

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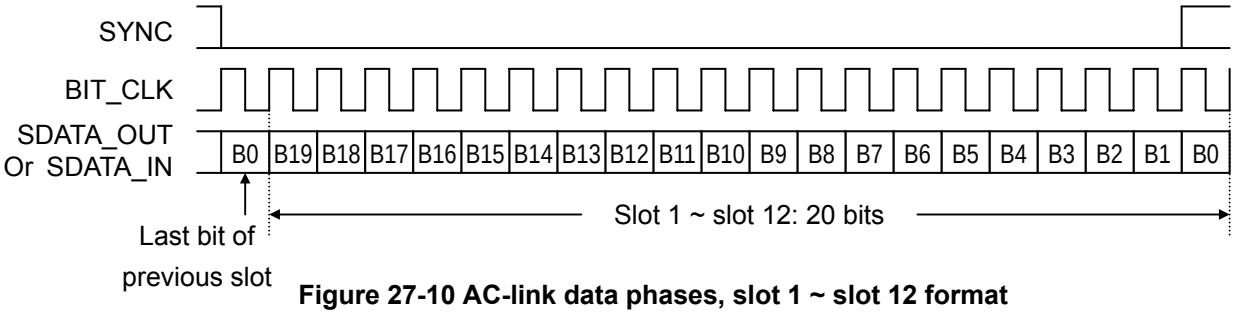


Figure 27-10 AC-link data phases, slot 1 ~ slot 12 format

27.3.2 I2S and MSB-justified serial audio format

Normal I2S and MSB-justified are similar protocols for digitized stereo audio transmitted over a serial path.

The BIT_CLK supplies the serial audio bit rate, the basis for the external CODEC bit-sampling logic. Its frequency is 64 times the audio sampling frequency. Divided by 64, the resulting 8 kHz to 48 kHz or even higher signal signifies timing for left and right serial data samples passing on the serial data paths. This left/right signal is sent to the CODEC on the SYNC pin. Each phase of the left/right signal is accompanied by one serial audio data sample on the data pins SDATA_IN and SDATA_OUT.

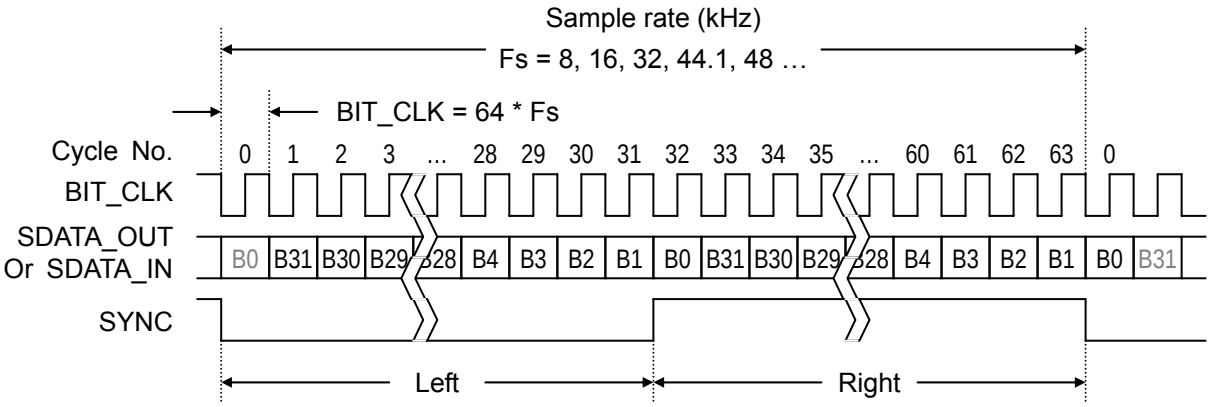


Figure 27-11 I2S data format (A: LR mode)

In the A: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode of I2S.

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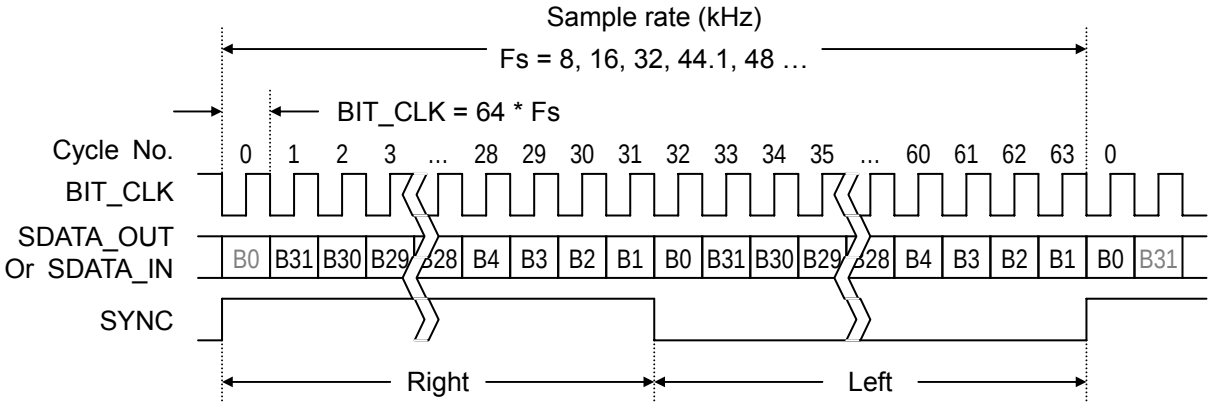


Figure 27-12 I2S data format (B: RL mode)

In the B: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame. It is used in same CODEC.

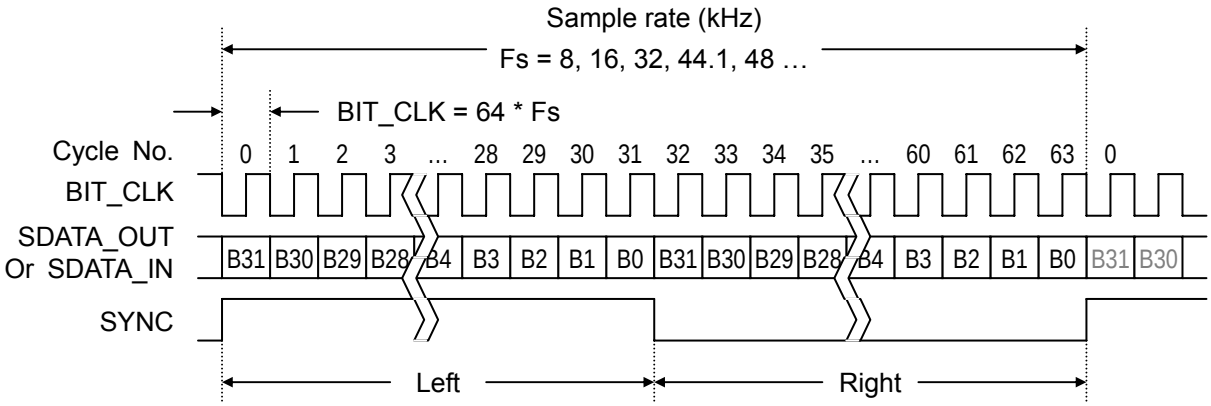


Figure 27-13 MSB-justified data format (C: LR mode)

In the C: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode in MSB-justified.

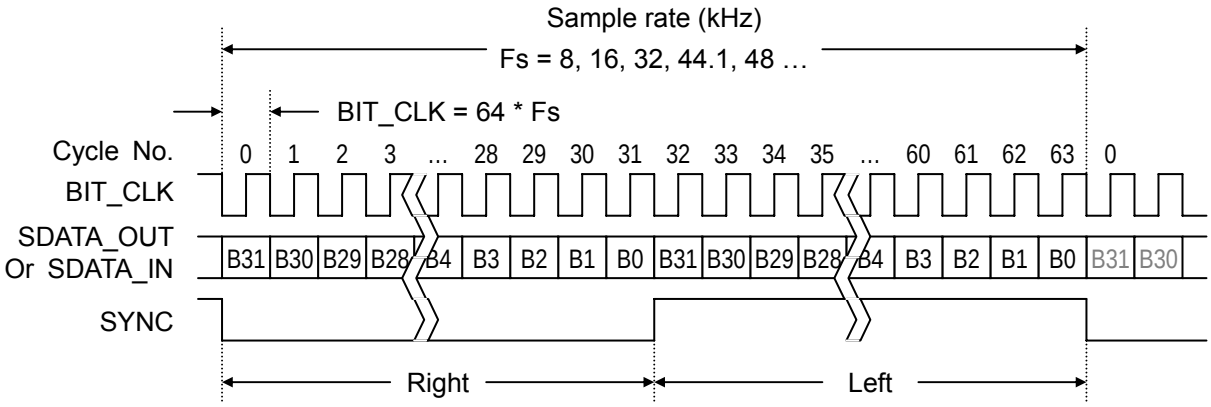


Figure 27-14 MSB-justified data format (D: RL mode)

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In the D: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame.

Figure 27-11 and Figure 27-13 provide timing diagrams that show formats for the normal I2S and MSB-justified modes of operations. Data is sampled on the rising edge of the BIT_CLK and data is sent out on the falling edge of the BIT_CLK.

Data is transmitted and received in frames of 64 BIT_CLK cycles(If BIT_CLK is generated internally). Each frame consists of a left sample and a right sample. Each sample holds 8, 16, 18, 20 or 24 bits of valid data. The LSB other bits of each sample is padded with zeroes.

In the normal I2S mode, the SYNC is low for the left sample and high for the right sample. Also, the MSB of each data sample lags behind the SYNC edges by one BIT_CLK cycle.
In the MSB-justified mode, the SYNC is high for the left sample and low for the right sample. Also, the MSB of each data sample is aligned with the SYNC edges.

When use with the internal CODEC, the BIT_CLK and SYNC signals also with O_BIT_CLK and O_SYNC signals are provided by the internal CODEC from the SYSCLK, which is enabled by I2SCR.ESCLK and configured to 12MHz clock using CPM.

27.3.3 Audio sample data placement in SDATA_IN/SDATA_OUT

The placement of audio sample in incoming/outgoing serial data stream for all formats support in AIC is MSB (Most Significant Bit) justified. Suppose n bit sample composed by

S_{n-1}	S_{n-2}	…	S_2	S_1	S_0

Table 27-3 described the how sample data bits are transferred.

Table 27-3 Sample data bit relate to SDATA_IN/SDATA_OUT bit

AC-link Format						I2S/MSB-Justified Format					
SDATA IN/OUT	Audio Sample Size (bit)					SDATA IN/OUT					
	8	16	18	20	24		8	16	18	20	24
B19	S7	S15	S17	S19	S23	B31	S7	S15	S17	S19	S23
B18	S6	S14	S16	S18	S22	B30	S6	S14	S16	S18	S22
B17	S5	S13	S15	S17	S21	B29	S5	S13	S15	S17	S21
B16	S4	S12	S14	S16	S20	B28	S4	S12	S14	S16	S20
B15	S3	S11	S13	S15	S19	B27	S3	S11	S13	S15	S19
B14	S2	S10	S12	S14	S18	B26	S2	S10	S12	S14	S18
B13	S1	S9	S11	S13	S17	B25	S1	S9	S11	S13	S17
B12	S0	S8	S10	S12	S16	B24	S0	S8	S10	S12	S16
B11	0	S7	S9	S11	S15	B23	0	S7	S9	S11	S15
B10	0	S6	S8	S10	S14	B22	0	S6	S8	S10	S14

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B9	0	S5	S7	S9	S13	B21	0	S5	S7	S9	S13
B8	0	S4	S6	S8	S12	B20	0	S4	S6	S8	S12
B7	0	S3	S5	S7	S11	B19	0	S3	S5	S7	S11
B6	0	S2	S4	S6	S10	B18	0	S2	S4	S6	S10
B5	0	S1	S3	S5	S9	B17	0	S1	S3	S5	S9
B4	0	S0	S2	S4	S8	B16	0	S0	S2	S4	S8
B3	0	0	S1	S3	S7	B15	0	0	S1	S3	S7
B2	0	0	S0	S2	S6	B14	0	0	S0	S2	S6
B1	0	0	0	S1	S5	B13	0	0	0	S1	S5
B0	0	0	0	S0	S4	B12	0	0	0	S0	S4
						B11	0	0	0	0	S3
						B10	0	0	0	0	S2
						B9	0	0	0	0	S1
						B8	0	0	0	0	S0
						B7~ B0	0	0	0	0	0

If in 16 bits packed mode, the data transferred is the same as the 16 bits normal mode as shown above. But there are two samples in one word.

27.3.4 SPDIF Protocol

SPDIF block format is shown below:

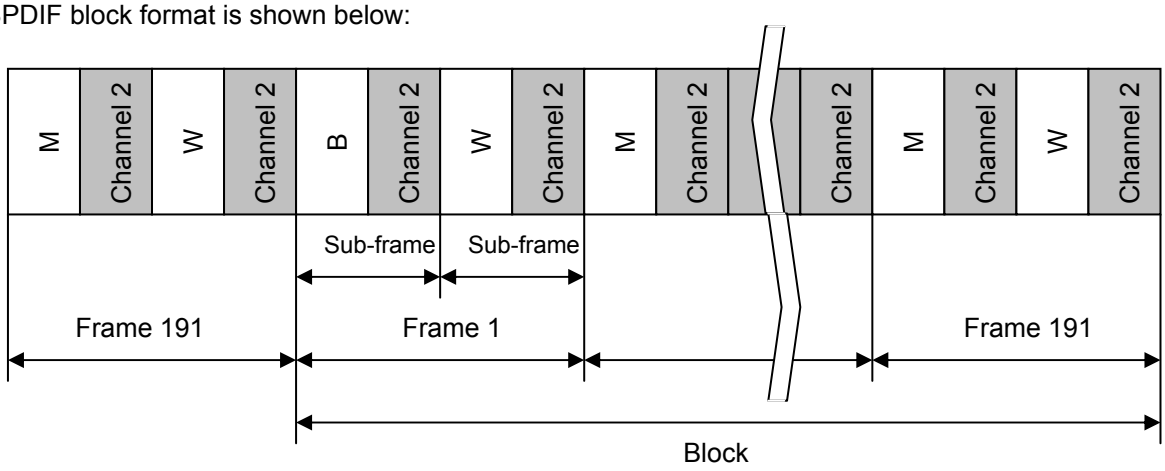


Figure 27-15 Block format

Sub-frame format in PCM mode is shown below:

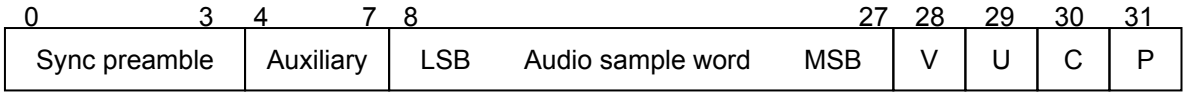


Figure 27-16 Sub-frame format in PCM mode

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Sub-frame format in non-PCM mode is shown below:

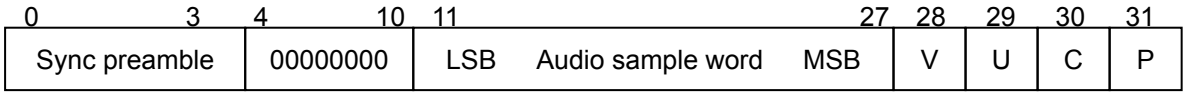


Figure 27-17 Sub-frame format in non-PCM mode

27.4 AC97/I2S Operation

The AIC can be accessed either by the processor using programmed I/O instructions or by the DMA controller. The processor uses programmed I/O instructions to access the AIC and can access the following types of data.

- **The AIC memory mapped registers data**—All registers are 32 bits wide and are aligned to word boundaries.
- **AIC controller FIFO data—**An entry is placed into the transmit FIFO by writing to the I2S controller's Serial Audio Data register (AICDR). Writing to AICDR updates a transmit FIFO entry. Reading AICDR flushes out a receive FIFO entry.
- **The external CODEC registers for I2S CODEC—**CODEC registers can be accessed through the L3 bus. The L3 bus operation is emulated by software controlling three GPIO pins.
- **The external CODEC registers for AC97 CODEC**—An AC97 audio CODEC can contain up to sixty-four 16-bit registers. A CODEC uses a 16-bit address boundary for registers. The AIC supplies access to the CODEC registers through several registers.
- **The internal CODEC registers** can be accessed via memory-mapped registers in the CODEC.

The DMA controller can only access the FIFOs. Accesses are made through the data registers, as explained in the previous paragraph. The DMA controller responds to the following DMA requests made by the I2S controller:

- The transmit FIFO request is based on the transmit trigger-threshold (AICFR.TFTH) setting. See 0 for further details regarding AICFR.TFTH.
- The receive FIFO request is based on the receive trigger-threshold (AICFR.RFTH) setting. See 0 for further details regarding AICFR.RFTH.

Before operation to AIC, you may need to set proper PIN function selection from GPIO using if the pin is shared with GPIO.

Please also reference to "AC '97 Component Specification Revision 2.3, 2002" when deal with AIC AC-link operations.

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27.4.1 Initialization

At power-on or other hardware reset (WDT and etc), AIC is disabled. Software must initiate AIC and the internal or external CODEC after power-on or reset. If errors found in data transferring, or in other places, software must initial AIC and optional, the internal or external CODEC. Here is the initial flow.

1 Select internal or external CODEC (AICFR.ICDC).
2 If external CODEC is selected, select AC-link or I2S/MSB-Justified (AICFR.AUSEL). If internal CODEC is used, select I2S/MSB-Justified format (AICFR.AUSEL=1). If the resettlement without involving link format and architecture changing, this step can be skip.
3 If I2S/MSB-Justified is selected, select between I2S and MSB-Justified (I2SCR.AMSL).
4 Decide BIT_CLK direction (AICFR.BCKD) and SYNC direction (AICFR.SYNCD).
5 If BIT_CLK is configured as output, BIT_CLK divider I2SDIV.DV must be set to what correspond with the values as shown in Table 27-7. And the clock selection and the divider between PLL clock out and AIC also must be set (CFCR.I2S and I2SCDR in CPM). If internal CODEC is used, select 12MHz clock input (via set proper value in CFCR.I2S and I2SCDR), I2S format (I2SCR.AMSL=0), input BIT_CLK (AICFR.BCKD=0), input SYNC (AICFR.SYNCD=0).
6 Enable AIC by write 1 to AICFR.ENB.
7 If it needs to reset AIC registers and flush FIFOs, write 1 to AICFR.RST. If it need only flush FIFOs, write 1 to AICCR.FLUSH. BIT_CLK must exist here and after.
8 In AC-link format, issue a warm or cold CODEC reset.
9 In AC-link format, configure AC ’97 CODEC via ACCAR and ACCDR registers. If the resettlement doesn’t involving AC’97 CODEC registers changing, this step can be skipped.
10 In case of external CODEC with I2S/MSB-Justified format, configure I2S/MSB-justified CODEC via the control bus connected to the CODEC, for instance I2C or L3, depends on CODEC. In case of internal CODEC, configure CODEC via CODEC’s memory mapped registers. If the resettlement without involving I2S/MSB-justified CODEC or ADC/DAC function changing, this step can be skip.

27.4.2 AC ’97 CODEC Power Down

AC ‘97 CODEC can be placed in a low power mode. When the CODEC’s power-down register (26h), is programmed to the appropriate value, the CODEC will be put in a low power mode and both BIT_CLK and SDATA_IN will be brought to and held at a logic low voltage level.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the CODEC Ready bit (input slot 0, bit 15).

27.4.3 Cold and Warm AC ’97 CODEC Reset

AC-link reset operations occur when the system is initially powered up, when resuming from a lower powered sleep state, and in response to critical subsystem failures that can only be recovered from

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with a reset.

27.4.3.1 Cold AC '97 CODEC Reset

A cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_IN will be activated, or re-activated as the case may be, and all AC '97 CODEC registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC '97 CODEC input.

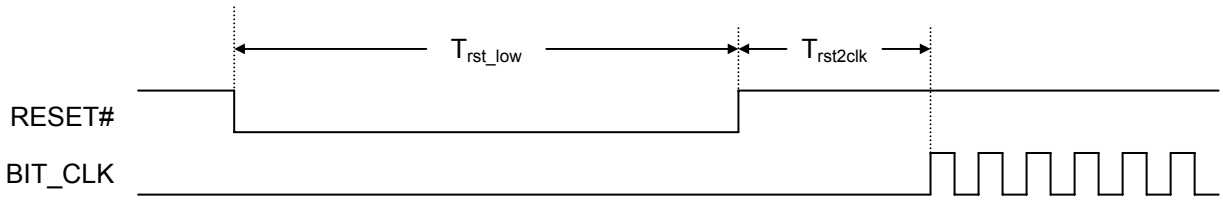


Figure 27-18 Cold AC '97 CODEC Reset Timing

Table 27-4 Cold AC '97 CODEC Reset Timing parameters

Parameter	Symbol	Min	Type	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	μs
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

27.4.3.2 Warm AC '97 CODEC Reset

A warm AC'97 reset will re-activate the AC-link without altering the current AC'97 register values. Driving SYNC high for a minimum of 1 μs in the absence of BIT_CLK signals a warm reset.

Within normal audio frames SYNC is a synchronous AC '97 CODEC input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC '97 CODEC.

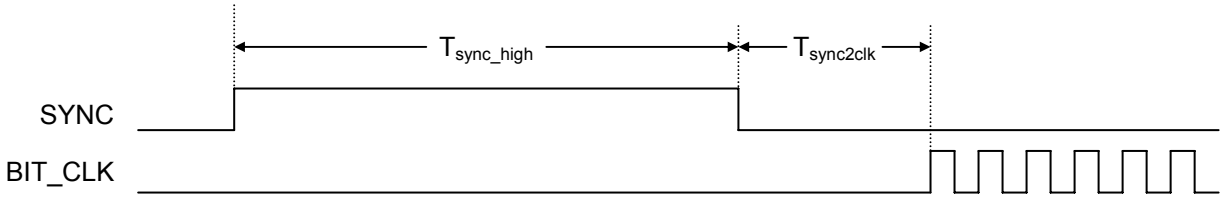


Figure 27-19 Warm AC '97 CODEC Reset Timing

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Table 27-5 Warm AC '97 CODEC Reset Timing Parameters

Parameter	Symbol	Min	Type	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	Ms
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	Ns

27.4.4 External CODEC Registers Access Operation

The external audio CODEC can be configured/controlled by its internal registers. To access these registers, an I2S/MSB-justified CODEC usually employs L3 bus, SPI bus, I2C bus or other control bus. The L3 bus operation can be emulated by software by using 3 GPIO pins of the chip. For AC '97, "AC '97 Component Specification" defines the CODEC register access protocol. Several registers are provided in AIC to accomplish this task.

The ACCAR and ACCDR are used to send a register accessing request command to external AC'97 CODEC. The ACSAR and ACSDR are used to receive a register's content from external AC'97 CODEC. The register accessing request and the register's content returning is asynchronous.

The AC'97 CODEC register accessing request flow:

1 If ACSR.CADT is 0, wait for 25.4μs. If no previous accessing request, this step can be skip.
2 Clear ACSR.CADT.
3 If read access, write read-command and register address to ACCAR, if write access, write write-command and register address to ACCAR and write data to ACCDR. Any order of write ACCAR and ACCDR is OK.
4 Polling for ACSR.CADT changing to 1, which means the request has been send to CODEC via AC-link.

The AC'97 CODEC register content receiving flow by polling:

1 Polling for ACSR.SADR changing to 1.
2 Read the CODEC register's address from ACSAR and content from ACSDR.
3 Clear ACSR.SADR.

The AC'97 CODEC register content receiving flow by interrupt:

1 Before accessing request, clear ACSR.SADR and set ACCR2.ESADR.
2 Waiting for the interrupt. When the interrupt is found, check if ACSR.SADR is 1, if not, repeat this step again.
3 Read the CODEC register's address from ACSAR and content from ACSDR.
4 Clear ACSR.SADR.

27.4.5 Audio Replay

Outgoing audio sample data (from AIC to CODEC) is written to AIC transmit FIFO from processor via store instruction or from memory via DMA. AIC then takes the data from the FIFO, serializes it, and

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sends it over the serial wire SDATA_OUT to an external CODEC or over an internal wire to an internal CODEC.

The audio transmission is enabled automatically when the AIC is enabled by set AICFR.ENB. But all replay data is zero at this time except both of the following conditions are true:

1 AICCR.ERPL must be 1. If AICCR.ERPL is 0, value of zero is send to CODEC even if there are samples in transmit FIFO.
2 At least one audio sample data in the transmit FIFO. If the transmit FIFO is empty, value of zero or last sample depends on AICFR.LSMP, is send to CODEC even if AICCR.ERPL is 1.

Here is the audio replay flow:

1 Configure the CODEC as needed.
2 Configure sample size by AICCR.OSS.
3 Configure sample channels (AICCR.CHANNEL).
4 If sample size is configured 16 bit, select packed or unpacked mode (AICCR.PACK16).
5 If two channels is configured, select the right-channel-first sample data or not (I2SCR.RFIRST).
6 If two channels is configured, select the sample data switched or not (I2SCR.SWLH).
7 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for AC-link or BIT_CLK provided by external CODEC) or by accessing CODEC internal registers (for internal CODEC).
8 For AC-link, configure replay channels by ACCR1.XS.
9 Some other configurations: mono to stereo, endian switch, signed/unsigned data transfer, transmit FIFO configuration, play ZERO or last sample when TX FIFO under-run, and etc.
10 Write 1 to AICCR.ERPL.
It is suggested that at least a frame of PCM data is pre-filled in the transmit FIFO to prevent FIFO under-run flag (AICSR.TUR).
But when using internal CODEC, write first frame of PCM data to transmit FIFO till TX FIFO under-run (AICSR.TUR is set to 1), otherwise left/right channel may be switched.
11 Fill sample data to the transmit FIFO. Repeat this till finish all sample data. In this procedure, please control the FIFO to make sure no FIFO under-run and other errors happen. When the transmit FIFO under-run, noise or pause may be heard in the audio replay, AICSR.TUR is 1, and if AICCR.ETUR is 1, AIC issues an interrupt. Please reference to 27.4.7 for detail description on FIFO.
12 Waiting for AICSR.TFL change to 0. So that all samples in the transmit FIFO has been replayed, then we can have a clean start up next time.
13 Write 0 to AICCR.ERPL.

NOTE: Before replaying Open ADC BITCLK and close it to generating Record internal circuit reset when using internal CODEC.

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27.4.6 Audio Record

Incoming audio sample data (from CODEC to AIC) is received from SDATA_IN (for an external CODEC) or an internal wire (for an internal CODEC) serially and converted to parallel word and stored in AIC receive FIFO. Then the data can be taken from the FIFO to processor via load instruction or to memory via DMA.

The audio recording is enabled automatically when the AIC is enabled by set AICFR.ENB. But all received data is discarded at this time except both of the following conditions are true:

1 AICCR.EREC must be 1. If AICCR.EREC is 0, the received data is discarded even if there are rooms in the receive FIFO.
2 At least one room left in the receive FIFO. If the receive FIFO is full, the received data is discarded even if AICCR.EREC is 1.

Here is the audio record flow:

1 Configure the CODEC as needed.
2 Configure sample size by AICCR.ISS.
3 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for AC-link or BIT_CLK provided by external CODEC) or by CODEC memory mapped registers (for internal CODEC).
4 Some other configurations: signed/unsigned data transfer, receive FIFO configuration, and etc.
5 Write 1 to AICCR.EREC. Make sure there are rooms available in the receive FIFO before set AICCR.EREC. Usually, it should empty the receive FIFO by fetch data from it before set AICCR.EREC.
6 Take sample data form the receive FIFO. Repeat this till the audio finished. In this procedure, please control the FIFO to make sure no FIFO over-run and other errors happen. When the receive FIFO over-run, same recorded audio samples will be lost, AICSR.ROR is 1, and if AICCR.EROR is 1, AIC issues an interrupt. Please reference to 27.4.7 for detail description on FIFO. For AC-link, ACCR1.RS tells which channels are recorded.
   When using internal CODEC, the first data should be ignored.
7 Write 0 to AICCR.EREC.
8 Take sample data from the receive FIFO until AICSR.RFL change to 0. So that all samples in the receive FIFO has been taken away, then we can have a clean start up next time. When the receive FIFO is empty, read from it returns zero.

27.4.7 FIFOs operation

AIC has two FIFOs, one for transmit audio sample and one for receive. All AIC played/recorded audio sample data is taken from/send to transmit/receive FIFOs. The RX FIFO is in 24 bits width and 32 entries depth, one entry for keeping one audio sample regardless of the sample size. The RX FIFO is in 32 bits width and 64 entries depth, one entry for keeping one audio sample regardless of the sample size, but in 16 bits packed mode, one entry for keeping two audio samples. AICDR.DATA provides the access point for processor/DMA to write to transmit FIFO and read from receive FIFO. One time

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access to AICDR.DATA process one sample. The sample data should be put in LSB (Least Significant Bit) in memory or processor registers. For transmitting, bits exceed sample are discarded. For receiving, these bits are set to 0. Figure 27-20 illustrates the FIFOs access.

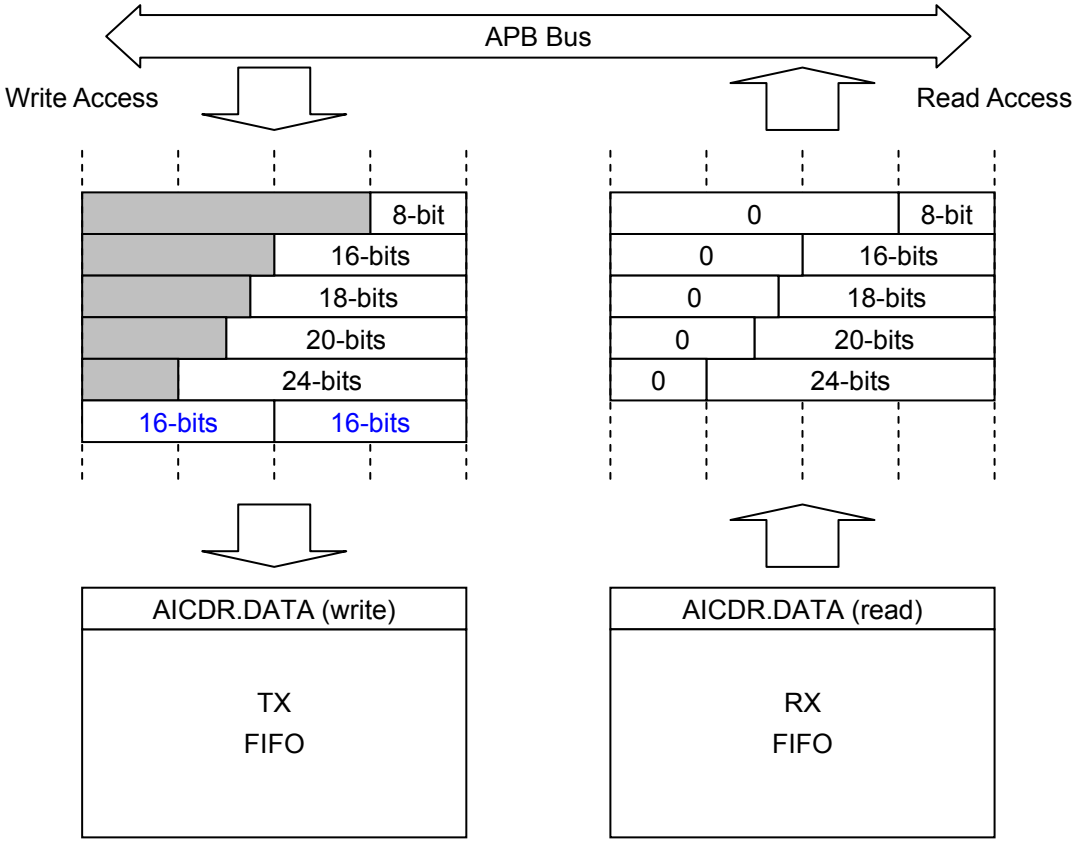


Figure 27-20 Transmitting/Receiving FIFO access via APB Bus

The software and bus initiator must guarantee the right sample placement at the bus.

In case of DMA bus initiator, one 24, 20, 18 bits audio sample must occupies one 32-bits word in memory, so 32-bits width DMA must be used. One 16 bits sample occupies one 16-bits half word in memory, so 16-bits width DMA must be used. One 8-bits sample occupies one byte in memory, and use 8-bits width DMA except 16bits packed mode. If in 16 bits packed mode, Two 16 bits sample occupies one 32-bits word in memory, so 32-bits width DMA must be used.

In case of processor bus initiator, any type of the audio sample must occupy one CPU general-purpose register at LSB, and read/write from/to AICDR.DATA with 32-bits load/store instruction. When process small sample size, 16-bits or 8-bits, software may need to do the data pack/unpack except 16 bits packed mode. In the 16bits packed mode, the sample data is packed, and two 16 bits audio samples occupy one CPU general-purpose register.

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The AICFR.TFTH and AICFR.RFTH are used to set the FIFO level thresholds, which are the trig levels of DMA request and/or FIFO service interrupt. The AICFR.TFTH and AICFR.RFTH should be set to proper value; too small or too big are not good. When AICFR.RFTH is too small, or AICFR.TFTH is too big, the DMA burst length or the number of sample can be processed by processor is too small, which harms the bus or processor efficiency. When AICFR.RFTH is too big or AICFR.TFTH is too small, the bus or the interrupt latency left for under-run/over-run is too small, which may causes replay/record errors.

AICSR.TUR is set to 1 during transmit under-run conditions. If AICCR.ETUR is 1, this can trigger an interrupt. During transmit under-run conditions, zero or last sample is continuously sent out across the serial link. Transmit under-run can occur under the following conditions:

1 Valid transmit data is still available in memory, but the DMA controller/processor starves the transmit FIFO, as it is busy servicing other higher-priority tasks.
2 The DMA controller/processor has transferred all valid data from memory to the transmit FIFO.

AICSR.ROR is set to 1 during receive over-run conditions. If AICCR.EROR is 1, this can trigger an interrupt. During receive over-run conditions, data sent by the CODEC is lost and is not recorded.

When replay/record two channels data, the left channel is default the first data in FIFOs and in the serial link. If multiple channels in AC-link are used, the channel sample order is follows the slot order. In 16bits packed mode, could configure that the left channel is the first data or the right channel. By default, the 16 bits LSB is left channel, 16 bits MSB is the right channel. But it also could be switched the Left or the Right channel (I2SCR.SWLH).

27.4.8 Data Flow Control

There are three approaches provided to control/synchronize the audio incoming/outgoing data flow.

27.4.8.1 Polling and Processor Access

AICSR.RFL and AICSR.TFL reflect how many samples exist in receiving and transmitting FIFOs. Through read these register fields, processor can detect when there are samples in receiving FIFO in audio record and then load them from the RX-FIFO, and when there are rooms in transmitting FIFO in audio replay and then store samples to the TX-FIFO.

Polling approach is in very low efficiency and is not recommended.

27.4.8.2 Interrupt and Processor Access

Set proper values to AICFR.TFTH and AICFR.RFTH, the FIFO interrupts trig thresholds. Set AICCR.ETFS and/or AICCR.ERFS to 1 to enable transmitting and/or receiving FIFO level trigger interrupts. When the interrupt found, it means there are rooms or samples in the TX or RX FIFO, and processor can store or load samples to or from the FIFO.

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Interrupt approach is more efficient than polling approach.

27.4.8.3 DMA Access

Audio data is real time stream, though it is in low data bandwidth, usually less than 1.2Mbps. DMA approach is the most efficient and is the recommended approach.

To enable DMA operation, set AICCR.TDMS and AICCR.RDMS to 1 for transmit and receive respectively. It also needs to allocate two channels in DMA controller for data transmitting and receiving respectively. Please reference to the processor's DMA controller spec for the details.

The AICFR.TFTH and AICFR.RFTH are used to set the transmitting and receiving FIFO level thresholds, which determine the issuing of DMA request to DMA controller. To respond the request, DMAC initiator and controls the data movement between memory and TX/RX FIFO.

27.4.9 Audio Samples format

27.4.9.1 16 bits packed mode

One channel (mono) mode and two channels (stereo) mode:

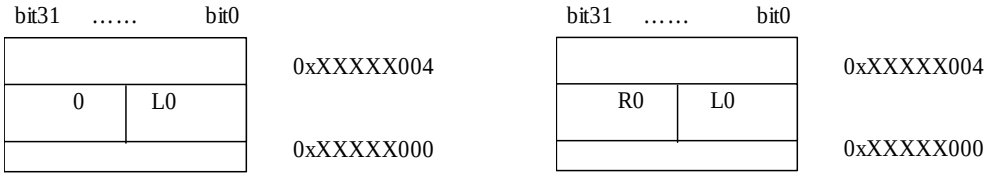


Figure 27-21 One channel (Left) and Two channels (right) mode (16 bits packed mode)

Four channels mode and six channels mode:

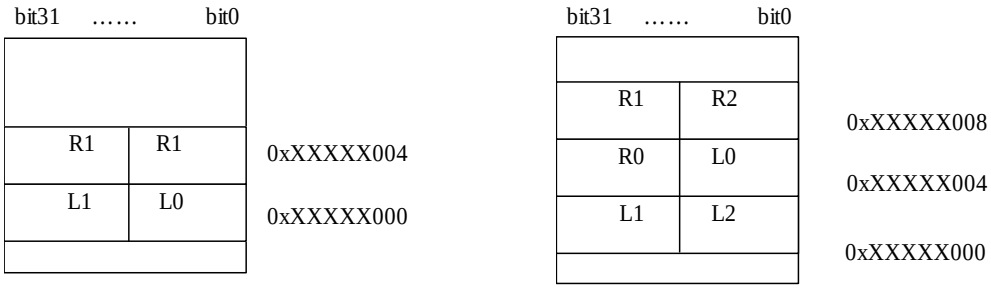


Figure 27-22 Four channels (Left) and Six channels (right) mode (16 bits packed mode)

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Eight channels mode:

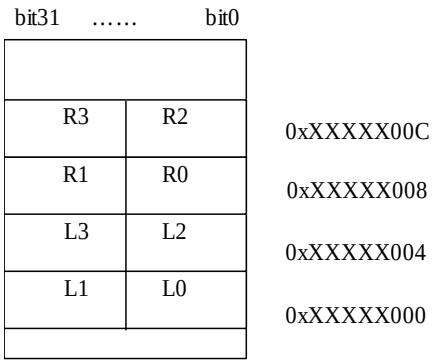


Figure 27-23 Eight channels mode (16 bits packed mode)

27.4.9.2 Normal mode.

One channel (Mono) and two channels (stereo) mode:

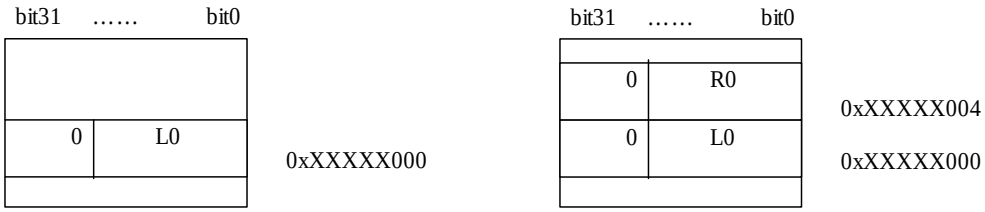


Figure 27-24 One channel (Left) and Two channels (right) mode

Four channels mode and six channels mode:

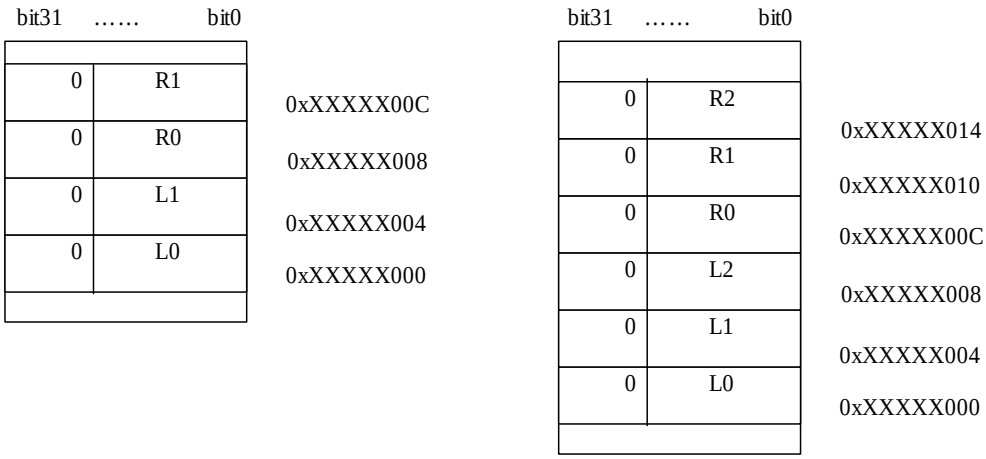


Figure 27-25 Four channels (Left) and Six channels (right) mode

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Eight channel mode:

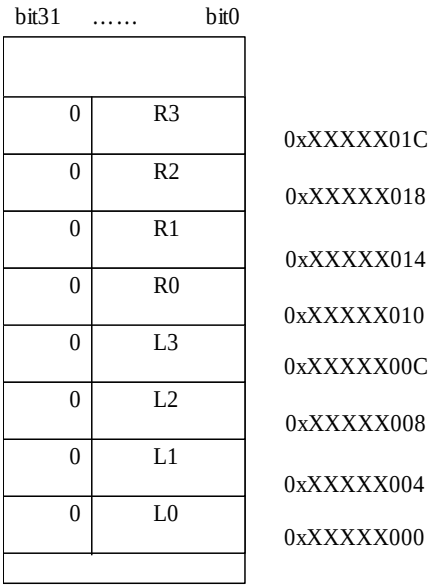


Figure 27-26 Eight channels mode

27.4.10 Serial Audio Clocks and Sampling Frequencies

For internal CODEC, CODEC module containing the audio CODEC circuit/logic and corresponding controlling registers. CODEC needs a 12MHz clock from CPM called SYS_CLK and provides I_BITCLK, O_BITCLK and I_SYNC, O_SYNC (left-right clock which is the sample rate as ADC or DAC) to AIC for outgoing and incoming audio respectively. These clocks change when change the sample rate in CODEC controlling registers. When using internal CODEC, must configure SYNC and BIT_CLK as input, more details refers to CODEC Spec.

For AC-link, the bit clock is input from chip external and is fixed to 12.288MHz. The sample frequency of 48kHz is supported in nature. Variable Sample Rate feature is supported in this AIC. If the CODEC supports this feature, sample rate other than 48kHz audio data can be replay directly. Otherwise, software has to do the rate transfer to replay other sample rate audio data. Double rate, 96kHz or even 88.2kHz audio is also supported with proper CODEC.

Following are for BIT_CLK/SYS_CLK configuration in I2S/MSB-Justified format with external CODEC.

The BIT_CLK is the rate at which audio data bits enter or leave the AIC. BIT_CLK can be supplied either by the CODEC or an internally PLL. If it is supplied internally, BIT_CLK is configured as output pins, and is supplied out to the CODEC. If BIT_CLK is supplied by the CODEC, then it is configured as an input pin. Register bit AICFR.BCKD is used to select BIT_CLK direction.

The audio sampling frequency is the frequency of the SYNC signal, which must be 1/64 of BIT_CLK, $f_{BIT\_CLK} = 64\ f_{S.}$ But SYNC signal frequency is not fixed when using internal CODEC.

SYS_CLK is only for CODEC. It usually takes one of the two roles, as CODEC master clock input or as CODEC over-sampling clock input. If SYS_CLK roles as CODEC master clock input, it usually should

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be set to a fixed frequency according to CODEC requirement but independent to audio sample rate. In this case, usually there is a PLL in the CODEC and CODEC roles master mode. See Figure 27-3 for the interface diagram. This is the recommended AIC CODEC system configuration.

If SYS_CLK roles as CODEC over-sampling clock, its frequency is usually 4, 6, 8 or 12 times of BIT_CLK frequency, which are 256, 384, 512 and 768 times of audio sample rates. Table 27-6 lists the relation between sample rate, BIT_CLK and SYS_CLK frequencies.

Table 27-6 Audio Sampling rate, BIT_CLK and SYS_CLK frequencies

Sample Rate f_S (kHz)	BIT_CLK (MHz) $f_{BIT\_CLK} = 64\ f_S$	SYS_CLK (MHz)			
		256 f_S	384 f_S	512 f_S	768 f_S
48	3.072	12.288	18.432	24.576	36.864
44.1	2.8224	11.2896	16.9344	22.5792	33.8688
32	2.048	8.192	12.288	16.384	24.576
24	1.536	6.144	9.216	12.288	18.432
22.05	1.4112	5.6448	8.4672	11.2896	16.9344
16	1.024	4.096	6.144	8.192	12.288
11.025	0.7056	2.8224	4.2336	5.6448	8.4672
8	0.512	2.048	3.072	4.096	6.144

In this processor, SYS_CLK can be selected from EXCLK or generated by dividing the PLL output clock in a CPM divider controlled by I2SCDR. If BIT_CLK is chosen as an output, another divider in AIC is used to divide SYS_CLK for it.

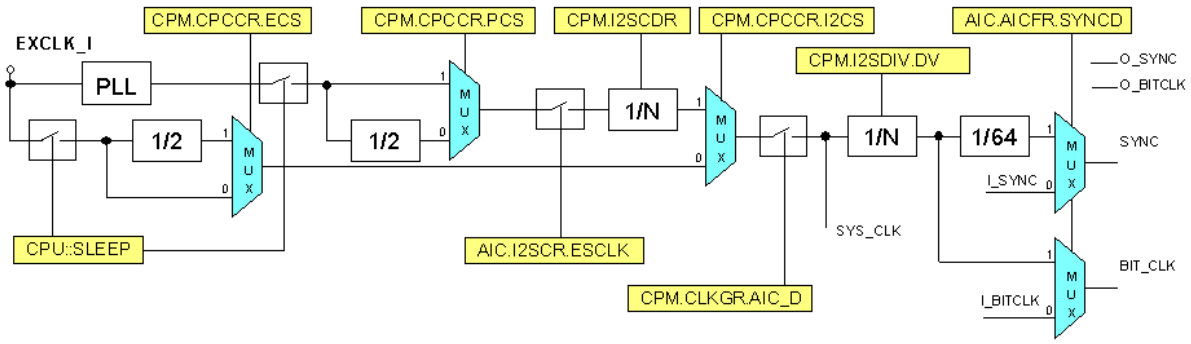


Figure 27-27 SYS_CLK, BIT_CLK and SYNC generation scheme

The setting of I2SDIV.DV is shown in Table 27-7.

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Table 27-7 BIT_CLK divider setting

I2SDIV.DV	f_{SYS_CLK}	f_{BIT_CLK}	f_{SYS_CLK} / f_{BIT_CLK}
0x1	128 f_S	64 f_S	2
0x2	196 f_S	64 f_S	3
0x3	256 f_S	64 f_S	4
0x5	384 f_S	64 f_S	6
0x7	512 f_S	64 f_S	8
0xB	768 f_S	64 f_S	12

As we observe in Table 27-6, if SYS_CLK is taken as over-sampling clock by CODEC, the common multiple of all SYS_CLK frequencies is much bigger than the PLL output clock frequency. To generate all different SYS_CLK frequencies, one approach is change PLL frequency according to sample rate. This is not realistic, since frequently change PLL frequency during normal operation is not recommended.

Another approach is to found some approximate common multiples of all SYS_CLK frequencies according to the fact that there tolerance in audio sample rate. Take f_{SYS_CLK} = 256 f_S, Table 27-8 list most frequencies, which are less than 400MHz, with relatively small sample rate errors. It is suggested to set PLL frequency as close to the frequencies listed as possible, then use clock dividers to generate different SYS_CLK/BIT_CLK for different sample rate.

Table 27-8 Approximate common multiple of SYS_CLK for all sample rates

Approximate Common Frequency (MHz)	Max Error Caused in Audio Sample Rate (%)
123.53	0.53
147.11	0.24
170.68	0.79
235.5	0.87
247.06	0.53
270.64	0.11
280.56	0.73
294.22	0.24
305.14	0.67
317.79	0.53
329.57	0.66
341.35	0.79
347	0.85
353.13	0.90
358.79	0.69
370.59	0.53

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382.96	0.54
394.17	0.24

Take PLL = 270.64 MHz as an example, Table 27-9 lists the divider settings for various sample rates.

Table 27-9 CPM/AIC clock divider setting for various sampling rate if PLL = 270.64MHz

Sample Rate (kHz)	I2SCDR	I2SDIV.DV	Sample Rate Error (%)
48	1	11	0.11
44.1	1	12	-0.11
32	0	33	0.11
24	1	22	0.11
22.05	1	24	-0.11
16	1	33	0.11
12	1	44	0.11
11.025	1	48	-0.11
8	1	66	0.11

For an EXCLK clock frequency, try to generate PLL frequencies as close to the frequencies listed in Table 27-8 as possible. Table 27-10 lists the PLL parameters and audio sample errors at different PLL frequencies for EXCLK at 12MHz.

Table 27-10 PLL parameters and audio sample errors for EXCLK=12MHz

PLL			Max Sample Rate Error
M	N	Freq (MHz)	
103	10	123.6	0.59%
49	4	147	0.31%
128	9	170.67	0.79%
157	8	235.5	0.87%
103	5	247.2	0.59%
65	3	260	0.82%
45	2	270	0.35%
203	9	270.67	0.12%
113	5	271.2	0.32%
187	8	280.5	0.75%
237	10	284.4	0.81%
49	2	294	0.31%
178	7	305.14	0.67%
53	2	318	0.60%
302	11	329.45	0.70%
256	9	341.33	0.79%

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318	11	346.91	0.88%
206	7	353.14	0.90%
299	10	358.8	0.69%
247	8	370.5	0.55%
351	11	382.91	0.55%
230	7	394.29	0.27%

The BIT_CLK should be stopped temporary when change the divider settings, or when change BIT_CLK source (from internal or external), to prevent clock glitch. Register I2SCR.STPBK is provided to assist the task. When I2SCR.STPBK = 1, BIT_CLK is disabled no matter whether it is generated internally or inputted from the external source. The operation flow is described in following.

1 Stop all replay/record by clear AICCR.ERPL and AICCR.EREC.
2 Polling I2SSR.BSY till it is 0.
3 Stop the BIT_CLK by write 1 to I2SCR.STPBK.
4 Operations concerning BIT_CLK.
5 Resume the BIT_CLK by write 0 to I2SCR.STPBK.

27.4.11 Interrupts

The following status bits, if enabled, interrupt the processor:

- Receive FIFO Service (AICSR.RFS). It's also DMA Request.
- Transmit FIFO Service (AICSR.TFS). It's also DMA Request.
- Transmit Under-Run (AICSR.TUR).
- Receive Over-Run (AICSR.ROR).
- Command Address and Data Transmitted, AC-link only (ACSR.CADT).
- External CODEC Registers Status Address and Data Received, AC-link only (ACSR.SADR).
- External CODEC Registers Read Status Time Out, AC-link only (ACSR.RSTO).

For further details, see the corresponding register description sections.

27.5 SPDIF Guide

27.5.1 Set SPDIF clock frequency

Set SPDIF clock frequency is as same as i2s clock.

27.5.2 PCM audio mode operation (Reference IEC60958)

1 Set SPCFG1 and SPCFG2 to configure SPDIF transmitter.
  a Set SPCFG2.CON_PRO to 0 to choose consumer mode.
  b Set SPCFG2. AUDIO_N to 0 to choose linear PCM audio data mode.
  c Set SPCFG1.XXX to configure SPDIF.
  d Set SPCFG2.XXX to configure SPDIF.

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2 Set SPCTRL.DMA_EN to choose DMA mode or CPU mode.
3 Set SPCTRL.SIGN_N to choose whether to transfer the most significant bit by toggle or not.
4 Set SPCTRL. SFT_RST to 1 reset FIFO.
5 Wait SPCTRL. SFT_RST set to be set 0 by hardware.
6 Set SPCTRL.M_TRIG and SPCTRL.M_FFUR to enable or disable the interrupt.
7 Set SPCTRL.INVALID 1 or 0 to set the V bit of sub-frame.
8 Set SPENA.SPEN to 1 to Enable SPDIF to transmitter.

27.5.3 Non-PCM mode operation (Reference IEC61937)

1 Set SPCFG1 and SPCFG2 to configure SPDIF transmitter.
   a Set SPCFG2.CON_PRO to 0 to choose consumer mode.
   b Set SPCFG2.AUDIO_N to 1 to choose non-PCM mode.
   c Set SPCFG1.SRC_NUM to 0.
   d Set SPCFG1.CH1_NUM to 0.
   e Set SPCFG1.CH2_NUM to 0.
   f Set SPCFG2.PRE to 0.
   g Set SPCFG2.CH_MD to 0.
   h Set SPCFG2.ORG_FRQ to 0.
   i Set SPCFG2.SAMPL_WL to 0.
   j Set SPCFG2.MAX_WL to 0.
   k Set SPCFG1.XXX to configure SPDIF.
   l Set SPCFG2.XXX to configure SPDIF.
2 Set SPCTRL.DMA_EN to choose DMA mode or CPU mode.
3 Set SPCTRL.SIGN_N to choose whether to transfer the most significant bit by toggle or not.
4 Set SPCTRL. SFT_RST to 1 reset FIFO.
5 Wait SPCTRL. SFT_RST to be set to 0 by hardware.
6 Set SPCTRL.M_TRIG and SPCTRL.M_FFUR to enable or disable the interrupt.
7 Set SPCTRL.INVALID 1 or 0 to set the V bit of sub-frame.
8 Set SPENA.SPEN to 1 to Enable SPDIF to transmitter.

27.5.4 Disable operation

1 Set SPENA.SPEN to 0 to disable SPDIF to transmitter.
2 Wait SPSTATE.BUSY to be set to 0 by hardware.
3 You can do other operation.

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28 PCM Interface

28.1 Overview

The PCM has the following features:

- Data starts with the frame PCMSYN or one PCMCLK later
- Support three modes of operation for PCM
  - Short frame sync mode
  - Long frame sync mode
  - Multi-slot mode
- Data is transferred and received with the MSB first
- Support master mode and slave mode
- The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
- The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
- 8/16 bit sample data sizes supported
- DMA transfer mode supported
- Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- Two independent PCM interface. As PCM0,PCM1

28.2 Pin Description

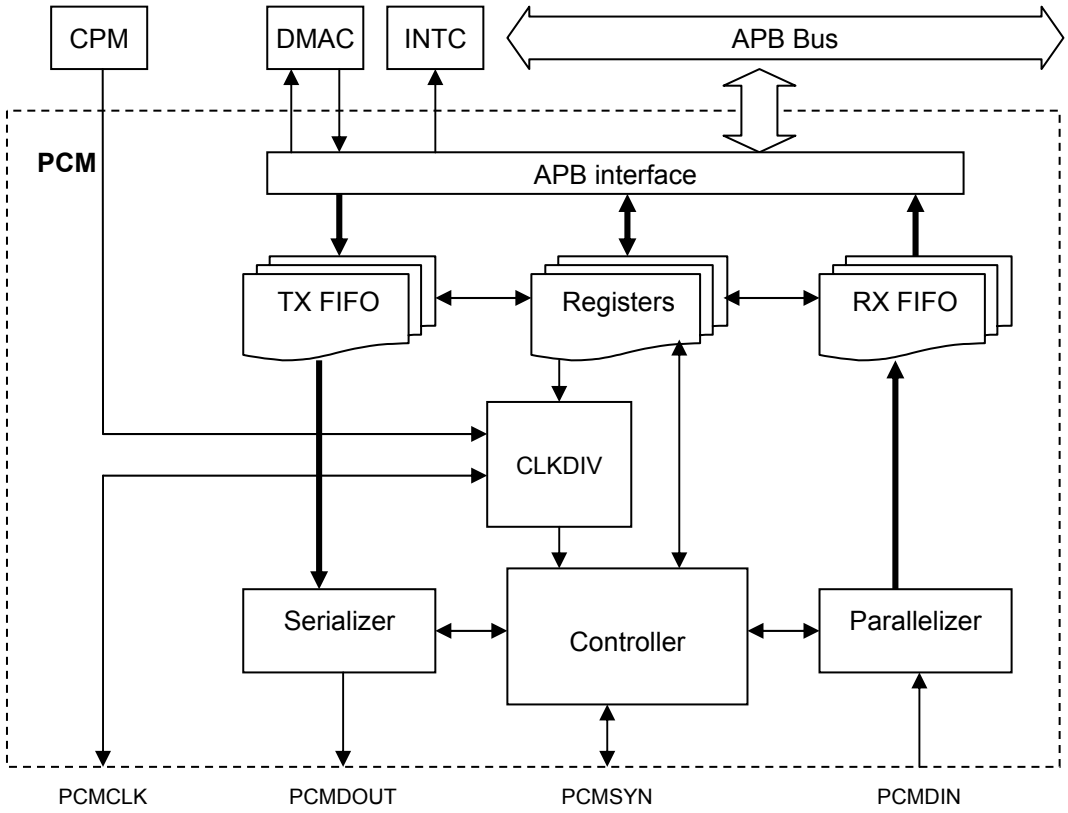
There are all 4 pins used to connect between PCM interface and an external device. They are listed and described in Table 28-1.

Table 28-1 PCM Interface Pins Description

Name	I/O	Description
PCMCLK	Input/Output	PCM Serial clock Line signal input/output
PCMSYN	Input/Output	PCM sync signal input/output
PCMDOUT	Output	PCM Serial data output
PCMDIN	Input	PCM Serial data input

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28.3 Block Diagram



28.4 Register Description

Table 28-2 PCM0 Registers Description

Name	Description	RW	Reset Value	Address	Size
PCMCTL0	PCM Control Register	RW	0x00000000	0x10071000	32
PCMCFG0	PCM Configure Register	RW	0x00000110	0x10071004	32
PCMDP0	PCM FIFO Data Port Register	RW	0x00000000	0x10071008	32
PCMINTC0	PCM Interrupt Control Register	RW	0x00000000	0x1007100c	32
PCMINTS0	PCM Interrupt Status Register	RW	0x00000100	0x10071010	32
PCMDIV0	PCM Clock Divide Register	RW	0x00000001	0x10071014	32

Table 28-3 PCM1 Registers Description

Name	Description	RW	Reset Value	Address	Size
PCMCTL1	PCM Control Register	RW	0x00000000	0x10074000	32

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PCMCFG1	PCM Configure Register	RW	0x00000110	0x10074004	32
PCMDP1	PCM FIFO Data Port Register	RW	0x00000000	0x10074008	32
PCMINTC1	PCM Interrupt Control Register	RW	0x00000000	0x1007400c	32
PCMINTS1	PCM Interrupt Status Register	RW	0x00000100	0x10074010	32
PCMDIV1	PCM Clock Divide Register	RW	0x00000001	0x10074014	32

28.4.1 PCM Control Register (PCMCTL)

PCMCTL0, PCMCTL1 **0x10071000, 0x10074000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						ERDMA	ETDMA	LSMP	ERPL	EREC	FLUSH	RST	SYNEN	CLKEN	PCMEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Writing has no effect, read as zero.	R
9	ERDMA	Receive DMA Enable. This bit is used to enable or disable the DMA during receiving audio data. **ERDMA** / **Receive DMA** 0 / Disabled. 1 / Enabled.	RW
8	ETDMA	Transmit DMA Enable. This bit is used to enable or disable the DMA during transmit audio data. **ETDMA** / **Transmit DMA** 0 / Disabled. 1 / Enabled.	RW
7	LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. **LSMP** / **CODEC used** 0 / Play ZERO sample when TX FIFO underflow. 1 / Play last sample when TX FIFO underflow.	RW
6	ERPL	Enable Playing Back function. This bit is used to disable or enable the audio sample data transmitting. **ERPL** / **Description** 0 / PCM Playing Back Function is Disabled. 1 / PCM Playing Back Function is Enabled.	RW
5	EREC	Enable Recording Function. This bit is used to disable or enable the audio sample data receiving. **EREC** / **Description**	RW

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			0	PCM Recording Function is Disabled.	
			1	PCM Recording Function is Enabled.	
4	FLUSH	FIFO Flush. Write 1 to this bit flush transmit/receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.			W
3	RST	Reset PCM. Write 1 to this bit reset PCM registers and FIFOs. Writing 0 to this bit has no effect and this bit is always reading 0.			W
2	Reserved	Writing has no effect, read as zero.			R
1	CLKEN	Enable the serial clock division logic. Must be HIGH for the PCM to operate.			RW
0	PCMEN	Enable PCM function. This bit is used to enable or disable the PCM function.			RW

PCMENB	Description
0	Disable PCM Controller.
1	Enable PCM Controller.

28.4.2 PCM Configuration Register (PCMCFG)

PCMCFG0, PCMCFG1 **0x10071004, 0x10074004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	SLOT		ISS	OSS	IMSBPOS	OMSBPOS	RFTH				TFTH				PCMMOD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14:13	SLOT	Controls the amount of valid PCM timeslot in one PCMSYN frame.	RW
12	ISS	Input Sample Size. These bits reflect input sample data size to memory or register. The data sizes supported are: 8/16bits. The sample data is LSB-justified in memory/register.	RW
11	OSS	Output Sample Size. These bits reflect output sample data size from memory or register. The data sizes supported are: 8/16 bits. The sample data is LSB-justified in memory/register.	RW
10	IMSBPOS	Controls the position of the MSB bit in the serial input stream relative	RW

ISS	Sample Size
0	8 bit
1	16 bit

OSS	Sample Size
0	8 bit
1	16 bit

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		to the PCMSYN signal. 0: MSB is captured on the falling edge of PCMCLK during the same cycle that PCMSYNC is high 1: MSB is captured on the falling edge of PCMCLK during the cycle after the PCMSYNC is high	
9	OMSBPOS	Controls the position of the MSB bit in the serial output stream relative to the PCMSYN signal. 0: MSB sent during the same clock that PCMSYN is high 1: MSB sent on the next PCMSCLK cycle after PCMSYNC is high	RW
8:5	RFTH	Receive FIFO threshold for interrupt or DMA request. Determines when the RFS flags go active for the RXFIFO. When the sample number in receive FIFO, indicated by PCMINTS.RFL, is great than the threshold value, PCMINTS.RFS is set. Larger RFTH value provides lower DMA/interrupt request frequency but have more risk to involve receive FIFO overflow. The optimum value is system dependent.	RW
4:1	TFTH	Transmit FIFO threshold for interrupt or DMA request. Determines when the TFS flags go active for the TXFIFO. When the sample number in transmit FIFO, indicated by PCMINTS.TFL, is less than the threshold value, PCMINTS.TFS is set. Smaller TFTH value provides lower DMA/interrupt request frequency but have more risk to involve transmit FIFO underflow. The optimum value is system dependent.	RW
0	PCMMOD	PCM mode select. 0: Master mode; 1: Slave mode.	RW

28.4.3 PCM FIFO DATA PORT REGISTER (PCMDP)

PCMDP0, PCMDP1 **0x10071008, 0x10074008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DATA	FIFO port. When write to it, data is push to the transmit FIFO. When read from it, data is pop from the receiving FIFO.	RW

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28.4.4 PCM INTERRUPT CONTROL REGISTER (PCMINTC)

PCMINTCR0, PCMINTCR1 **0x1007100c, 0x1007400c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												ETFS	ETUR	ERFS	EROR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	ETFS	Enable TFS Interrupt. This bit is used to control the TFS interrupt enable or disable. **ETFS** / **TFS Interrupt** 0 / Disabled. 1 / Enabled.	RW
2	ETUR	Enable TUR Interrupt. This bit is used to control the TUR interrupt enable or disable. **ETUR** / **TUR Interrupt** 0 / Disabled. 1 / Enabled.	RW
1	ERFS	Enable RFS Interrupt. This bit is used to control the RFS interrupt enable or disable. **ERFS** / **RFS Interrupt** 0 / Disabled. 1 / Enabled.	RW
0	EROR	Enable ROR Interrupt. This bit is used to control the ROR interrupt enable or disable. **EROR** / **ROR Interrupt** 0 / Disabled. 1 / Enabled.	RW

28.4.5 PCM INTERRUPT STATUS REGISTER (PCMINTS)

PCMINTS0, PCMINTS1 **0x10071010, 0x10074010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	RSTS	TFL						TFS	TUR	RFL				RFS	ROR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:15</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>14</td><td>RSTS</td><td>Soft reset / flush state.
0: Nothing / reset or flush operation has completed
1: reset or flush operation has not completed</td><td>R</td></tr>
<tr><td>13:9</td><td>TFL</td><td>Transmit FIFO Level. The bits indicate the amount of valid PCM data in Transmit FIFO.</td><td>R</td></tr>
<tr><td>8</td><td>TFS</td><td>Transmit FIFO Service Request. This bit indicates that transmit FIFO level exceeds TFL threshold which is controlled by PCMCFG.TFTH When TFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table>
<tr><th>TFS</th><th>Description</th></tr>
<tr><td>0</td><td>Transmit FIFO level exceeds TFL threshold.</td></tr>
<tr><td>1</td><td>Transmit FIFO level at or below TFL threshold.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>7</td><td>TUR</td><td>Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run.
<table>
<tr><th>TUR</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>When read, indicates under-run has not been found.</td></tr>
<tr><td>When write, clear itself.</td></tr>
<tr><td rowspan="2">1</td><td>When read, indicates data has even been read from empty transmit FIFO.</td></tr>
<tr><td>When write, not effects.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>6:2</td><td>RFL</td><td>Receive FIFO Level. The bits indicate the amount of valid PCM data in Receive FIFO.</td><td>R</td></tr>
<tr><td>1</td><td>RFS</td><td>Receive FIFO Service Request. This bit indicates that receive FIFO level is or not below RFL threshold which is controlled by PCMCFG.RFTH. When RFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table>
<tr><th>RFS</th><th>Description</th></tr>
<tr><td>0</td><td>Receive FIFO level below RFL threshold.</td></tr>
<tr><td>1</td><td>Receive FIFO level at or above RFL threshold.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>0</td><td>ROR</td><td>Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun.
<table>
<tr><th>ROR</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>When read, indicates over-run has not been found.</td></tr>
<tr><td>When write, clear itself.</td></tr>
<tr><td rowspan="2">1</td><td>When read, indicates data has even been written to full receive FIFO.</td></tr>
<tr><td>When write, not effects.</td></tr>
</table></td><td>RW</td></tr>
</table>

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28.4.6 PCM CLOCK DIVIDE REGISTER (PCMDIV)

PCMDIV0, PCMDIV1 **0x10071014, 0x10074014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SYNL						SYNDIV					CLKDIV					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
16:11	SYNL	Controls the length that the PCMSYN based upon the PCMCLK. The length of PCMSYN = (SYNL + 1) * PCMCLK cycle.	RW
10:6	SYNDIV	Controls the frequency of the PCMSYN signal based upon the PCMCLK. PCMSYN = PCMCLK / 8 (SYNDIV + 1).	RW
5:0	CLKDIV	PCMCLK clock divider value minus 1. Controls the divider used to create the PCMCLK based upon the CPM_PCM_SYSCLK. PCMCLK = CPM_PCM_SYSCLK / (CLKDIV + 1).	RW

28.5 PCM Interface Timing

The following figures show the timing relationship for the PCM transfers, Note in all cases. In master mode, the PCMCLK is derived from dividing the input clock, CPM_PCM_SYSCLK, and the PCMSYN is divided depended on the PCMCLK. In slave mode, the PCMCLK and PCMSYN are input from the external device. Data is sampled on the falling edge of the PCMCLK and sent out on the rising edge of the PCMCLK. The PCMSYN signal determines when the next data sample is to be transferred between the controller and the external device. Also, the PCMSYN signal as seen in the figure can be one bit time or a long bit time controlled by PCMDIV.SYNL. The PCMSYN frequency controlled by PCMDIV.SYNDIV is usually the sample rate. There are some variations controlled by PCMCFG.ISS, PCMCFG.OSS and PCMCFG.SLOT to accommodate 8 / 16bit sample sizes and multi-slot transmission.

28.5.1 Short Frame SYN

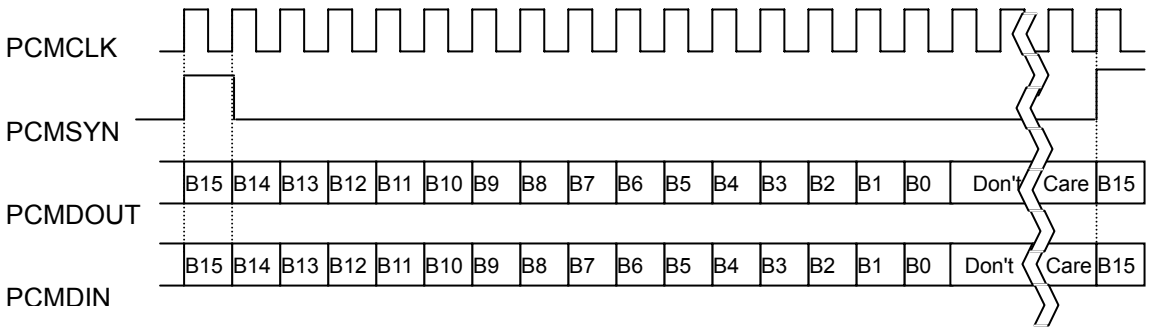


Figure 28-1 Short Frame SYN Timing (Shown with 16bit Sample)

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NOTE: Figure 28-1 shows a PCM transfer with the MSB configured to be coincident with the PCMSYN.

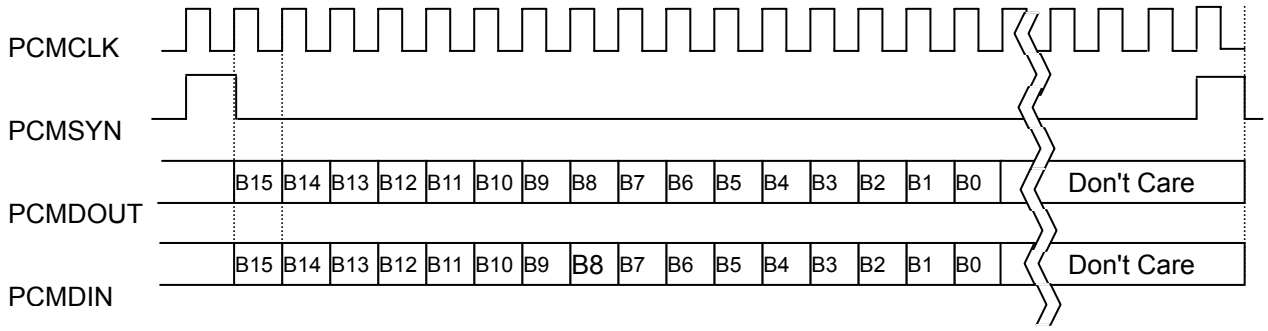


Figure 28-2 Short Frame SYN Timing (Shown with 16bit Sample)

NOTE: Figure 28-2 shows a PCM transfer with the MSB configured one shift clock after the PCMSYN.

28.5.2 Long Frame SYN

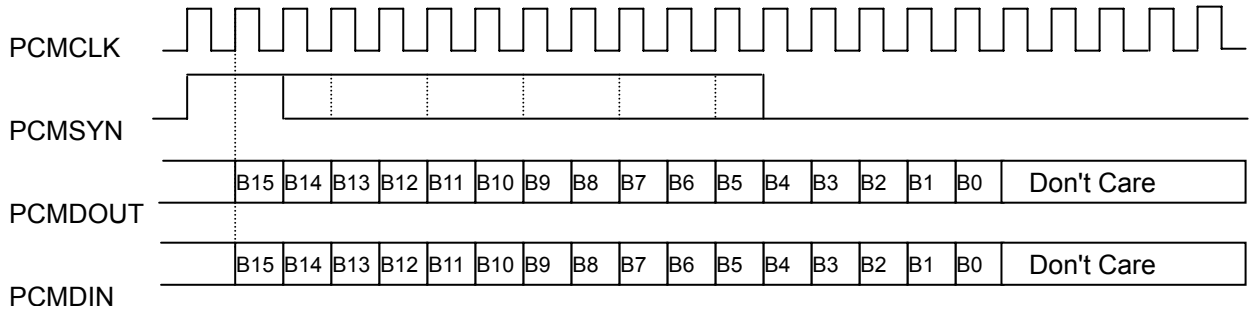


Figure 28-3 Long Frame SYN Timing (Shown with 16bit Sample)

NOTE: Figure 28-3 shows a PCM transfer with the MSB configured one shift clock after the PCMSYN.

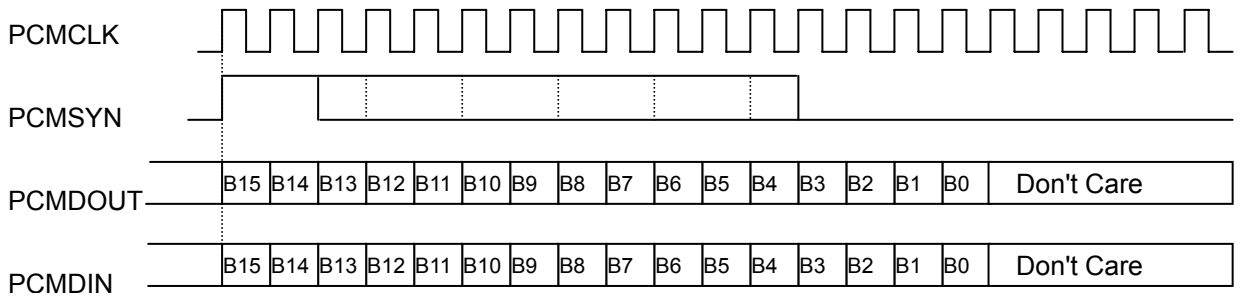


Figure 28-4 Long Frame SYN Timing (Shown with 16bit Sample)

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NOTE: Figure 28-4 shows a PCM transfer with the MSB configured to be coincident with the PCMSYN.

28.5.3 Multi-Slot Operation

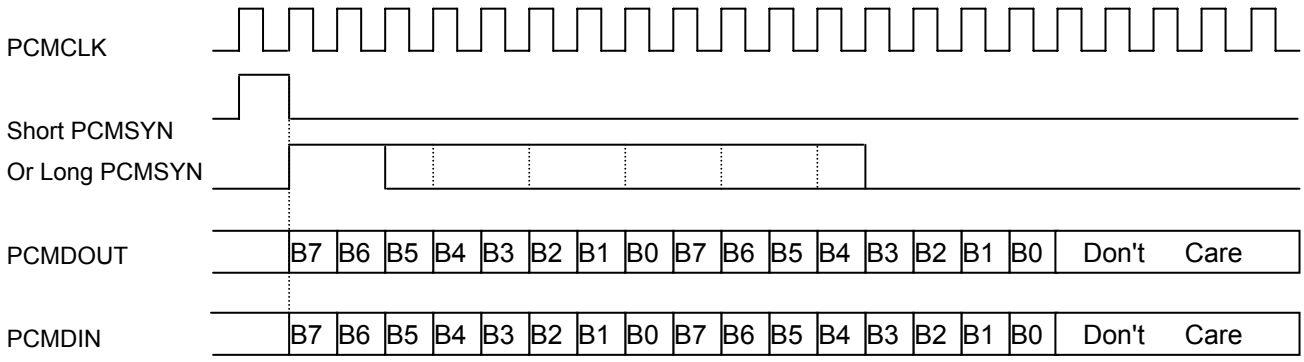
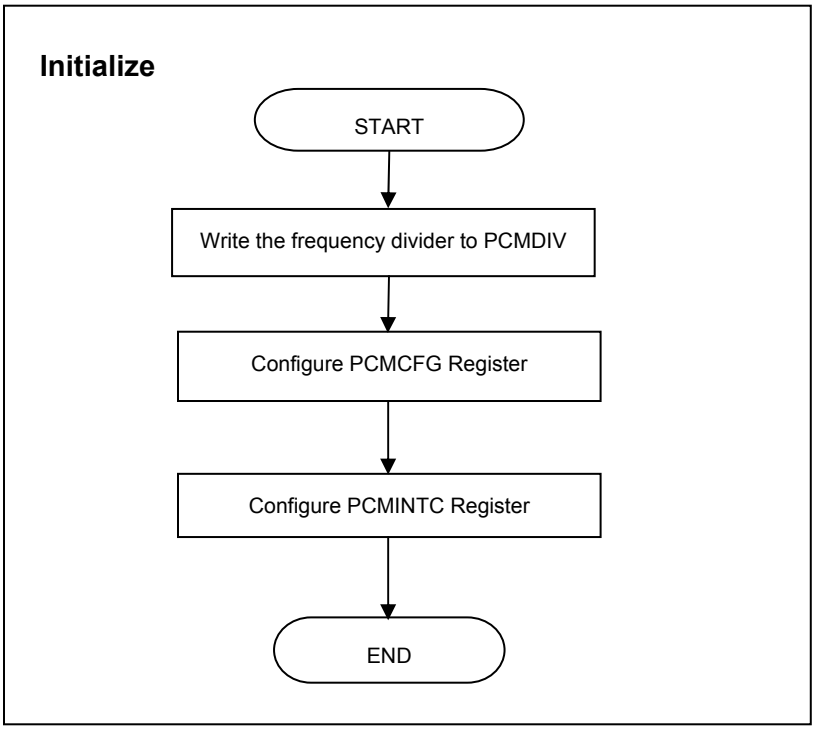


Figure 28-5 Multi-Slot Frame SYN Timing (Shown with two Slots and 8bit Sample)

28.6 PCM Operation

28.6.1 PCM Initialization

At power-on or other hardware reset (WDT and etc), PCM is disabled. Software must initiate PCM after power-on or reset.



For further details, see the corresponding register description sections.

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28.6.2 Audio Replay

Outgoing audio sample data is written to PCM transmit FIFO from processor via store instruction or from memory via DMA. PCM then takes the data from the FIFO, serializes it, and sends it over the serial wire PCMDOUT to an external DEVICE.

The audio transmission is enabled automatically when the PCM is enabled by set PCMCTL.PCMEN. And PCMCTL.ERPL must be 1. If PCMCTL.ERPL is 0, value of zero is sent to external DEVICE even if there are samples in transmit FIFO. At least one audio sample data in the transmit FIFO. If the transmit FIFO is empty, value of zero or last sample depends on AICFR.LSMP, is send to external DEVICE even if PCMCTL.ERPL is 1.

Here is the audio replay flow:

1 Configure the external DEVICE as needed.
2 Initialize PCM and configure the register.
3 Write 1 to PCMCTL.PCMEN and PCMCTL.CLKEN.
4 Fill sample data to the transmit FIFO. Repeat this till finish all sample data. In this procedure, please control the FIFO to make sure no FIFO under-run and other errors happen. When the transmit FIFO under-run, noise or pause may be heard in the audio replay, PCMINTS.TUR is 1, and if PCMINTC.ETUR is 1, PCM issues an interrupt. Please reference to 28.6.4 for detail description on FIFO.
5 Write 1 to PCMCTL.ERPL. It is suggested that at least a frame of PCM data is pre-filled in the transmit FIFO to prevent FIFO under-run flag (PCMINTS.TUR).
6 Waiting for PCMINTS.TFL change to 0. So that all samples in the transmit FIFO has been replayed, then we can have a clean start and write 0 to PCMCTL.ERPL.

28.6.3 Audio Record

Incoming audio sample data is received from PCMDIN serially and converted to parallel word and stored in PCM receive FIFO. Then the data can be taken from the FIFO to processor via load instruction or to memory via DMA.

The audio recording is enabled automatically when the PCM is enabled by set PCMCTL.PCMEN, And PCMCTL.EREC must be 1. If PCMCTL.EREC is 0, the received data is discarded even if there are rooms in the receive FIFO. At least one room left in the receive FIFO. If the receive FIFO is full, the received data is discarded even if PCMCTL.EREC is 1.

Here is the audio record flow:

1 Configure the external DEVICE as needed.
   a Initialize PCM and configure the register.
   b Write 1 to PCMCTL.PCMEN and PCMCTL.CLKEN.
2 Write 1 to PCMCTL.EREC. Make sure there are rooms available in the receive FIFO before set PCMCTL.EREC. Usually, it should empty the receive FIFO by fetch data from it before set PCMCTL.EREC.

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3 Take sample data form the receive FIFO. Repeat this till the audio finished. In this procedure, please control the FIFO to make sure no FIFO over-run and other errors happen. When the receive FIFO over-run, same recorded audio samples will be lost, PCMINTS.ROR is 1, and if PCMINTC.EROR is 1, PCM issues an interrupt. Please reference to 28.6.4 for detail description on FIFO.

4 Write 0 to AICCR.EREC.

5 Take sample data from the receive FIFO until PCMINTS.RFL change to 0. So that all samples in the receive FIFO has been taken away, then we can have a clean start up next time. When the receive FIFO is empty, read from it returns zero.

28.6.4 FIFOs operation

PCM has two FIFOs, one for transmitting and one for receiving. The FIFOs are in 16 bits width and 16 entries depth, one entry for keep one sample regardless of the sample size. PCMDP.DATA provides the access point for processor/DMA to write to transmit FIFO and read from receive FIFO. One time access to PCMDP.DATA process one sample. The sample data should be put in LSB (Least Significant Bit) in memory or processor registers. For transmitting, bits exceed sample are discarded. For receiving, these bits are set to 0. Figure 6 illustrates the FIFOs access.

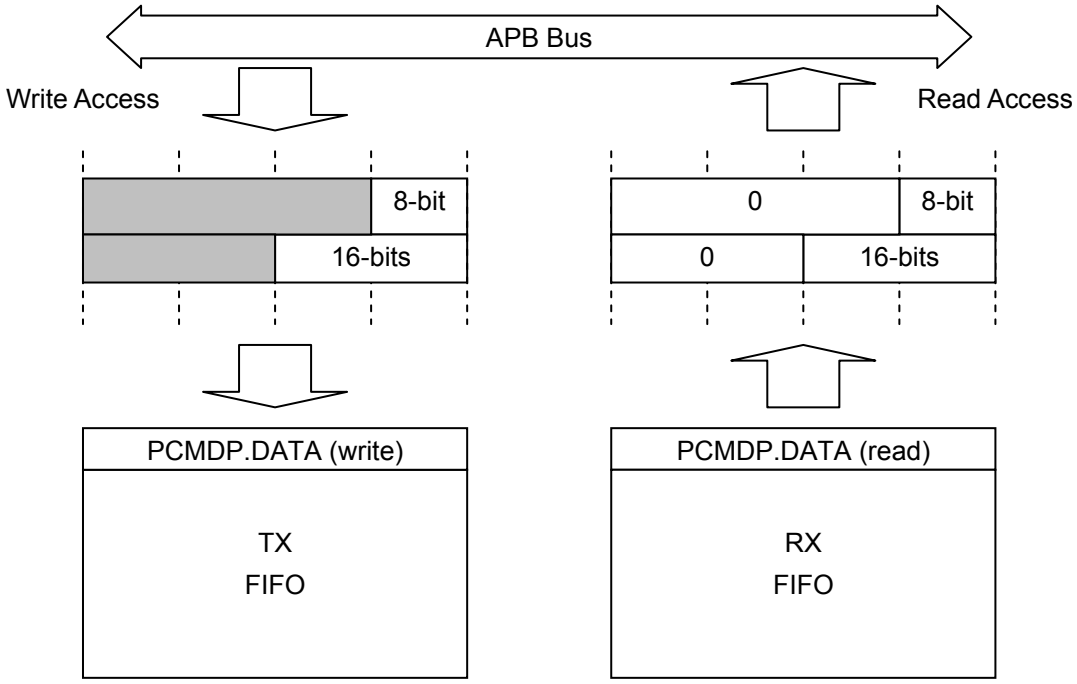


Figure 28-6 Transmitting/Receiving FIFO access via APB Bus

The software and bus initiator must guarantee the right sample placement at the bus.

In case of DMA bus initiator, One 16 bits sample occupies one 16-bits half word in memory, so 16-bits width DMA must be used. One 8-bits sample occupies one byte in memory, and use 8-bits width DMA.

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28.6.5 Data Flow Control

There are three approaches provided to control/synchronize the incoming/outgoing data flow.

28.6.5.1 Polling and Processor Access

PCMINTS.RFL and PCMINTS.TFL reflect how many samples exist in receiving and transmitting FIFOs. Through read these register fields, processor can detect when there are samples in receiving FIFO and then load them from the RxFIFO, and when there are rooms in transmitting FIFO and then store samples to the TxFIFO.

Polling approach is in very low efficiency and is not recommended.

28.6.5.2 Interrupt and Processor Access

Set proper values to PCMCFG.TFTH and PCMCFG.RFTH, the FIFO interrupts trig thresholds. Set PCMINTC.ETFS and/or PCMINTC.ERFS to 1 to enable transmitting and/or receiving FIFO level trigger interrupts. When the interrupt found, it means there are rooms or samples in the TX or RX FIFO, and processor can store or load samples to or from the FIFO.

Interrupt approach is more efficient than polling approach.

28.6.5.3 DMA Access

To enable DMA operation, set PCMCTL.ERDMA and PCMCTL.ETDMA to 1 for transmit and receive respectively. It also needs to allocate two channels in DMA controller for data transmitting and receiving respectively. Please reference to DMAC spec for the details.

The PCMCFG.TFTH and PCMCFG.RFTH are used to set the transmitting and receiving FIFO level thresholds, which determine the issuing of DMA request to DMA controller. To respond the request, DMAC initiator and controls the data movement between memory and TX/RX FIFO.

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28.6.6 PCM Serial Clocks and Sampling Frequencies

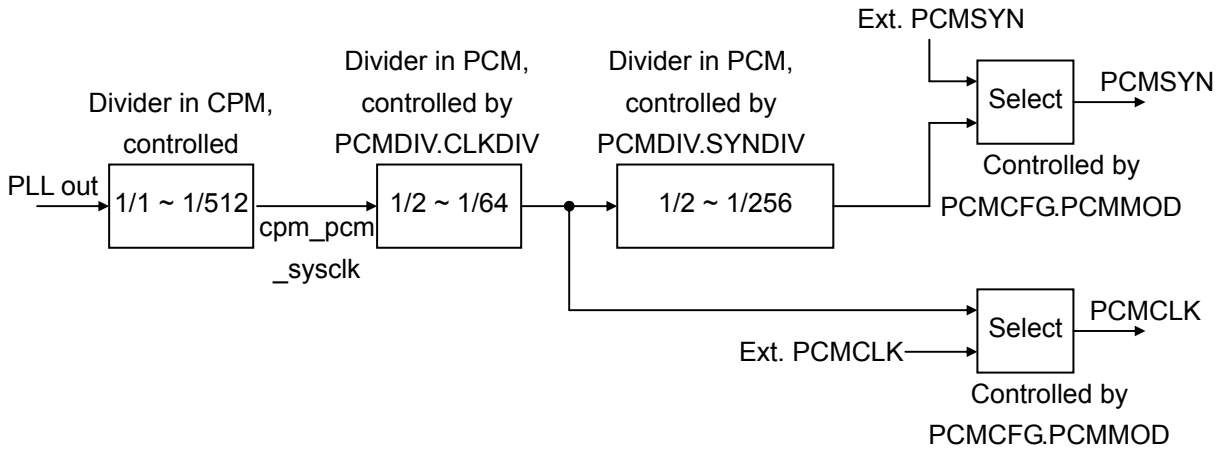


Figure 28-7 PCMCLK and PCMSYN generation scheme

28.6.7 Interrupts

The following status bits, if enabled, interrupt the processor:

- Receive FIFO Service (PCMINTS.RFS). It's also DMA Request.
- Transmit FIFO Service (PCMINTS.TFS). It's also DMA Request.
- Transmit Under-Run (PCMINTS.TUR).
- Receive Over-Run (PCMINTS.ROR).

For further details, see the corresponding register description sections.

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29 SAR A/D Controller

29.1 Overview

The A/D in falcon is CMOS low-power dissipation 12bit touch screen SAR analog to digital converter. It operates with 3.3/1.2V power supply. It is developed as an embedded high resolution ADC targeting to the 65nm CMOS process and has wide application in portable electronic devices, high-end home entertainment center, communication systems and so on.

The SAR A/D controller is dedicated to control A/D to work at three different modes: Touch Screen (measure pen position and pen down pressure), Battery (check the battery power), and two auxiliary input. Touch Screen can transfer the data to memory though the DMA or CPU. Battery and two auxiliary input can transfer the data to memory though CPU.

Features:

- 7 Channels
- Resolution: 12-bit
- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±0.5 LSB
- Resolution/speed: up to 2Msps
- Max Frequency: 200k
- Low power dissipation: 1.5mW(worst)
- Support 4-wire and 5-wire touch panel measurement (Through pin XP, XN, YP, YN and AUX2)
- Support multi-touch detect
- Support write control command by software
- Support voltage measurement (Through pin VBAT)
- Support two auxiliary input (Through pin AUX1, AUX2)
- Single-end and Differential Conversion Mode
- Auto X/Y, X/Y/Z1/Z2 and X/Y/Z1/Z2/X2/Y2 position measurement
- Support external touch screen controller
- Pin Description

Table 29-1 SADC Pin Description

Name	I/O	Description
XN	AI	Touch screen analog differential X- position input
YN	AI	Touch screen analog differential Y- position input
XP	AI	Touch screen analog differential X- position input
YP	AI	Touch screen analog differential Y- position input
VBAT	AI	VBAT direct input *[1]
AUX1	AI	Auxiliary Input

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AUX2	AI	Auxiliary Input

NOTE:

*[1]: Users who already deployed resistor networks on board level can use VBAT to direct measure the battery value.

29.2 Register Description

In this section, we will describe the registers in SAR A/D controller. Following table lists all the register definitions. All registers' 32bit addresses are physical addresses. And detailed function of each register will be described below.

Table 29-2 SADC Register Description

Name	Description	RW	Reset Value	Address	Access Size
ADENA	ADC Enable Register	RW	0x80	0x10070000	8
ADCFG	ADC Configure Register	RW	0x00040000	0x10070004	32
ADCTRL	ADC Control Register	RW	0x3F	0x10070008	8
ADSTATE	ADC Status Register	RW	0x00	0x1007000C	8
ADSAME	ADC Same Point Time Register	RW	0x0000	0x10070010	16
ADWAIT	ADC Wait Time Register	RW	0x0000	0x10070014	16
ADTCH	ADC Touch Screen Data Register	RW	0x00000000	0x10070018	32
ADVDAT	ADC VBAT Data Register	RW	0x0000	0x1007001C	16
ADADAT	ADC AUX Data Register	RW	0x0000	0x10070020	16
ADCLK	ADC Clock Divide Register	RW	0x00041000	0x10070028	32
ADCMD	ADC Command Register	RW	0x00000000	0x10070024	32
ADTEST	ADC TEST Register	RW	0x00000000	0x1007002C	32

29.2.1 ADC Enable Register (ADENA)

The register ADENA is used to trigger A/D to work.

ADENA **0x10070000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								POWER	SLP_MD	Reserved		PENDEN	TCHEN	VBATEN	AUXEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R

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7	POWER	SADC Power control bit. 1: SADC power down 0: SADC power on When POWER is set from 1 to 0, you should wait at least 2ms to enable SADC.	RW
6	SLP_MD	SLEEP Mode Control. 1:Enter sleep mode 0:Exit sleep mode	RW
5:4	Reserved	Writing has no effect, read as zero.	R
3	PENDEN	Pen Down Detect Enable control. 0: disable 1: enable	RW
2	TCHEN	Touch Screen Enable Control. 0: disable 1: enable	RW
1	VBATEN	VBAT Enable Control. No matter TCHEN is 1 or 0, VBATEN can be set to 1 to sample the voltage of battery, and when the value of voltage is ready, PBATEN will be cleared by hardware auto.	RW
0	AUXEN	AUX n Enable Control. No matter TCHEN is 1 or 0, AUXEN can be set to 1 to sample the voltage of AUX1, AU2 or AUX3, and when the value of voltage is ready. AUXEN will be cleared by hardware auto.	RW

NOTES:

1 TCHEN, VBATEN and AUXEN can be set to 1 at the same time. The priority of the three mode is AUX > VBAT > TCH.

2 SLP_MD, TCHEN can be set to 1 at the same time. The priority of the two mode is SLP_MD > TCH.

3 When VBATEN and AUXEN are all 0, SLP_MD can be set to 1.

29.2.2 ADC Configure Register (ADCFG)

The register ADCFG is used to configure the A/D.

ADCFG **0x10007004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPZZ	Reserved							Wire_cel_r	Cmd_sel_r	PRU						DMA_EN	XYZ	SNUM				Reserved									CMD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31</td><td>SPZZ*1</td><td>The $X_dY_dZ_mZ_n$ of different point measure can be different.
But the $X_dY_dZ_mZ_n$ of the same point measure can be same or different.
0: The $X_dY_dZ_mZ_n$ of the same point measure is all the same
(X_dY_dZ1Z2, X_dY_dZ1Z2, X_dY_dZ1Z2, X_dY_dZ1Z2 … X_dY_dZ1Z2)
1: The $X_dY_dZ_mZ_n$ of the same point measure maybe different
(X_dY_dZ1Z2, X_dY_dZ3Z4, X_dY_dZ3Z4, X_dY_dZ1Z2 … X_dY_dZ1Z2)</td><td>RW</td></tr>
<tr><td>30:24</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>23</td><td>WIRE_SEL</td><td>0: use 4-wire touch panel
1: use 5-wire touch panel</td><td>RW</td></tr>
<tr><td>22</td><td>CMD_SEL</td><td>0: use hardware inter command to control touch panel
1: use software write command to control touch panel</td><td>RW</td></tr>
<tr><td>21:16</td><td>RPU</td><td>Internal Pull-up resistor for Pen Detection.
6’b111111: 64kΩ/63 = 1.02kΩ (least sensitive)
6’b111110: 64KΩ/62 = 1.03KΩ
… (pull-up = 64kΩ / binary value of RPU)
6’b000010: 64KΩ/2 = 32KΩ
6’b000001: 64kΩ/1 = 64kΩ (most sensitive) default
6’b000000: RESERVED (do not use this setting)</td><td>RW</td></tr>
<tr><td>15</td><td>DMA_EN</td><td>When A/D is used as Touch Screen , DMA_EN is used as follows:
0: The sample data is read by CPU
1: The sample data is read by DMA</td><td>RW</td></tr>
<tr><td>14:13</td><td>XYZ</td><td>When A/D is used in Touch Screen mode, XYZ is used as follows:
<table>
<tr><th>XYZ</th><th>Measure</th></tr>
<tr><td>00</td><td>$X_s \rightarrow Y_s$</td></tr>
<tr><td>01</td><td>$X_d \rightarrow Y_d$</td></tr>
<tr><td>10</td><td>$X_d \rightarrow Y_d \rightarrow Z1_d \rightarrow Z2_d$ or $X_d \rightarrow Y_d \rightarrow Z3_d \rightarrow Z4_d$</td></tr>
<tr><td>11</td><td>$X_d \rightarrow Y_d \rightarrow Z1_d \rightarrow Z2_d \rightarrow X2 \rightarrow Y2$ or
$X_d \rightarrow Y_d \rightarrow Z3_d \rightarrow Z4_d \rightarrow X2 \rightarrow Y2$</td></tr>
</table></td><td>RW</td></tr>
<tr><td>12:10</td><td>SNUM</td><td>The number of repeated sampling one point. When A/D is used as Touch Screen, SNUM is used as follows:
<table>
<tr><th>SNUM</th><th>Number</th></tr>
<tr><td>000</td><td>Reserved</td></tr>
<tr><td>001</td><td>1</td></tr>
<tr><td>010</td><td>2</td></tr>
<tr><td>011</td><td>3</td></tr>
<tr><td>100</td><td>4</td></tr>
<tr><td>101</td><td>5</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>9:2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

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1:0	CMD	CMD is used to choose the current sample command when ADENA.AUXEN is set to 1. CMD: 00 Reserved; 01 Measure AUX1 voltage; 10 Measure AUX2 voltage; 11 Reserved	RW

NOTE:

*1: X_s, Y_s means the reference mode of X, Y is single-end mode.

X_d, Y_d, $Z1_d$, $Z2_d$, $Z3_d$, Z4d means the reference mode of X, Y, Z1, Z2, Z3, Z4 is differential mode.

When you measure Xs you need to make sure that X-plate is driven by external DC power.

When you measure Ys you need to make sure that Y-plate is driven by external DC power.

29.2.3 ADC Control Register (ADCTRL)

The register ADCTRL is used to control A/D to work.

ADCTRL **0x10070008**

Bit	31:6	5	4	3	2	1	0
	Reserved	SLPENDM	PENDM	PENUM	DTCHM	VRDYM	ARDYM
RST	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	SLPENDM	In SLEEP mode pen down interrupt mask. 0: enabled 1: masked	RW
4	PENDM	Pen down interrupt mask. 0: enabled 1: masked	RW
3	PENUM	Pen up interrupt mask. 0: enabled 1: masked	RW
2	DTCHM	Touch Screen Data Ready interrupt mask. 0: enabled 1: masked	RW
1	VRDYM	VBAT data ready interrupt mask. 0: enabled	RW

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		1: masked	
0	ARDYM	AUX data ready interrupt mask. 0: enabled 1: masked	RW

29.2.4 ADC Status Register (ADSTATE)

The register ADSTATE is used to keep the status of A/D.

ADSTATE **0x1007000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SLP_RDY	Reserved	SLPEND	PEND	PENU	DTCH	VRDY	ARDY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	SLP_RDY	Sleep state bit. 1:The set of sleep mode is ready 0:The set of sleep mode is not ready	R
6	Reserved	Writing has no effect, read as zero.	R
5	SLPEND	In SLEEP mode pen down interrupt flag. Write 1 to this bit, the bit will clear this bit. 1: active 0: not active	RW
4	PEND	Pen down interrupt flag. Write 1 to this bit, the bit will clear this bit. 1: active 0: not active	RW
3	PENU	Pen up interrupt flag. Write 1 to this bit, the bit will clear this bit. 1: active 0: not active	RW
2	DTCH	Touch screen data ready interrupt flag. Write 1 to this bit, the bit will clear this bit. 1: active 0: not active	RW
1	VRDY	VBAT data ready interrupt flag. Write 1 to this bit, the bit will clear this bit. 1: active 0: not active	RW
0	ARDY	AUX data ready interrupt flag. Write 1 to this bit, the bit will	RW

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		clear this bit. 1: active 0: not active	

29.2.5 ADC Same Point Time Register (ADSAME)

The register ADSAME is used to store the interval time between repeated sampling the same point. The clock of the counter is clk_us.

ADSAME **0x10070010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

29.2.6 ADC Wait Pen Down Time Register (ADWAIT)

The register ADWAIT is used to store the interval time of wait pen down. And the register can be used as the interval time among the different point. The clock of the counter is clk_us.

ADWAIT **0x10070014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																WCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

29.2.7 ADC Touch Screen Data Register (ADTCH)

The read-only ADTCH is corresponded to 16x32 bit FIFO, it keep the sample data for touch screen. 0~11 bits are data, 15 bit is data type. 16~27 bits are data, 31 bit is data type. When write to the register, DATA will be clear to 0.

ADTCH **0x10070018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE1	Reserved															TYPE0	Reserved														
			TDATA1																TDATA0													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31	TYPE1	Type of the Touch Screen Data1. When A/D is used as Touch Screen, ADCFG.XYZ=10 or XYZ=11: TYPE1=1: X_d→Y_d→Z1→Z2 or X_d→Y_d→Z1→Z2→X2→Y2; TYPE1=0: X_d→Y_d→Z3→Z4 or X_d→Y_d→Z3→Z4→X2→Y2. When A/D is used as Touch Screen, ADCFG.XYZ=00 or XYZ=01: TYPE1=0.	RW
30:28	Reserved	Writing has no effect, read as zero.	R
27:16	TDATA1	The concert data of touch screen A/D.	RW
15	TYPE0	Type of the Touch Screen Data2. When A/D is used as Touch Screen, ADCFG.XYZ=10 or XYZ=11: TYPE0=1: X_d→Y_d→Z1→Z2 or X_d→Y_d→Z1→Z2→X2→Y2; TYPE0=0: X_d→Y_d→Z3→Z4 or X_d→Y_d→Z3→Z4→X2→Y2. When A/D is used as Touch Screen, ADCFG.XYZ=00 or XYZ=01: TYPE0=0.	RW
14:12	Reserved	Writing has no effect, read as zero.	R
11:0	TDATA0	The concert data of touch screen A/D.	RW

NOTES:

1 When A/D is used as Touch Screen, ADCFG.XYZ=00.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
0	000	Y_s	0	000	X_s

2 When A/D is used as Touch Screen, ADCFG.XYZ=01.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
0	000	Y_d	0	000	X_d

3 When A/D is used as Touch Screen, ADCFG.XYZ=10.TYPE=1.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
1	000	Y_d	1	000	X_d
1	000	$Z2_d$	1	000	$Z1_d$

Users need to read twice to get the whole data. The first time reading gets the data Yd and Xd. The second time reading gets the data Z2d and Z1d.

The touch pressure measurement formula is as follows: (You can use formula 1 or formula 2.)

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$$R_{TOUCH} = R_{X\text{-}Plate} \bullet \frac{X\text{-}Position}{4096}\left(\frac{Z_2}{Z_1} - 1\right) \quad (1)^{*1}$$

$$R_{TOUCH} = \frac{R_{X\text{-}Plate} \bullet X\text{-}Position}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y\text{-}Plate} \bullet \left(1 - \frac{Y\text{-}Position}{4096}\right) \quad (2)^{*1}$$

4 When A/D is used as Touch Screen, ADCFG.XYZ=10.TYPE=0.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
0	000	Y_d	0	000	X_d
0	000	$Z4_d$	0	000	$Z3_d$

Users need to read twice to get the whole data. The first time reading gets the data Y_d and X_d. The second time reading gets the data $Z4_d$ and $Z3_d$.

The touch pressure measurement formula is as follows: (You can use formula 3 or formula 4.)

$$R_{TOUCH} = R_{Y\text{-}Plate} \bullet \frac{Y\text{-}Position}{4096}\left(\frac{Z_4}{Z_3} - 1\right) \quad (3)^{*1}$$

$$R_{TOUCH} = \frac{R_{Y\text{-}Plate} \bullet Y\text{-}Position}{4096}\left(\frac{4096}{Z_3} - 1\right) - R_{X\text{-}Plate} \bullet \left(1 - \frac{X\text{-}Position}{4096}\right) \quad (4)^{*1}$$

5 When A/D is used as Touch Screen, ADCFG.XYZ=11.TYPE=1.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
1	000	Y_d	1	000	X_d
1	000	$Z2_d$	1	000	$Z1_d$
1	000	Y2	1	000	X2

Users need to read thrice to get the whole data. The first time reading gets the data Y_d and X_d. The second time reading gets the data $Z2_d$ and $Z1_d$. The third time reading gets the data Y2 and X2.

6 When A/D is used as Touch Screen, ADCFG.XYZ=11.TYPE=0.
The format of touch screen data is as follows:

Type1	Reserved	Data1	Type0	Reserved	Data0
0	000	Y_d	0	000	X_d
0	000	$Z4_d$	0	000	$Z3_d$
0	000	Y2	0	000	X2

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Users need to read thrice to get the whole data. The first time reading gets the data Y_d and X_d. The second time reading gets the data $Z4_d$ and $Z3_d$. The third time reading gets the data Y2 and X2.

NOTE:

*1: To determine pen or finger touch, the pressure of the touch needs to be determined. Generally, it is not necessary to have very high performance for this test; therefore, the 8-bit resolution mode is recommended (however, calculations will be shown here are in 12bit resolution mode).

$R_{X\text{-plate}}$: Total X-axis resistor value (about 200Ω~ 600Ω)

$R_{Y\text{-plate}}$: Total Y-axis resistor value (about 200Ω~ 600Ω)

X-Position: X-axis voltage sample value

Y-Position: Y-axis voltage sample value

Z1, Z2: Z1, Z2 voltage sample value

Z3, Z4: Z3, Z4 voltage sample value

X2, Y2: X2, Y2 voltage sample value

29.2.8 ADC VBAT Data Register (ADVDAT)

The read-only ADVDAT is a 16-bit register, it keep the sample data of VBAT. 0~11 bits are data.

ADBDAT **0x1007001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				VDATA											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDATA	Data of VBAT A/D convert. When write to the register, DATA will be clear to 0.	RW

The measured voltage V_{BAT} is as follows:

$$V_{BAT} = \frac{VDATA}{4096} \bullet 1.2V$$

29.2.9 ADC AUX Data Register (ADADAT)

The read-only ADADAT is a 16-bit register, it keep the sample data. 0~11 bits are data.

ADSDAT **0x10070020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				ADATA											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	ADATA	Data of AUX. When write to the register, DATA will be clear to 0.	RW

The measured voltage V_{AUX} (V_{AUX1} and V_{AUX2}) is as follows:

$$V_{SAD} = \frac{ADATA}{4096} \bullet AVDD33$$

29.2.10 ADC Clock Divide Register (ADCLK)

The register ADCLK is used to set the A/D's clock dividing number.

ADCLK **0x10070028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKDIV_MS																CLKDIV_US								CLKDIV							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CLKDIV_MS	Dividing number to get ms clock from ADC clock. ms_clk = us_clk / (CLK_MS +1)	RW
15:8	CLKDIV_US	Dividing number to get us clock from ADC clock. us_clk = adc_clk / (CLKDIV_US+1) 0 ≤CLKDIV_10 ≤127	RW
7:0	CLKDIV	Dividing number to get ADC clock from device clock. The A/D works at the frequency between 20KHz and 200KHz. If CLKDIV = N, Then the freq of adc_clk = dev_clk / (N+1). 0 ≤ N ≤ 255	RW

29.2.11 ADC Command Register (ADCMD)

ADC Command Register ADCMD is used for write touch screen control command by software. Then, if the cmd_sel_r = 1, the controller will read ADCMD's command, then use command to control touch screen. The controller has 32x32 bit FIFO to store commands, the command format like this.

ADCMD **0x10070024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIL	RPU					XPSUP	XNSUP	YPSUP	XPGRU	XNGRU	YNGRU	VREFNAUX	VREFNXN	VREFNXP	VREFNYN	VREFPVDD33	VREFPAUX	VREFPXN	VREFPXP	VREFPYP	XPADC	XNADC	YPADC	YNADC	WIPEADC	AUX2ADC	AUX1ADC	RPUWP	RPUXP	RPUYP	APIL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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its	Name	Description	RW
31	PIL	Current used for pressure measurement. 0: Ip = 200μA(default) 1: Ip = 400μA	RW
30:26	RPU	Internal Pull-up resistor for Pen Detection.	RW
25	XPSUP	XP to TPVDD control Switch. 0: open; 1:close.	RW
24	XNSUP	XN to TPGND control Switch. 0: open; 1:close.	RW
23	YPSUP	YP to TPVDD control Switch. 0: open; 1:close.	RW
22	XPGRU	XP to TPGND control Switch. 0: open; 1:close.	RW
21	XNGRU	XN to TPGND control Switch. 0: open; 1:close.	RW
20	YNGRU	YN to TPGND control Switch. 0: open; 1:close.	RW
19	VREFNAUX	ADC low voltage reference to AUX control switch. 0: open; 1: close.	RW
18	VREFNXN	ADC low voltage reference to XN control switch. 0: open; 1: close.	RW
17	VREFNXP	ADC low voltage reference to XP control switch. 0: open; 1: close.	RW
16	VREFNYN	ADC low voltage reference to YN control switch. 0: open; 1: close.	RW
15	VREFPVDD33	ADC high voltage reference to VDD control switch. 0: open; 1: close.	RW
14	VREFPAUX	ADC high voltage reference to AUX control switch. 0: open; 1: close.	RW
13	VREFPXN	ADC high voltage reference to XN control switch. 0: open; 1: close.	RW
12	VREFPXP	ADC high voltage reference to XP control switch. 0: open; 1: close.	RW
11	VREFPYP	ADC high voltage reference to YP control switch. 0: open; 1: close.	RW
10	XPADC	Use XP as ADC input channel control switch. 0: open; 1: close.	RW
9	XNADC	Use XN as ADC input channel control switch. 0: open; 1: close.	RW
8	YPADC	Use YP as ADC input channel control switch. 0: open; 1: close.	RW
7	YNADC	Use YN as ADC input channel control switch. 0: open; 1: close.	RW
6	WIPEADC	Use WIPE as ADC input channel control switch. 0: open; 1: close.	RW
5	AUX2ADC	Use AUX2 as ADC input channel control switch. 0: open; 1: close.	RW
4	AUX1ADC	Use AUX1 as ADC input channel control switch. 0: open; 1: close.	RW
3	RPUWP	Connect WP to RPU control switch. 0: open; 1: close.	RW
2	RPUXP	Connect XP to RPU control switch. 0: open; 1: close.	RW
1	RPUYP	Connect YP to RPU control switch. 0: open; 1: close.	RW
0	APIL	Use inter current source control switch. 0: open; 1: close.	RW

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29.2.12 ADTEST Command Register (ADTEST)

ADC TEST Register (ADTEST) is used for test adc function.

ADCMD **0x1007002C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Test_en	Reserved																										SW_test	VREF_test	RPU_test	APIL_test	BG_test
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Test_en	Test enable. 0: disable; 1: enable.	RW
30:5	Reserved	Writing has no effect, read as zero.	R
4	SW_test	SW test. 0: disable; 1: enable test SW.	RW
3	VREF_test	VREF test. 0: disable; 1: enable test VREF.	RW
2	RPU_test	RPU test. 0: disable; 1: enable test RPU.	RW
1	APIL_test	APIL test. 0: disable; 1: enable test APIL.	RW
0	BG_test	Bandgap test. 0: disable; 1: enable test Bandgap.	RW

NOTES:

1 Please don't set ADTEST.test_en to 1 in normal use.
2 If you want to use ADTEST mode , please called Hardware and IC engineer for help.
3 In Bg_test mode, the bandgap voltage can be tested through XP_BR pin with a 32Kohm resistor between XP_BR and AGND33.
4 In APIL_test mode, the current for pressure measurement can be tested through YP_TR pin to AGND33.
5 In RPU_test mode, the output current of the WIPER_AUX is equal to "TPVDD/R_{pullup}" when connect WIPER_AUX pin to AGND33.
6 In VREF_test mode, the vref generator block can be test through XP_BR and XN_TL pins.
7 In SW_test mode, 2 transmission gates are serialized between AUX2 and AUX1 pins.

29.3 SAR A/D Controller Guide

The following describes steps of using SAR-ADC.

29.3.1 Power Down Mode

1 Then initial value of ADENA.POWER is 1, and the state of SADC is in dower down state.
2 When you want to use SADC, you should first set ADENA.POWERON to 0 to power on SADC. And you should wait for at least 2ms, then you can enable Touch Screen, VBAT and AUX.
3 When you want to power down SADC to get lower power, you should disable Touch Screen,

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VBAT and AUX, and then set ADENA.POWER to 1.

29.3.2 A Sample Touch Screen Operation

(Pen Down → Sample some data of several points → Pen Up)

1 Set ADCTRL to 0x1f to mask all the interrupt of SADC.
2 Set DMA_EN to choose whether to use DMA to read the sample data out or to use CPU to read the sample data out.
3 Set ADCFG.RPU to choose the Internal Pull-up resistor for Pen Detection.
4 Set ADCFG.WIRE_SEL to choose 4-wire or 5-wire mode in pendown detect.
5 Set ADCFG.CMD_SEL to choose use hardware inter command or software command control touch screen. If you want to use software command, you must write your command by ADCMD register. And if you want to use hardware inter command, please straight to set ADCFG.SPZZ.
6 Set ADCFG.SPZZ and ADCFG.XYZ to choose sample mode.
   a X_s→Y_s (Single-end X→Single-end Y).
   b X_d→Y_d (Differential X→Differential Y).
   c X_d→Y_d→$Z1_d$→$Z2_d$ or X_d→Y_d→$Z3_d$→$Z4_d$ (Reference register ADCFG.SPZZ)
   (Differential X→Differential Y→Differential Z1→Differential Z2 or
   Differential X→Differential Y→Differential Z3→Differential Z4).
   d X_d→Y_d→$Z1_d$→$Z2_d$→X2→Y2 or X_d→Y_d→$Z3_d$→$Z4_d$ →X2→Y2 (Reference register bit SPZZ).
7 Set ADCFG.SNUM to choose one point sampling times.
8 Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.
9 Set ADWAIT to decide the wait time of pen down and the interval time between sampling different points. This time delay is necessary because when pen is put down or pen position change, there should be some time to wait the pen down signal to become stable.
10 Set ADSAME to decide the interval time between repeated sampling the same point. User can repeat sampling one point to get the most accurate data.
11 Set ADCTRL.PENDM to 0 to enable the pen down interrupt of touch panel.
12 Set ADENA.TCHEN to 1 to start touch panel.
13 When pen down interrupt happened, you should set ADCTRL.PENDM to 1 and clear ADSTATE.PEND to close pen down interrupt. Then you should clear ADSTATE.PENDU and set ADCTRL.PENUM to 0 to enable pen up interrupt.
14 When pen down interrupt happened, the SARADC is sampling data. When ADSTATE.DTCH to 1, user must read the sample data from ADTCH. The SARADC will not sample the next point until the whole data of the one point are read (no matter by CPU or DMA). If ADCFG.XYZ is mode zero and mode one, user needs to read 1*ADCFG.SNUM times to get the whole data. In mode two, user needs to read 2*ADCFG.SNUM times to get the whole data. And in mode three, user needs to read 3*ADCFG.SNUM times to get all data.
15 Repeat 14 till pen up interrupt happened.
16 When pen up interrupt happened, you should set ADCTRL.PENUM to 1 and clear

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ADSTATE.PENU. Then you should clear ADSTATE.PEND and set ADCTRL.PENDM to 0 to enable pen down interrupt.

17 Wait pen down interrupt and repeat from 13.

18 When you want to shut down the touch screen, user can set the ADENA.TCHEN to 0. If the last point is not sampled completely, user can abandon it.

29.3.3 SLEEP mode Sample Operation

1 If the register ADCLK have not been set before, you should set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.

2 Clear ADSTATE.SLP_RDY, then you can set ADENA.SLP_MD to 1. When ADSTATE.SLP_RDY = 1, the Touch Screen is have entered the SLEEP mode.

3 After that you should clear ADSTATE.SLPEND and set ADCTRL.SLPENDM to 0 to enable “in SLEEP mode pen down interrupt” and mask all other interrupts. Then you can execute the SLEEP instruction to enter the SLEEP mode.

4 When “in SLEEP mode pen down interrupt” happened, it will switch from the SLEEP mode to NORMAL. Then you should set ADCTRL.SLPENDM to 1 and clear ADSTATE.SLPEND to close “in SLEEP mode pen down interrupt”. Clear ADSTATE.SLP_RDY, and you should set ADENA.SLP_MD to 0. When ADSTATE.SLP_RDY = 1, the Touch Screen is have exited the SLEEP mode.

5 Then you can do any other operations.

29.3.4 VBAT Sample Operation

1 Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.

2 Set ADCFG.CH_MD to choose VBAT test mode channel.

3 Set ADENA.VBATEN to 1 to enable the channel.

4 When ADSTATE.VRDY = 1, you can read the sample data from ADVDAT. And the VBATEN will be set to 0 auto.

29.3.5 AUX Sample Operation

1 Set ADCFG.CMD to choose one CMD. (AUX1 or AUX2)

2 Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.

3 Set ADENA.AUXEN to 1 to enable the channel.

4 When ADSTATE. ARDY = 1, you can read the sample data from ADADAT. And the AUXEN will be set to 0 auto.

29.3.6 Disable Touch Screen

1 When ADENA.TCHEN=1, ADENA.VBATEN=0, ADENA.AUXEN=0.

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2 Set ADENA.TCHEN to 0.
3 Read ADENA.TCHEN till it is set to 0 by hardware, then Touch Screen is fully disabled.

29.3.7 Multi-touch Operation

If you want to detect multi-touch, you should follow to steps as below.

1 Set ADENA.YYZ=11.
2 Set ADCTRL.PENDM to 0 to enable the pen down interrupt of touch panel.
3 Set ADCFG.TCHEN=1 to start touch panel.
4 When pen down interrupt happened, you should set ADCTRL.PENDM to 1 and clear ADSTATE.PEND to close pen down interrupt. Then you should clear ADSTATE.PENDU and set ADCTRL.PENUM to 0 to enable pen up interrupt.
5 When ADSTATE.DTCH to 1, you can read the sample data from ADTCH. The measured data recorded as $X2_1$, $Y2_1$, you need to compare the measurement values of $X2_1$, $Y2_1$ and calibration values of X2, Y2. If $X2_1$<X2 and $Y2_1$<Y2, now is two points touch.
6 If the next measure is two points touch, the measured data recorded as $X2_2$, $Y2_2$, you can compare the $X2_1$, $y2_1$ and $X2_2$, $Y2_2$. If $X2_2$ >$X2_1$ and $Y2_2$ > $y2_1$, the touch movement state is shrinkage; if $X2_2$ <$X2_1$ and $Y2_2$ < $Y2_1$, the touch movement state is expand.

NOTE: Before in normally measurement ,you must calibration the values of X2 and Y2. When you calibration the X2, Y2 value, you need a single point of touch the touch panel, record the measurements data. Then repeat these measurements at least three times, recording measure data is $X2_1$, $X2_2$, $X2_3$ and $Y2_1$, $Y2_2$, $Y2_3$. You can use the formula (5) ,(6) to calculate the X2, Y2 value.

$$X2 = \frac{X2_1 + X2_2 + X2_3}{3} \quad (5)$$

$$Y2 = \frac{Y2_1 + Y2_2 + Y2_3}{3} \quad (6)$$

29.3.8 Use Software Command Operation

If you want to use software write command, you should follow to steps as below.

1 Set ADCFG.CMD_SEL =1.
2 Read ADCMD register once, discard the read-in data. This reading purpose is to activate the command logic.
3 Write you command to ADCMD register.
4 Write 0x00000000 to ADCMD register, indicate the written command is end.
5 Set ADENA.TCHEN=1 to start touch panel.

NOTE: The RPU values are 6bits in SARADC, but in ADCMD register , it has 5 bits only. In fact, the lowest RPU bit circuit is given as a fixed value of 1.

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29.3.9 Use 5-wire touch panel Operation

If you want to use 5-wrie touch panel, you should complete the following set.

1 Set ADCFG.WIRE_SEL=1 to use 5-wire pendown detect.
2 Write all your commands to the command FIFO through ADCMD register.
3 Set ADENA.TCHEN=1 to start touch panel.

NOTE: In 5-wire mode, the ADCFG.SNUM will disable. The control logic will execution the control commands until the command value equals to 0x00000000.

29.3.10 Use External Touch Screen Controller Operation

If you want to use external touch screen controller, you should set ADCENA.TCHEN=0 and ADCENA.PEND=0, than you can use external touch screen controller freely.

NOTE: In this mode, all switches will open(default), but you can use VBAT or AUX sample operation by configure the appropriate register.

29.3.11 Use TSC to support keypad

SADC TSC function can apply to a keypad, if touch screen is not used. Suppose the keypad is a NxM matrix, where X direction has N key columns and Y direction has M key rows. Kij is used to indicate the key in ith column from left to right and jth row from bottom to top, where i=0~(N-1) and j=0~(M-1). Figure 29-1 is a 6x5 keypad circuit. The blue color is for X direction network and pink color is for Y. The networks are composed by resistors and metal line. These two networks should be connected to SADC 4 pins: XP/XN/YP/YN as illustrated in the figure. The gray circle is the key. When no key pressing, X network and Y network is open circuit. When a key is pressed, the X network and Y network is shorted under the key position.

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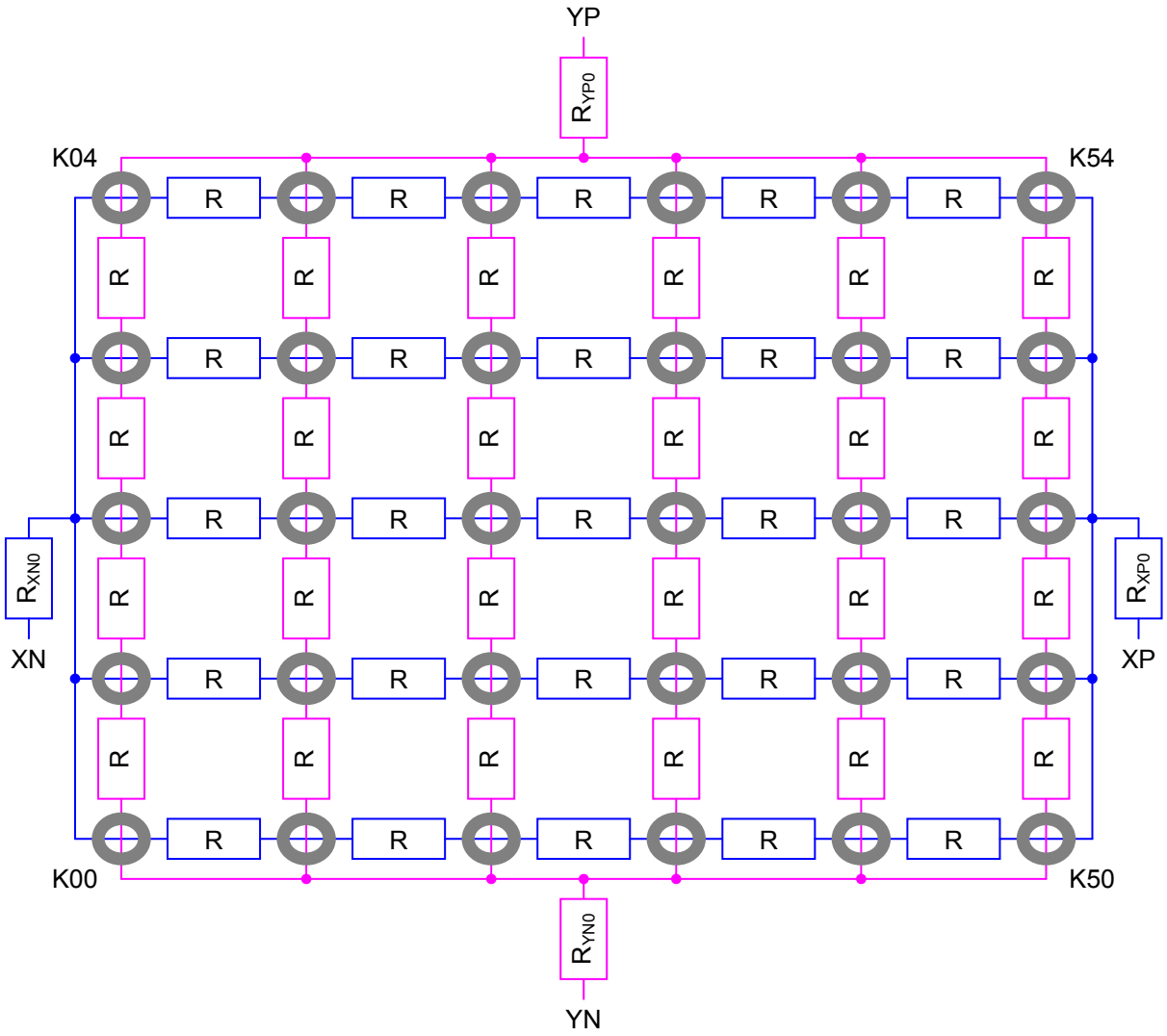


Figure 29-1 6x5 keypad circuit

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When SADC is in waiting for pen-down status (C=1100), the equivalent circuit is show in Figure 29-2. When the key is not pressed, XP is open and the PEN is pulled to VDDADC, which is logic 1. When the key Kij is pressed, the circuit is: VDDADC→(10kΩ resistor)→R_{XP}→R_{YN}→VSSADC.

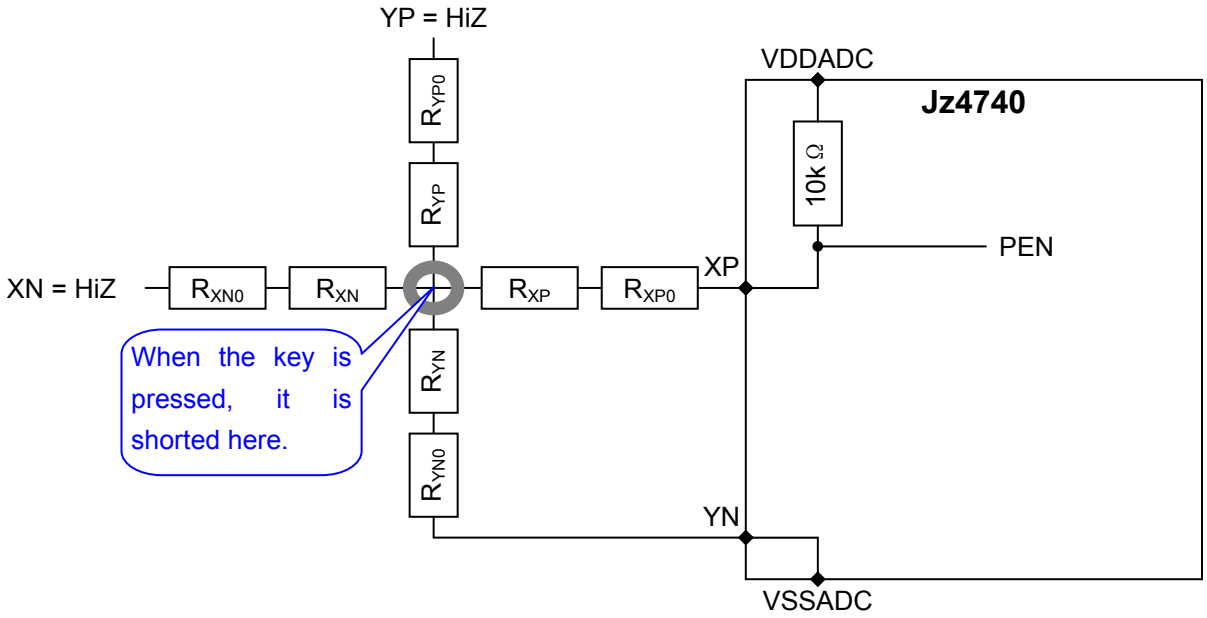


Figure 29-2 Wait for pen-down (C=1100) circuit

Where

$$R_{XP} = \frac{(N-1)^2 - i^2}{M \times (N-1-i) + 2i} \times R$$

$$R_{YN} = \frac{j \times (2M-2-j)}{N \times j + 2M - 2 - 2j} \times R$$

To ensure logic 0 at PEN in this case, following formula should be obeyed.

$$R_{XP} + R_{YN} + R_{XP0} + R_{YN0} \le 3k\Omega \quad (7)$$

It is suggested the value of N and M is as close to each other as possible. For N=2~20, M=2~20 and M=(N-1, N or N+1), we found

$$R_{XP} + R_{YN} < 2.7 \times R \quad (8)$$

After key pressing is found, the key Kij location, columns and row, should be measured by using C=0010 and C=0011 respectively. The equivalent circuits are show in Figure 29-3 and Figure 29-4, where

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$$R_{X0} = \frac{N-1}{M-1} \times R$$
$$R_{Y0} = \frac{M-1}{N-1} \times R$$
$$R_{XNi} = i \times R$$
$$R_{XPi} = (N-1-i) \times R$$
$$R_{YNj} = j \times R$$
$$R_{YPj} = (M-1-j) \times R$$

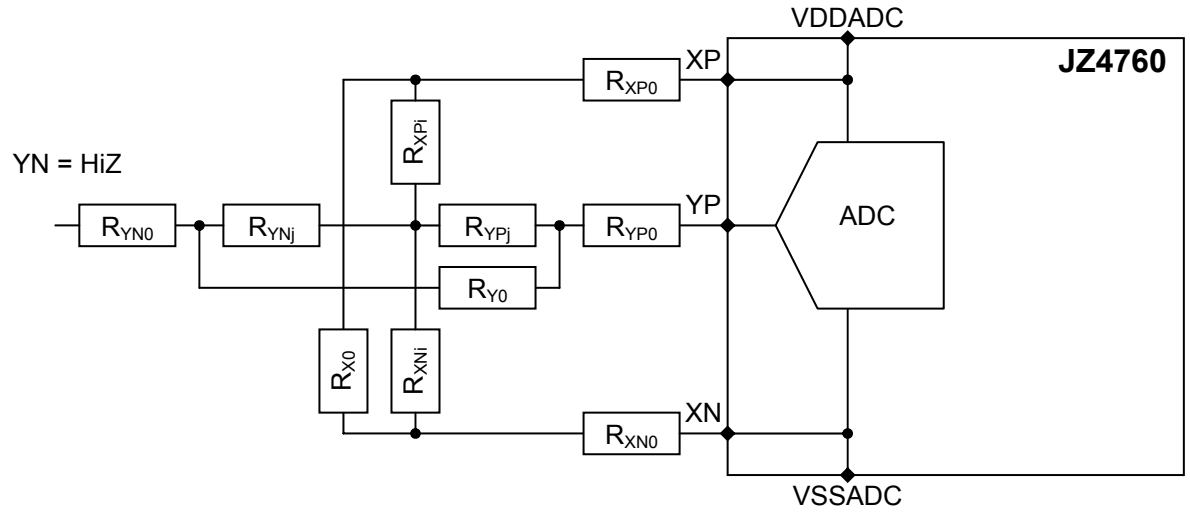


Figure 29-3 Measure X-position (C=0010) circuit

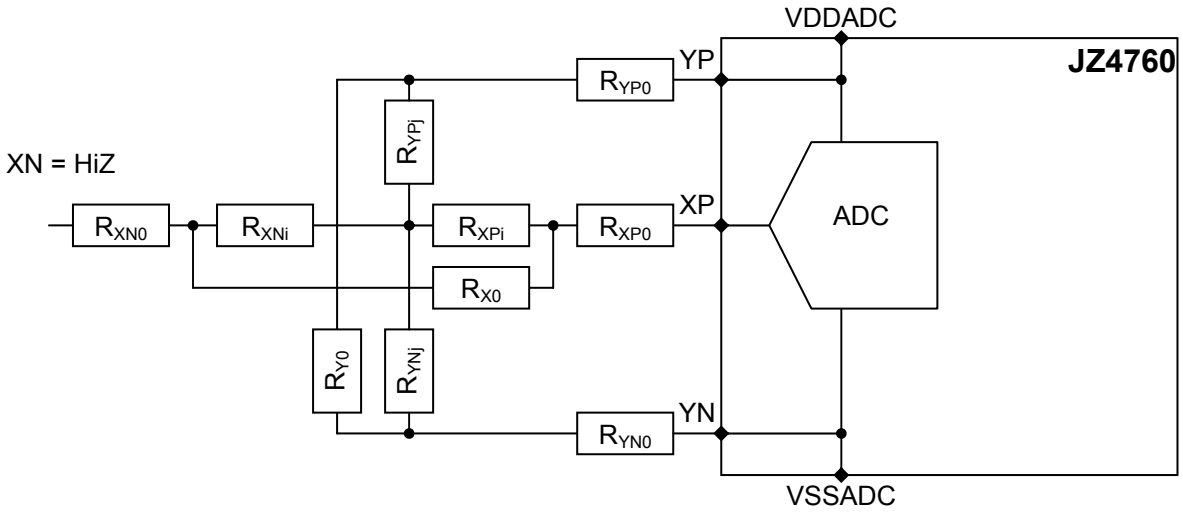


Figure 29-4 Measure Y-position (C=0011) circuit

So for Kij pressing, we should get ADC converted number Ni and Nj for i and j respectively.

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$$Ni = \frac{R_{XN0} + \frac{i}{M}R}{R_{XN0} + \frac{N-1}{M}R + R_{XP0}} \times 4096$$

$$Nj = \frac{R_{YN0} + \frac{j}{N}R}{R_{YN0} + \frac{M-1}{N}R + R_{YP0}} \times 4096$$

It is required the resistor between XP and XN in case of C=0010, between YP and YN in case of C=0011, must be ≥200Ω and it better be ≥500Ω. Also consider the requirement in formula (7) and (8) above, we suggest to put R_{XP0} = R_{XN0} = R_{YP0} = R_{YN0} = 50Ω or 100Ω, put R = 500Ω ~ 1kΩ.

To use the keypad, the software should set:

ADENA.TCHEN = 1

ADCFG.XYZ = 10

The operation is similar to touch screen.

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30 General-Purpose I/O Ports

30.1 Overview

General Purpose I/O Ports (GPIO) is used in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

Features:

- Each port can be configured as an input, an output or an alternate function port
- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
- Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
- GPIO output 6 interrupts, 1 for every group, to INTC

30.1.1 GPIO Port A Summary

Table 30-1 GPIO Port A summary

Bit N	PA N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	U	sd0(io)	-	-	-	
1	01	U	sd1(io)	-	-	-	
2	02	U	sd2(io)	-	-	-	
3	03	U	sd3(io)	-	-	-	
4	04	U	sd4(io)	-	-	-	
5	05	U	sd5(io)	-	-	-	
6	06	U	sd6(io)	-	-	-	
7	07	U	sd7(io)	-	-	-	
8	08	U	sd8(io)	-	-	-	
9	09	U	sd9(io)	-	-	-	
10	10	U	sd10(io)	-	-	-	
11	11	U	sd11(io)	-	-	-	
12	12	U	sd12(io)	-	-	-	
13	13	U	sd13(io)	-	-	-	
14	14	U	sd14(io)	-	-	-	
15	15	U	sd15(io)	-	-	-	

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16	16	U rst-pe	rd_(o)	-	-	-	
17	17	U rst-pe	we_(o)	-	-	-	
18	18	U rst-pe	fre_(o)	msc0_clk(o)	ssi0_clk(o)	-	
19	19	U rst-pe	fwe_(o)	msc0_cmd(io)	ssi0_ce0_(o)	-	
20	20	U	msc0_d0(io)	ssi0_dr(i)	-	-	1
21	21	U rst-pe	cs1_(o)	msc0_d1(io)	ssi0_dt(o)	-	
22	22	U rst-pe	cs2_(o)	msc0_d2(io)	-	-	
23	23	U rst-pe	cs3_(o)	msc0_d3(io)	-	-	
24	24	U rst-pe	cs4_(o)	-	-	-	
25	25	U rst-pe	cs5_(o)	-	-	-	
26	26	U rst-pe	cs6_(o)	rdwr_(o)	-	-	
27	27	U	wait_(i)	-	-	-	
28	28	U	dreq0(i)	-	-	-	
29	29	U	dack0(o)	owi(io)	-	-	
30	30	-	-	-	-	-	6
31	31	-	-	-	-	-	7,11

30.1.2 GPIO Port B Summary

Table 30-2 GPIO Port B summary

Bit N	PB N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	D rst-pe	sa0_cl(o)	-	-	-	8
1	01	D rst-pe	sa1_al(o)	-	-	-	9
2	02	U	sa2(o)	-	-	-	
3	03	U	sa3(o)	-	-	-	
4	04	U	sa4(o)	dreq1(i)	mii_crs(i)	-	
5	05	U	sa5(o)	dack1(o)	-	-	

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6	06	U	cim_pclk(i)	-	-	-	
7	07	U	cim_hsyn(i)	-	-	-	
8	08	U rst-pe	cim_vsyn(i)	-	-	-	
9	09	U	cim_mclk(o)	-	-	epd_pwc(o)	
10	10	D	cim_d0(i)	-	-	epd_pwr0(o)	
11	11	D	cim_d1(i)	-	-	epd_pwr1(o)	
12	12	U	cim_d2(i)	-	-	epd_sce2_(o)	
13	13	U	cim_d3(i)	-	-	epd_sce3_(o)	
14	14	U	cim_d4(i)	-	-	epd_sce4_(o)	
15	15	U	cim_d5(i)	-	-	epd_sce5_(o)	
16	16	D	cim_d6(i)	-	-	epd_pwr2(o)	
17	17	D	cim_d7(i)	-	-	epd_pwr3(o)	
18	18	D	cim_d8(i)	dmic_clk(o)	-	epd_bd0(o)	
19	19	D	cim_d9(i)	dmic_in(i)	-	epd_bd1(o)	
20	20	U	msc2_d0(io)	ssi0_dr(i)	ssi1_dr(i)	tsd0(i)	
21	21	U	msc2_d1(io)	ssi0_dt(o)	ssi1_dt(o)	tsd1(i)	
22	22	U	tsd2(i)	-	-	-	
23	23	U	tsd3(i)	-	-	-	
24	24	U	tsd4(i)	-	-	-	
25	25	U	tsd5(i)	-	-	-	
26	26	U	tsd6(i)	-	-	-	
27	27	U	tsd7(i)	-	-	-	
28	28	U	msc2_clk(o)	ssi0_clk(o)	ssi1_clk(o)	tsclk(i)	
29	29	U rst-pe	msc2_cmd(io)	ssi0_ce0_(o)	ssi1_ce0_(o)	tsstr(i)	
30	30	U	msc2_d2(io)	ssi0_gpc(o)	ssi1_gpc(o)	tsfail(i)	
31	31	U rst-pe	msc2_d3(io)	ssi0_ce1_(o)	ssi1_ce1_(o)	tsfrm(i)	

30.1.3 GPIO Port C Summary

Table 30-3 GPIO Port C summary

Bit N	PC N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	U	lcd_b0(o)	lcd_rev(o)	-	-	
1	01	U	lcd_b1(o)	lcd_ps(o)	-	-	
2	02	U	lcd_b2(o)	-	-	-	
3	03	U	lcd_b3(o)	-	-	-	
4	04	U	lcd_b4(o)	-	-	-	

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5	05	U	lcd_b5(o)	-	-	-	
6	06	U	lcd_b6(o)	-	-	-	
7	07	U	lcd_b7(o)	-	-	-	
8	08	U	lcd_pclk(o)	-	-	-	
9	09	U	lcd_de(o)	-	-	-	
10	10	U rst-pe	lcd_g0(o)	lcd_spl(o)	uart4_txd(o)	-	
11	11	U	lcd_g1(o)	-	-	-	
12	12	U	lcd_g2(o)	-	-	-	
13	13	U	lcd_g3(o)	-	-	-	
14	14	U	lcd_g4(o)	-	-	-	
15	15	U	lcd_g5(o)	-	-	-	
16	16	U	lcd_g6(o)	-	-	-	
17	17	U	lcd_g7(o)	-	-	-	
18	18	U	lcd_hsyn(io)	-	-	-	
19	19	U	lcd_vsyn(io)	-	-	-	
20	20	U	lcd_r0(o)	lcd_cls(o)	uart4_rxd(i)	-	
21	21	U	lcd_r1(o)	-	-	-	
22	22	U	lcd_r2(o)	-	-	-	
23	23	U	lcd_r3(o)	-	-	-	
24	24	U	lcd_r4(o)	-	-	-	
25	25	U	lcd_r5(o)	-	-	-	
26	26	U	lcd_r6(o)	-	-	-	
27	27	U	lcd_r7(o)	-	-	-	
28	28	U	uart2_rxd(i)	-	-	-	
29	29	U	uart2_cts_(i)	-	-	-	
30	30	U rst-pe	uart2_txd(o)	-	-	-	
31	31	U rst-pe	uart2_rts_(o)	-	-	-	

30.1.4 GPIO Port D Summary

Table 30-4 GPIO Port D summary

Bit N	PD N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	U	pcm0_do(o)	-	-	-	
1	01	U	pcm0_clk(io)	-	-	-	
2	02	U	pcm0_syn(io)	-	-	-	
3	03	U	pcm0_di(i)	-	-	-	

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4	04	U	ps2_mclk(io)	-	-	-	
5	05	U	ps2_mdata(io)	-	-	-	
6	06	U	ps2_kclk(io)	-	-	-	
7	07	U	ps2_kdata(io)	-	-	-	
8	08	U	scc_data(io)	-	-	-	
9	09	U	scc_clk(o)	clk48m(i)	-	-	
10	10	U	pwm6(io)	-	-	-	
11	11	U	pwm7(io)	-	-	-	
12	12	D	uart3_rxd(i)	bclk0(io)	-	epd_pwr4(o)	
13	13	D	lrclk0(io)	-	-	epd_pwr5(o)	
14	14	U	-	-	-	-	10
15	15	D rst-pe	exclk(o)	-	-	-	
16	16	U	-	-	-	-	
17	17	U	-	-	-	-	2,5
18	18	U	-	-	-	-	3,5
19	19	U	-	-	-	-	4,5
20	20	U	msc1_d0(io)	ssi0_dr(i)	ssi1_dr(i)	-	
21	21	U	msc1_d1(io)	ssi0_dt(o)	ssi1_dt(o)	-	
22	22	U	msc1_d2(io)	ssi0_gpc(o)	ssi1_gpc(o)	-	
23	23	U rst-pe	msc1_d3(io)	ssi0_ce1_(o)	ssi1_ce1_(o)	-	
24	24	U	msc1_clk(o)	ssi0_clk(o)	ssi1_clk(o)	-	
25	25	U rst-pe	msc1_cmd(io)	ssi0_ce0_(o)	ssi1_ce0_(o)	-	
26	26	U	uart1_rxd(i)	mii_rxd2(i)	-	-	
27	27	U	uart1_cts_(i)	mii_rxd3(i)	-	-	
28	28	U rst-pe	uart1_txd(o)	mii_txd2(o)	-	-	
29	29	U rst-pe	uart1_rts_(o)	mii_txd3(o)	-	-	
30	30	U	i2c0_sda(io)	-	-	-	
31	31	U	i2c0_sck(io)	-	-	-	

30.1.5 GPIO Port E Summary

Table 30-5 GPIO Port E summary

Bit N	PE N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	D	pwm0(io)	-	-	-	

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1	01	D	pwm1(o)	-	-	-	
2	02	U	pwm2(o)	-	-	-	
3	03	U	pwm3(io)	-	-	-	
4	04	U	pwm4(io)	-	-	-	
5	05	U rst-pe	pwm5(io)	uart3_txd(o)	sclk_rstn(o)	-	
6	06	U	aic0_sdati(i)	-	-	epd_pwr6(o)	
7	07	D	aic0_sdato(o)	-	-	epd_pwr7(o)	
8	08	U	uart3_cts_(i)	bclk0_ad(io)	-	-	
9	09	U rst-pe	uart3_rts_(o)	lrclk0_ad(io)	-	-	
10	10	D rst-pe	drvvbus(o)	-	-	-	
11	11	U	sdato1(o)	-	-	-	
12	12	U	sdato2(o)	bclk1_ad(io)	-	-	
13	13	U	sdato3(o)	lrclk1_ad(io)	-	-	
14	14	U	ssi0_dr(i)	ssi1_dr(i)	-	-	
15	15	U	ssi0_clk(o)	ssi1_clk(o)	-	-	
16	16	U rst-pe	ssi0_ce0_(o)	ssi1_ce0_(o)	-	-	
17	17	U	ssi0_dt(o)	ssi1_dt(o)	-	-	
18	18	U rst-pe	ssi0_ce1_(o)	ssi1_ce1_(o)	-	-	
19	19	U	ssi0_gpc(o)	ssi1_gpc(o)	-	-	
20	20	U	msc0_d0(io)	msc1_d0(io)	msc2_d0(io)	-	
21	21	U	msc0_d1(io)	msc1_d1(io)	msc2_d1(io)	-	
22	22	U	msc0_d2(io)	msc1_d2(io)	msc2_d2(io)	-	
23	23	U	msc0_d3(io)	msc1_d3(io)	msc2_d3(io)	-	
24	24	U	msc0_d4(io)	msc1_d4(io)	msc2_d4(io)	-	
25	25	U	msc0_d5(io)	msc1_d5(io)	msc2_d5(io)	-	
26	26	U	msc0_d6(io)	msc1_d6(io)	msc2_d6(io)	-	
27	27	U	msc0_d7(io)	msc1_d7(io)	msc2_d7(io)	-	
28	28	U	msc0_clk(o)	msc1_clk(o)	msc2_clk(o)	-	
29	29	U	msc0_cmd(io)	msc1_cmd(io)	msc2_cmd(io)	-	
30	30	U	i2c1_sda(io)	-	-	-	
31	31	U	i2c1_sck(io)	-	-	-	

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30.1.6 GPIO Port F Summary

Table 30-6 GPIO Port F summary

Bit N	PF N	Pull (U/D)	Shared Function Port Selected by				
			0	1	2	3	Note
0	00	U	uart0_rxd(i)	gps_clk(i)	-	-	
1	01	U rst-pe	uart0_cts_(i)	gps_mag(i)	-	-	
2	02	U rst-pe	uart0_rts_(o)	gps_sig(i)	-	-	
3	03	U rst-pe	uart0_txd(o)	-	-	-	
4	04	D	mii_txd0(o)	-	-	-	
5	05	D	mii_txd1(o)	-	-	-	
6	06	D	mii_txclk(i)	-	-	-	
7	07	D	mii_rxclk(i)	-	-	-	
8	08	D	mii_rxer(i)	-	-	-	
9	09	D	mii_rxdv(i)	-	-	-	
10	10	D	mii_rxd0(i)	-	-	-	
11	11	D	mii_rxd1(i)	-	-	-	
12	12	U	mii_txen(o)	pcm1_do(o)	-	-	
13	13	U	mii_mdc(o)	pcm1_clk(io)	-	-	
14	14	U	mii_mdio(io)	pcm1_syn(io)	-	-	
15	15	U	mii_col(i)	pcm1_di(i)	-	-	
16	16	D	cim_d10(i)	-	i2c2_sda(io)	epd_bd2(o)	
17	17	D	cim_d11(i)	-	i2c2_sck(io)	epd_bd3(o)	
18	18	U	sysclk(o)	-	-		
19	19	D	bclk1(io)	-	-		
20	20	D	lrclk1(io)	-	-		
21	21	U	aic1_sdati(i)	-	-		
22	22	D	aic1_sato(o)	-	-		

NOTES:

1 If NAND flash is used, this pin must be used as NAND FRB.

2 PD17: GPIO group D bit 17 is used as BOOT_SEL0 input during boot.

3 PD18: GPIO group D bit 18 is used as BOOT_SEL1 input during boot.

4 PD19: GPIO group D bit 19 is used as BOOT_SEL2 input during boot.

5 BOOT_SEL2, BOOT_SEL1, BOOT_SEL0 are used to select boot source and function during the processor boot.

6 PA30: GPIO group A bit 30 can only be used as input and interrupt, no pull-up and pull-down. It is also used to select the function between PS2 function and JTAG function of

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JTAG/UART3/PS2 Pins(TCK_UART3_RTS_PS2_MCLK, TMS_UART3_CTS_PS2_MDATA, TDI_UART3_RxD_PS2_KCLK and TDO_UART3_TxD_PS2_KDATA), which share the same set of pins.

When PA30.function1 is false, select JTAG function.

When PA30.function1 is true, select PS2 function.

7 PA31: GPIO group A bit 31. No corresponding pin exists for this GPIO.

It is only used to select the function between UART and JTAG of JTAG/UART3/PS2 Pins (TCK_UART3_RTS_PS2_MCLK,TMS_UART3_CTS_PS2_MDATA,TDI_UART3_RxD_PS2_KCLK and TDO_UART3_TxD_PS2_KDATA), which share the same set of pins, by using register PASEL [31].

When PA31.function1 is false, select JTAG function.

When PA31.function1 is true, select UART function.

8 If NAND flash is used, this pin must be used as NAND CLE.

9 If NAND flash is used, this pin must be used as NAND ALE.

10 PD14 : this pin is just used as RTCLK input, not a really GPIO pin, can not be used as GPIO input , output and interrupt.

11 The pull enable of PA31 is used to control UART and JTAG of JTAG/UART3/PS2 Pins.

30.2 Registers Description

Table 30-7 summarized all memory-mapped registers, which can be programmed to operate GPIO port and alternate function port sharing configuration.

All registers are in 32-bits width. Usually, 1 bit in the register affects a corresponding GPIO port and every GPIO port can be operated independently.

Table 30-7 GPIO Registers

Name	Description	RW	Reset Value	Address	Size
GPIO PORT A					
PAPIN	PORT A PIN Level Register	R	0x????????	0x10010000	32
PAINT	PORT A Interrupt Register	RW	0x00000000	0x10010010	32
PAINTS	PORT A Interrupt Set Register	W	0x????????	0x10010014	32
PAINTC	PORT A Interrupt Clear Register	W	0x????????	0x10010018	32
PAMSK	PORT A Interrupt Mask Register	RW	0xFFFFFFFF	0x10010020	32
PAMSKS	PORT A Interrupt Mask Set Register	W	0x????????	0x10010024	32
PAMSKC	PORT A Interrupt Mask Clear Register	W	0x????????	0x10010028	32
PAPAT1	PORT A Pattern 1 Register	RW	0xFFFFFFFF	0x10010030	32
PAPAT1S	PORT A Pattern 1 Set Register	W	0x????????	0x10010034	32
PAPAT1C	PORT A Pattern 1 Clear Register	W	0x????????	0x10010038	32
PAPAT0	PORT A Pattern 0 Register	RW	0x00000000	0x10010040	32
PAPAT0S	PORT A Pattern 0 Set Register	W	0x????????	0x10010044	32

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PAPAT0C	PORT A Pattern 0 Clear Register	W	0x????????	0x10010048	32
PAFLG	PORT A FLAG Register	R	0x00000000	0x10010050	32
PAFLGC	PORT A FLAG Clear Register	W	0x????????	0x10010058	32
PAPEN	PORT A PULL Disable Register	RW	0x00000000	0x10010070	32
PAPENS	PORT A PULL Disable Set Register	W	0x????????	0x10010074	32
PAPENC	PORT A PULL Disable Clear Register	W	0x????????	0x10010078	32
PADRVL	-	RW	0x00000000	0x10010080	32
PADRVLS	-	W	0x????????	0x10010084	32
PADRVLC	-	W	0x????????	0x10010088	32
PADIR	-	RW	0x00000000	0x10010090	32
PADIRS	-	W	0x????????	0x10010094	32
PADIRC	-	W	0x????????	0x10010098	32
PADRVH	-	RW	0x00000000	0x100100A0	32
PADRVHS	-	W	0x????????	0x100100A4	32
PADRVHC	-	W	0x????????	0x100100A8	32
GPIO PORT B					
PBPIN	PORT B PIN Level Register	R	0x????????	0x10010100	32
PBINT	PORT B Interrupt Register	RW	0x00000000	0x10010110	32
PBINTS	PORT B Interrupt Set Register	W	0x????????	0x10010114	32
PBINTC	PORT B Interrupt Clear Register	W	0x????????	0x10010118	32
PBMSK	PORT B Interrupt Mask Register	R	0xFFFFFFFF	0x10010120	32
PBMSKS	PORT B Interrupt Mask Set Register	W	0x????????	0x10010124	32
PBMSKC	PORT B Interrupt Mask Clear Register	W	0x????????	0x10010128	32
PBPAT1	PORT B Pattern 1 Register	R	0xFFFFFFFF	0x10010130	32
PBPAT1S	PORT B Pattern 1 Set Register	W	0x????????	0x10010134	32
PBPAT1C	PORT B Pattern 1 Clear Register	W	0x????????	0x10010138	32
PBPAT0	PORT B Pattern 0 Register	RW	0x00000000	0x10010140	32
PBPAT0S	PORT B Pattern 0 Set Register	W	0x????????	0x10010144	32
PBPAT0C	PORT B Pattern 0 Clear Register	W	0x????????	0x10010148	32
PBFLG	PORT B FLAG Register	R	0x00000000	0x10010150	32
PBFLGC	PORT B FLAG Clear Register	W	0x????????	0x10010158	32
PBPEN	PORT B PULL Disable Register	RW	0x00000000	0x10010170	32
PBPENS	PORT B PULL Disable Set Register	W	0x????????	0x10010174	32
PBPENC	PORT B PULL Disable Clear Register	W	0x????????	0x10010178	32
PBDRVL	-	RW	0x00000000	0x10010180	32
PBDRVLS	-	W	0x????????	0x10010184	32
PBDRVLC	-	W	0x????????	0x10010188	32
PBDIR	-	RW	0x00000000	0x10010190	32
PBDIRS	-	W	0x????????	0x10010194	32
PBDIRC	-	W	0x????????	0x10010198	32

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PBDRVH	-	RW	0x00000000	0x100101A0	32
PBDRVHS	-	W	0x????????	0x100101A4	32
PBDRVHC	-	W	0x????????	0x100101A8	32
GPIO PORT C					
PCPIN	PORT C PIN Level Register	R	0x????????	0x10010200	32
PCINT	PORT C Interrupt Register	RW	0x00000000	0x10010210	32
PCINTS	PORT C Interrupt Set Register	W	0x????????	0x10010214	32
PCINTC	PORT C Interrupt Clear Register	W	0x????????	0x10010218	32
PCMSK	PORT C Interrupt Mask Register	R	0xFFFFFFFF	0x10010220	32
PCMSKS	PORT C Interrupt Mask Set Register	W	0x????????	0x10010224	32
PCMSKC	PORT C Interrupt Mask Clear Register	W	0x????????	0x10010228	32
PCPAT1	PORT C Pattern 1 Register	R	0xFFFFFFFF	0x10010230	32
PCPAT1S	PORT C Pattern 1 Set Register	W	0x????????	0x10010234	32
PCPAT1C	PORT C Pattern 1 Clear Register	W	0x????????	0x10010238	32
PCPAT0	PORT C Pattern 0 Register	RW	0x00000000	0x10010240	32
PCPAT0S	PORT C Pattern 0 Set Register	W	0x????????	0x10010244	32
PCPAT0C	PORT C Pattern 0 Clear Register	W	0x????????	0x10010248	32
PCFLG	PORT C FLAG Register	R	0x00000000	0x10010250	32
PCFLGC	PORT C FLAG Clear Register	W	0x????????	0x10010258	32
PCPEN	PORT C PULL Disable Register	RW	0x00000000	0x10010270	32
PCPENS	PORT C PULL Disable Set Register	W	0x????????	0x10010274	32
PCPENC	PORT C PULL Disable Clear Register	W	0x????????	0x10010278	32
PCDRVL	-	RW	0x00000000	0x10010280	32
PCDRVLS	-	W	0x????????	0x10010284	32
PCDRVLC	-	W	0x????????	0x10010288	32
PCDIR	-	RW	0x00000000	0x10010290	32
PCDIRS	-	W	0x????????	0x10010294	32
PCDIRC	-	W	0x????????	0x10010298	32
PCDRVH	-	RW	0x00000000	0x100102A0	32
PCDRVHS	-	W	0x????????	0x100102A4	32
PCDRVHC	-	W	0x????????	0x100102A8	32
GPIO PORT D					
PDPIN	PORT D PIN Level Register	R	0x????????	0x10010300	32
PDINT	PORT D Interrupt Register	RW	0x00000000	0x10010310	32
PDINTS	PORT D Interrupt Set Register	W	0x????????	0x10010314	32
PDINTC	PORT D Interrupt Clear Register	W	0x????????	0x10010318	32
PDMSK	PORT D Interrupt Mask Register	R	0xFFFFFFFF	0x10010320	32
PDMSKS	PORT D Interrupt Mask Set Register	W	0x????????	0x10010324	32
PDMSKC	PORT D Interrupt Mask Clear Register	W	0x????????	0x10010328	32
PDPAT1	PORT D Pattern 1 Register	R	0xFFFFFFFF	0x10010330	32
PDPAT1S	PORT D Pattern 1 Set Register	W	0x????????	0x10010334	32

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PDPAT1C	PORT D Pattern 1 Clear Register	W	0x????????	0x10010338	32
PDPAT0	PORT D Pattern 0 Register	RW	0x00000000	0x10010340	32
PDPAT0S	PORT D Pattern 0 Set Register	W	0x????????	0x10010344	32
PDPAT0C	PORT D Pattern 0 Clear Register	W	0x????????	0x10010348	32
PDFLG	PORT D FLAG Register	R	0x00000000	0x10010350	32
PDFLGC	PORT D FLAG Clear Register	W	0x????????	0x10010358	32
PDPEN	PORT D PULL Disable Register	RW	0x00000000	0x10010370	32
PDPENS	PORT D PULL Disable Set Register	W	0x????????	0x10010374	32
PDPENC	PORT D PULL Disable Clear Register	W	0x????????	0x10010378	32
PDDRVL	-	RW	0x00000000	0x10010380	32
PDDRVLS	-	W	0x????????	0x10010384	32
PDDRVLC	-	W	0x????????	0x10010388	32
PDDIR	-	RW	0x00000000	0x10010390	32
PDDIRS	-	W	0x????????	0x10010394	32
PDDIRC	-	W	0x????????	0x10010398	32
PDDRVH	-	RW	0x00000000	0x100103A0	32
PDDRVHS	-	W	0x????????	0x100103A4	32
PDDRVHC	-	W	0x????????	0x100103A8	32
GPIO PORT E					
PEPIN	PORT E PIN Level Register	R	0x????????	0x10010400	32
PEINT	PORT E Interrupt Register	RW	0x00000000	0x10010410	32
PEINTS	PORT E Interrupt Set Register	W	0x????????	0x10010414	32
PEINTC	PORT E Interrupt Clear Register	W	0x????????	0x10010418	32
PEMSK	PORT E Interrupt Mask Register	R	0xFFFFFFFF	0x10010420	32
PEMSKS	PORT E Interrupt Mask Set Register	W	0x????????	0x10010424	32
PEMSKC	PORT E Interrupt Mask Clear Register	W	0x????????	0x10010428	32
PEPAT1	PORT E Pattern 1 Register	R	0xFFFFFFFF	0x10010430	32
PEPAT1S	PORT E Pattern 1 Set Register	W	0x????????	0x10010434	32
PEPAT1C	PORT E Pattern 1 Clear Register	W	0x????????	0x10010438	32
PEPAT0	PORT E Pattern 0 Register	RW	0x00000000	0x10010440	32
PEPAT0S	PORT E Pattern 0 Set Register	W	0x????????	0x10010444	32
PEPAT0C	PORT E Pattern 0 Clear Register	W	0x????????	0x10010448	32
PEFLG	PORT E FLAG Register	R	0x00000000	0x10010450	32
PEFLGC	PORT E FLAG Clear Register	W	0x????????	0x10010458	32
PEPEN	PORT E PULL Disable Register	RW	0x00000000	0x10010470	32
PEPENS	PORT E PULL Disable Set Register	W	0x????????	0x10010474	32
PEPENC	PORT E PULL Disable Clear Register	W	0x????????	0x10010478	32
PEDRVL	-	RW	0x00000000	0x10010480	32
PEDRVLS	-	W	0x????????	0x10010484	32
PEDRVLC	-	W	0x????????	0x10010488	32
PEDIR	-	RW	0x00000000	0x10010490	32

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PEDIRS	-	W	0x????????	0x10010494	32
PEDIRC	-	W	0x????????	0x10010498	32
PEDRVH	-	RW	0x00000000	0x100104A0	32
PEDRVHS	-	W	0x????????	0x100104A4	32
PEDRVHC	-	W	0x????????	0x100104A8	32
GPIO PORT F					
PFPIN	PORT F PIN Level Register	R	0x????????	0x10010500	32
PFINT	PORT F Interrupt Register	RW	0x00000000	0x10010510	32
PFINTS	PORT F Interrupt Set Register	W	0x????????	0x10010514	32
PFINTC	PORT F Interrupt Clear Register	W	0x????????	0x10010518	32
PFMSK	PORT F Interrupt Mask Register	R	0xFFFFFFFF	0x10010520	32
PFMSKS	PORT F Interrupt Mask Set Register	W	0x????????	0x10010524	32
PFMSKC	PORT F Interrupt Mask Clear Register	W	0x????????	0x10010528	32
PFPAT1	PORT F Pattern 1 Register	R	0xFFFFFFFF	0x10010530	32
PFPAT1S	PORT F Pattern 1 Set Register	W	0x????????	0x10010534	32
PFPAT1C	PORT F Pattern 1 Clear Register	W	0x????????	0x10010538	32
PFPAT0	PORT F Pattern 0 Register	RW	0x00000000	0x10010540	32
PFPAT0S	PORT F Pattern 0 Set Register	W	0x????????	0x10010544	32
PFPAT0C	PORT F Pattern 0 Clear Register	W	0x????????	0x10010548	32
PFFLG	PORT F FLAG Register	R	0x00000000	0x10010550	32
PFFLGC	PORT F FLAG Clear Register	W	0x????????	0x10010558	32
PFPEN	PORT F PULL Disable Register	RW	0x00000000	0x10010570	32
PFPENS	PORT F PULL Disable Set Register	W	0x????????	0x10010574	32
PFPENC	PORT F PULL Disable Clear Register	W	0x????????	0x10010578	32
PFDRVL	-	RW	0x00000000	0x10010580	32
PFDRVLS	-	W	0x????????	0x10010584	32
PFDRVLC	-	W	0x????????	0x10010588	32
PFDIR	-	RW	0x00000000	0x10010590	32
PFDIRS	-	W	0x????????	0x10010594	32
PFDIRC	-	W	0x????????	0x10010598	32
PFDRVH	-	RW	0x00000000	0x100105A0	32
PFDRVHS	-	W	0x????????	0x100105A4	32
PFDRVHC	-	W	0x????????	0x100105A8	32

NOTE: PX**** in the description of register as follows means PA****, PB****, PC****, PD****, PE**** and PF****.

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30.2.1 PORT PIN Level Registers (PxPIN)

PAPIN, PBPIN, PCPIN, PDPIN, PEPIN and PFPIN are six 32-bit PORT PIN level registers. They are read-only registers.

PAPIN, PBPIN, PCPIN, PDPIN, PEPIN, PFPIN — **0x10010000, 0x10010100, 0x10010200, 0x10010300, 0x10010400, 0x10010500**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	PINL n	Where n = 0 ~ 31 and PINL n = PINL0 ~ PINL31. The PORT PIN level can be read by reading PINL n bit in register PXPIN.	R

30.2.2 PORT Interrupt Registers (PxINT)

PAINT, PBINT, PCINT, PDINT, PEINT and PFINT are six 32-bit interrupt registers.

PAINT, PBINT, PCINT, PDINT, PEINT, PFINT — **0x10010010, 0x10010110, 0x10010210, 0x10010310, 0x10010410, 0x10010510**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10	INT09	INT08	INT07	INT06	INT05	INT04	INT03	INT02	INT01	INT00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
N	INT n	Where n = 0 ~ 31 and INT n = INT31 ~ INT00. Interrupt enable. 0: Corresponding pin is used as device functions or normal gpio 1: Corresponding pin is used as interrupt	RW

30.2.3 PORT Interrupt Set Registers (PxINTS)

PAINTS, PBINTS, PCINTS, PDINTS, PEINTS and PFINTS are six 32-bit interrupt set registers.

PAINTS, PBINTS, PCINTS, PDINTS, PEINTS, PFINTS — **0x10010014, 0x10010114, 0x10010214, 0x10010314, 0x10010414, 0x10010514**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	R/W
N	INTS n	Writing 1 to INTS n will set INT n to 1 in register PXINT. Writing 0 to INTS n will no use.	W

30.2.4 PORT Interrupt Clear Registers (PxINTC)

PAINTC, PBINTC, PCINTC, PDINTC, PEINTC and PFINTC are six 32-bit interrupt clear registers.

PAINTC, PBINTC, PCINTC, **0x10010018, 0x10010118, 0x10010218,**
PDINTC, PEINTC, PFINTC **0x10010318, 0x10010418, 0x10010518**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	INTC n	Writing 1 to INTC n will set INT n to 0 in register PXINT. Writing 0 to INTC n will no use.	W

30.2.5 PORT Mask Registers (PxMSK)

PAMSK, PBMSK, PCMSK, PDMSK, PEMSK and PFMSK are six 32-bit PORT MASK registers.

PAMSK, PBMSK, PCMSK, **0x10010020, 0x10010120, 0x10010220,**
PDMSK. PEMSK, PFMSK **0x10010320, 0x10010420, 0x10010520**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24	MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16	MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK09	MSK08	MSK07	MSK06	MSK05	MSK04	MSK03	MSK02	MSK01	MSK00
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
n	MSK n	Where n = 0 ~ 31 and MSK n = MSK31 ~ MSK0. When PXINT n = 1: 0: Enable the pin as an interrupt source 1: Disable the pin as an interrupt source When PXINT n = 0: 0: Corresponding pin will be used as device function 1: Corresponding pin will be used as gpio	RW

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30.2.6 PORT Mask Set Registers (PxMSKS)

PAMSKS, PBMSKS, PCMSKS, PDMSKS, PEMSKS and PFMSKS are six 32-bit PORT MASK set registers.

PAMSKS, PBMSKS, PCMSKS, PDMSKS, PEMSKS, PFMSKS — **0x10010024, 0x10010124, 0x10010224, 0x10010324, 0x10010424, 0x10010524**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	MSKS n	Writing 1 to MSKS n will set MSK n to 1 in register PXMSK. Writing 0 to MSKS n will no use.	W

30.2.7 PORT Mask Clear Registers (PxMSKC)

PAMSKC, PBMSKC, PCMSKC, PDMSKC, PEMSKC and PFMSKC are six 32-bit PORT MASK clear registers.

PAMSKS, PBMSKC, PCMSKC, PDMSKC, PEMSKC, PFMSKC — **0x10010028, 0x10010128, 0x10010228, 0x10010328, 0x10010428, 0x10010528**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	MSKC n	Writing 1 to MSKC n will set MSK n to 0 in register PXMSK. Writing 0 to MSKC n will no use.	W

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30.2.8 PORT PAT1/Direction Registers (PxPAT1)

PAPAT1, PBPAT1, PCPAT1, PDPAT1, PEPAT1 and PFPAT1 are six 32-bit PORT pattern1/direction registers.

PAPAT1, PBPAT1, PCPAT1, PDPAT1, PEPAT1, PFPAT1 — **0x10010030, 0x10010130, 0x10010230, 0x10010330, 0x10010430, 0x10010530**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT131	PAT130	PAT129	PAT128	PAT127	PAT126	PAT125	PAT124	PAT123	PAT122	PAT121	PAT120	PAT119	PAT118	PAT117	PAT116	PAT115	PAT114	PAT113	PAT112	PAT111	PAT110	PAT109	PAT108	PAT107	PAT106	PAT105	PAT104	PAT103	PAT102	PAT101	PAT100
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
n	PAT1 n	Where n = 0 ~ 31 and PAT1 n = PAT131 ~ PAT10. When PINT n = 1 (Interrupt function): 0: Level trigger interrupt 1: Edge trigger interrupt When PINT n = 0 and PMSK = 0 (Device function): 0: Corresponding pin is used as device 0 or device 1 function 1: Corresponding pin is used as device 2 or device 3 function When PINT n = 0 and PMSK = 0 (GPIO function): 0: Corresponding pin is used as gpio output 1: Corresponding pin is used as gpio input	RW

30.2.9 PORT PAT1/Direction Set Registers (PxPAT1S)

PAPAT1S, PBPAT1S, PCPAT1S, PDPAT1S, PEPAT1S and PFPAT1S are six 32-bit PORT pattern1/direction set registers.

PAPAT1S, PBPAT1S, PCPAT1S, PDPAT1S, PEPAT1S, PFPAT1S — **0x10010034, 0x10010134, 0x10010234, 0x10010334, 0x10010434, 0x10010534**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PAT1S n	Writing 1 to PAT1S n will set PAT1 n to 1 in register PXPAT1. Writing 0 to PAT1S n will no use.	W

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30.2.10 PORT PAT1/Direction Clear Registers (PxPAT1C)

PAPAT1C, PBPAT1C, PCPAT1C, PPAT1C, PEPAT1C and PFPAT1C are six 32-bit PORT pattern1 or direction clear registers.

PAPAT1S, PBPAT1C, PCPAT1C, **0x10010038, 0x10010138, 0x10010238,**
PDPAT1C, PEPAT1C, PFPAT1C **0x10010338, 0x10010438, 0x10010538**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PAT1C n	Writing 1 to PAT1C n will set PAT1 n to 0 in register PXPAT1. Writing 0 to PAT1C n will no use.	W

30.2.11 PORT PAT0/Data Registers (PxPAT0)

PAPAT0, PBPAT0, PCPAT0, PDPAT0, PEPAT0 and PFPAT0 are six 32-bit PORT Pattern 0 or DATA registers.

PAPAT0, PBPAT0, PCPAT0, **0x10010040, 0x10010140, 0x10010240,**
PDPAT0, PEPAT0, PFPAT0 **0x10010340, 0x10010440, 0x10010540**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT031	PAT030	PAT029	PAT028	PAT027	PAT026	PAT025	PAT024	PAT023	PAT022	PAT021	PAT020	PAT019	PAT018	PAT017	PAT016	PAT015	PAT014	PAT013	PAT012	PAT011	PAT010	PAT009	PAT008	PAT007	PAT006	PAT005	PAT004	PAT003	PAT002	PAT001	PAT000
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
N	PAT0 n	Where n = 0 ~ 31 and PAT0 n = PAT00 ~ PAT031. When PINTn = 1 and PPAT1 = 0: 0: Port is low level triggered interrupt input 1: Port is low high triggered interrupt input When PINTn = 1 and PPAT1 = 1: 0: Port is falling edge triggered interrupt input 1: Port is rising edge triggered interrupt input When PINTn = 0 and PMSK = 0 and PPAT1 = 0: 0: Port is pin of device 0 1: Port is pin of device 1 When PINTn = 0 and PMSK = 0 and PPAT1 = 1: 0: Port is pin of device 2	RW

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		1: Port is pin of device 3 When PINTn = 0 and PMSK = 1 and PPAT1 = 0: 0: Port is GPIO output 0 1: Port is GPIO output 1	

30.2.12 PORT PAT0/Data Set Registers (PxPAT0S)

PAPAT0S, PBPAT0S, PCPAT0S, PDPAT0S, PEPAT0S and PFPAT0S are six 32-bit PORT Pattern0 or DATA set registers.

PAPAT0S, PBPAT0S, PCPAT0S, PDPAT0S, PEPAT0S, PFPAT0S — **0x10010044, 0x10010144, 0x10010244, 0x10010344, 0x10010444, 0x10010544**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PAT0S n	Writing 1 to PAT0S n will set PAT0 n to 1 in register PXPAT0. Writing 0 to PAT0S n will no use.	W

30.2.13 PORT PAT0/Data Clear Registers (PxPAT0C)

PAPAT0C, PBPAT0C, PCPAT0C, PDPAT0C, PEPAT0C and PFPAT0C are six 32-bit PORT Pattern 0 or DATA clear registers.

PAPAT0C, PBPAT0C, PCPAT0C, PDPAT0C, PEPAT0C, PFPAT0C — **0x10010048, 0x10010148, 0x10010248, 0x10010348, 0x10010448, 0x10010548**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PAT0C n	Writing 1 to PAT0C n will set PAT0 n to 0 in register PXPAT0. Writing 0 to PAT0C n will no use.	W

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30.2.14 PORT FLAG Registers (PxFLG)

PAFLG, PBFLG, PCFLG, PDFLG, PEFLG and PFFLG are six 32-bit GPIO FLAG registers. They are read-only registers.

PAFLG, PBFLG, PCFLG, PDFLG, PEFLG, PFFLG — **0x10010050, 0x10010150, 0x10010250, 0x10010350, 0x10010450, 0x10010550**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31. FLAG n is interrupt flag bit for checking the interrupt whether to happen. When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PXFLG will be set to 1.	R

30.2.15 PORT FLAG Clear Registers (PxFLGC)

PAFLGC, PBFLGC, PCFLGC, PDFLGC, PEFLGC and PFFLGC are six 32-bit GPIO FLAG Clear registers. They are read-only registers.

PAFLGC, PBFLGC, PCFLGC, PDFLGC, PEFLGC, PFFLGC — **0x10010058, 0x10010158, 0x10010258, 0x10010358, 0x10010458,0x10010558**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	FLAGC n	When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PXFLG will be cleared.	R

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30.2.16 PORT PULL Disable Registers (PxPE)

PAPE, PBPE, PCPE, PDPE, PEPE and PFPE are six 32-bit PORT PULL disable registers.

PAPE, PBPE, PCPE, PDPE, PEPE, PFPE — **0x10010070, 0x10010170, 0x10010270, 0x10010370, 0x10010470, 0x10010570**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULL31	PULL30	PULL29	PULL28	PULL27	PULL26	PULL25	PULL24	PULL23	PULL22	PULL21	PULL20	PULL19	PULL18	PULL17	PULL16	PULL15	PULL14	PULL13	PULL12	PULL11	PULL10	PULL09	PULL08	PULL07	PULL06	PULL05	PULL04	PULL03	PULL02	PULL01	PULL00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
N	PULL n	Where n = 0 ~ 31 and PULL n = PULL0 ~ PULL31. PULL n is used for setting the port to be PULL UP or PULL DOWN enable. 0: An internal pull up or pull down resistor connects to the port. Up or down is pin dependence 1: No pull up or pull down resistor connects to the port	RW

30.2.17 PORT PULL Set Registers (PxPES)

PAPES, PBPES, PCPES, PDPES, PEPES and PFPES are six 32-bit PORT PULL set registers. They are write-only registers.

PAPES, PBPES, PCPES, PDPES, PEPES, PFPES — **0x10010074, 0x10010174, 0x10010274, 0x10010374, 0x10010474, 0x10010574**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULLS31	PULLS30	PULLS29	PULLS28	PULLS27	PULLS26	PULLS25	PULLS24	PULLS23	PULLS22	PULLS21	PULLS20	PULLS19	PULLS18	PULLS17	PULLS16	PULLS15	PULLS14	PULLS13	PULLS12	PULLS11	PULLS10	PULLS09	PULLS08	PULLS07	PULLS06	PULLS05	PULLS04	PULLS03	PULLS02	PULLS01	PULLS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PULLS n	Writing 1 to PULLS n will set PULL n to 1 in register PXPE. Writing 0 to PULLS n will no use.	W

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30.2.18 PORT PULL Clear Registers (PxPEC)

PAPEC, PBPEC, PCPEC, PDPEC, PEPEC and PFPEC are six 32-bit PORT PULL clear registers.

PAPES, PBPEC, PCPEC, PDPEC, PEPEC, PFPEC — **0x10010078, 0x10010178, 0x10010278, 0x10010378, 0x10010478, 0x10010578**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULLC31	PULLC30	PULLC29	PULLC28	PULLC27	PULLC26	PULLC25	PULLC24	PULLC23	PULLC22	PULLC21	PULLC20	PULLC19	PULLC18	PULLC17	PULLC16	PULLC15	PULLC14	PULLC13	PULLC12	PULLC11	PULLC10	PULLC09	PULLC08	PULLC07	PULLC06	PULLC05	PULLC04	PULLC03	PULLC02	PULLC01	PULLC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PULLC n	Writing 1 to PULLC n will set PULL n to 0 in register PXPE. Writing 0 to PULLC n will no use.	W

30.3 Program Guide

30.3.1 Port Function Guide

INT	MASK	PAT1	PAT0	Port Description
1	0	0	0	Port is low level triggered interrupt input.
1	0	0	1	Port is high level triggered interrupt input.
1	0	1	0	Port is fall edge triggered interrupt input.
1	0	1	1	Port is rise edge triggered interrupt input.
1	1	0	0	Port is low level triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	0	1	Port is high level triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	0	Port is fall edge triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	1	Port is rise edge triggered interrupt input. Interrupt is masked. Flag is recorded.
0	0	0	0	Port is pin of device 0.
0	0	0	1	Port is pin of device 1.
0	0	1	0	Port is pin of device 2.
0	0	1	1	Port is pin of device 3.
0	1	0	0	Port is GPIO output 0.
0	1	0	1	Port is GPIO output 1.
0	1	1	?	Port is GPIO input.

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31 I2C Controller

31.1 Overview

The I2C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is the device that initializes/terminates a data transfer on the bus and generates clock signals to permit that transfer. During that time, any addressed device is considered as a slave. The I2C controller is software controlled. It behaves as a master or a slave. However, operating as a master and slave simultaneously is not supported.

31.1.1 Features

- Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Two speeds
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
- Device clock is identical with pclk
- Programmable SCL generator
- Master or slave I2C operation
- 7-bit addressing/10-bit addressing
- 16-level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 3 independent I2C channels (I2C0, I2C1, I2C2)

31.1.2 Pin Description

Table 31-1 I2C Pin Description

Name	Width	IO	Description
SDA	1-bit	IO	I2C serial data
SCL	1-bit	IO	I2C serial clock

Please note that dedicate pull-up resistors must be introduced on board-level. The low-to-high (rise time) transition is highly dependent on RC time constant of the bus.

Totally speaking, for standard-mode I2C-bus system, the pull up resistor depends on following

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parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices

For fast-mode I2C-bus system, switched pull-up circuit may be essential for strict speed and load requirement. (Refer to ' Philips Semiconductor, *THE I²C-BUS SPECIFICATION*, Version 2.1. Jan, 2000')

31.2 Registers

31.2.1 Registers Memory Map

A read operation to an address location that contains unused bits results in a 0 value being returned on each of the unused bits.

Registers in I2C controller can be accessed by indicating 24-bit Address Base combined with 8-bit Address Offset.

Table 31-2 Registers Memory Map-Address Base

Name	Addr Base	Description
I2C0	0x10050000	Address base of I2C0
I2C1	0x10051000	Address base of I2C1
I2C2	0x10055000	Address base of I2C2

Table 31-3 Registers Memory Map-Address Offset

Name	Addr Offset	Description	Width	RW	Reset
I2CCON	0x00	I2C control	8bits	RW	0x6D
I2CTAR	0x04	I2C target address	13bits	RW	0x0855
I2CSAR	0x08	I2C slave address	10bits	RW	0x055
I2CDC	0x10	I2C data buffer and command	9bits	RW	0x000
I2CSHCNT	0x14	Standard speed I2C SCL high count	16bits	RW	0x0190
I2CSLCNT	0x18	Standard speed I2C SCL low count	16bits	RW	0x01D6
I2CFHCNT	0x1C	Fast speed I2C SCL high count	16bits	RW	0x003C
I2CFLCNT	0x20	Fast speed I2C SCL low count	16bits	RW	0x0082
I2CINTST	0x2C	I2C Interrupt Status	12bits	R	0x000
I2CINTM	0x30	I2C Interrupt Mask	12bits	R/W	12'h8FF
I2CRXTL	0x38	I2C RxFIFO Threshold	4 bits	RW	0xF
I2CTXTL	0x3C	I2C TxFIFO Threshold	4 bits	RW	0xF
I2CCINT	0x40	Clear Interrupts	1 bit	R	0x0

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I2CCRXUF	0x44	Clear RXUF Interrupt	1 bit	R	0x0
I2CCRXOF	0x48	Clear RX_OVER Interrupt	1 bit	R	0x0
I2CCTXOF	0x4C	Clear TX_OVER Interrupt	1 bit	R	0x0
I2CCRXREQ	0x50	Clear RDREQ Interrupt	1 bit	R	0x0
I2CCTXABT	0x54	Clear TX_ABRT Interrupt	1 bit	R	0x0
I2CCRXDN	0x58	Clear RX_DONE Interrupt	1 bit	R	0x0
I2CCACT	0x5c	Clear ACTIVITY Interrupt	1 bit	R	0x0
I2CCSTP	0x60	Clear STOP Interrupt	1 bit	R	0x0
I2CCSTT	0x64	Clear START Interrupt	1 bit	R	0x0
I2CCGC	0x68	Clear GEN_CALL Interrupt	1 bit	R	0x0
I2CENB	0x6C	I2C Enable	1 bit	RW	0x0
I2CST	0x70	I2C Status register	7 bits	R	0x06
I2CABTSRC	0x80	I2C Transmit Abort Status Register	16 bits	R	0x0000
I2CDMACR	0x88	DMA Control Register	2 bits	R/W	0x0
I2CDMATDLR	0x8c	DMA Transmit Data Level	4 bits	R/W	0x0
I2CDMARDLR	0x90	DMA Receive Data Level	4 bits	R/W	0x0
I2CSDASU	0x94	I2C SDA Setup Register	8 bits	RW	0x64
I2CACKGC	0x98	I2C ACK General Call Register	1 bit	RW	0x1
I2CENBST	0x9C	I2C Enable Status Register	3 bits	R	0x0

31.2.2 Registers and Fields Description

31.2.2.1 I2CCON

I2C control register. Only STPHLD can be written during I2C disable and enable, others only can be written when I2C is disable.

I2CCON **BASE + 0x00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								STPHLD	SLVDIS	REST	MATP	SATP	SPD		MD
RST	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1

Bits	Name	Description	RW
15:8	Reserved	Writing has no effect, read as zero.	R

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7	STPHLD	Stop Hold Enable bit. 0: When tx fifo is empty, a STP condition will be generated 1: STP will never be generated until this bit changed to 0 Only this bit in I2CCON can be written during I2C disable and enable status.	RW
6	SLVDIS	This bit controls whether I2C has its slave disabled after reset. 0: slave is enabled 1: slave is disabled	RW
5	REST	Determines whether RESTART conditions may be sent when acting as a master. 0: disable 1: enable	RW
4	MATP	This bit controls whether the I2C starts its transfers in 7-bit or 10-bit addressing mode when acting as a master. The function of this bit is handled by bit 12 of I2CTAR register. 0: 7-bit addressing 1: 10-bit addressing	R
3	SATP	When acting as a slave, this bit controls whether the I2C responds to 7-bit or 10-bit addresses. 0: 7-bit addressing 1: 10-bit addressing	RW
2:1	SPD	These bits control at which speed the I2C operates. 1: standard mode (100 kbps) 2: fast mode (400 kbps) **NOTE:** when these two bits are set to 2'b00 or 2'b11, the speed mode will be automatically set to 2'b10 i.e. fast mode.	RW
0	MD	This bit controls whether the I2C master is enabled. 0: master disabled 1: master enabled	RW

31.2.2.2 I2CTAR

I2CTAR **BASE + 0x04**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			MATP	SPECIAL	GC_OR_START	I2CTAR									
RST	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	1

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Bits	Name	Description	R/W
15:13	Reserved	Writing has no effect, read as zero.	R
12	MATP	This bit controls whether the I2C starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing; 1: 10-bit addressing. **NOTE:** this bit is initially set to 0.	RW
11	SPECIAL	This bit indicates whether software performs a General Call or START BYTE command. 0: ignore the bit of GC_OR_START and use I2CTAR normally 1: perform special I2C command as specified in GC_OR_START bit **NOTE:** this bit is initially set to 1.	RW
10	GC_OR_START	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the I2CINTST register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared 1: START BYTE	RW
9:0	I2CTAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the I2CTAR and I2CSAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself, but only to a slave.	RW

NOTE: It is not necessary to perform any write to this register if I2C is enabled as an I2C slave only.

31.2.2.3 I2CSAR

I2CSAR **BASE + 0x08**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						I2CSAR									
RST	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	I2CSAR	The I2CSAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only I2CSAR[6:0] is used. This register can be written only when the I2C interface is disabled. Writes at other times have no effect.	RW

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NOTE: It is not necessary to perform any write to this register if I2C is enabled as an I2C master only.

31.2.2.4 I2CDC

I2C Rx/Tx Data Buffer and Command Register, which the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO.

I2CDC **BASE + 0x10**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							CMD	DAT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:9	Reserved	Writing has no effect, read as zero.	R
8	CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C acts as a slave. It controls only the direction when it acts as a master. 1: Read 0: Write	RW
7:0	DAT	This register contains the data to be transmitted or received on the I2C bus.	RW

NOTE: this command only transfer 8-bit data combined with 1-bit CMD, extra bits on the bus will be eliminated. i.e. only 8-0 bits on the bus are accepted by I2C controller.

31.2.2.5 I2CSHCNT

I2CSHCNT **BASE + 0x14**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2CSHCNT															
RST	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	I2CSHCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. The register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled. Writes at other times have no effect. SCL high time of i2c is (I2CSHCNT + 8) i2c_clk periods.	RW

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NOTE: Minimum value allowed for the I2CSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.

31.2.2.6 I2CSLCNT

I2CSLCNT **BASE + 0x18**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2CSLCNT															
RST	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
15:0	I2CSLCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled. Writes at other times have no effect. SCL low time of i2c is (I2CSLCNT + 1) i2c_clk periods.	RW

NOTE: Minimum value that can be programmed in the I2CSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8.

31.2.2.7 I2CFHCNT

I2CFHCNT **BASE + 0x1C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2CFHCNT															
RST	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Name	Description	R/W
15:0	I2CFHCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. This register can be written only when the I2C interface is disabled. Writes at other times have no effect.	RW

NOTE: Minimum value allowed for the I2CSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.

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31.2.2.8 I2CFLCNT

I2CFLCNT BASE + 0x20

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2CFLCNT															
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Name	Description	R/W
15:0	I2CFLCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. This register can be written only when the I2C interface is disabled. Writes at other times have no effect.	RW

NOTE: Minimum value that can be programmed in the I2CSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8.

31.2.2.9 I2CINTST

Each bit in this register has a corresponding mask bit in the I2CINTM register. These bits are cleared by reading the matching interrupt clear register.

I2CINTST BASE + 0x2C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	IGC	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling I2C or when the CPU reads bit 0 of the I2CCGC register. I2C stores the received data in the Rx buffer.	R
10	ISTT	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
9	ISTP	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
8	IACT	This bit captures I2C activity and stays set until it is cleared. There are	R

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		four ways to clear it: 1 Disabling the I2C 2 Reading the I2CCACT register 3 Reading the I2CCINT register 4 System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the I2C module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	
7	RXDN	When the I2C is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TXABT	This bit indicates if I2C, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a “transmit abort”. When this bit is set to 1, the I2CABTSRC register indicates the reason why the transmit abort takes places. **NOTE:** The I2C flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2CCTXABT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	R
5	RDREQ	This bit is set to 1 when I2C is acting as a slave and another I2C master is attempting to read data from I2C. The I2C holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2CDC register. This bit is set to 0 just after the processor reads the I2CCRREQregister.	R
4	TXEMP	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TXTL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the I2CENB bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with I2CENB = 0, this bit is set to 0.	R
3	TXOF	Set during transmit if the transmit buffer is filled to I2CTX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the I2CDC register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when i2c_en goes to 0, this interrupt is cleared.	R
2	RXFL	Set when the receive buffer reaches or goes above the I2C_RXTL threshold in the I2C_RXTL register. It is automatically cleared by hardware when buffer level goes below the threshold.	R

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		It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2CENB[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2CENB bit 0 is programmed with a 0, regardless of the activity that continues.	
1	RXOF	Set if the receive buffer is completely filled to 2 and an additional byte is received from an external I2C device. The I2C acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2CENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when i2c_en goes to 0, this interrupt is cleared.	R
0	RXUF	Set if the processor attempts to read the receive buffer when it is empty by reading from the I2CDC register. If the module is disabled (I2CENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when i2c_en goes to 0, this interrupt is cleared.	R

31.2.2.10 I2CINTM

These bits mask their corresponding interrupt status bits. They are active low; a value of 0 prevents a bit from generating an interrupt.

I2CINTM **BASE + 0x30**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				MIGC	MISTT	MISTP	MIACT	MRXDN	MTXABT	MRDREQ	MTXEMP	MTXOF	MRXFL	MRXOF	MRXUF
RST	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	MIGC	These bits mask their corresponding interrupt status bits in the I2CINTST register.	RW
10	MISTT		RW
9	MISTP		RW
8	MIACT		RW
7	MRXDN		RW
6	MTXABT		RW
5	MRDREQ		RW
4	MTXEMP		RW
3	MTXOF		RW
2	MRXFL		RW

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1	MRXOF		RW
0	MRXUF		RW

31.2.2.11 I2CRXTL

I2CRXTL BASE + 0x38

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												RXTL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
3:0	RXTL	Receive FIFO Threshold Level. Controls the level of entries that triggers the RxFIFO full interrupt. A value of n sets the threshold for (n+1) entries.	RW

31.2.2.12 I2CTXTL

I2CTXTL BASE + 0x3C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TXTL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
3:0	TXTL	Transmit FIFO Threshold Level. Controls the level of entries that trigger the TxFIFO empty interrupt. A value of n sets the threshold for n entries.	RW

31.2.2.13 I2CCINT

I2CCINT BASE + 0x40

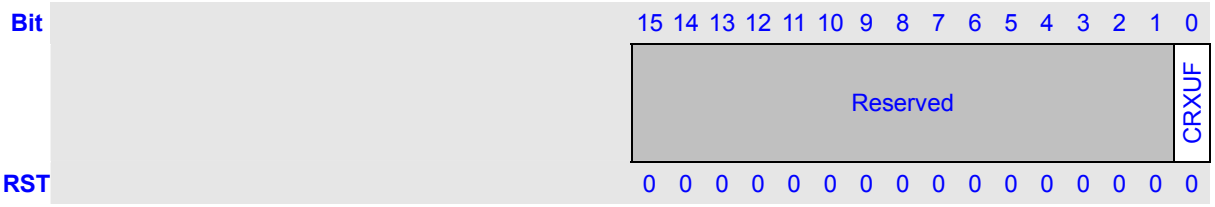
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CINT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CINT	Read this register to clear the combined interrupt, all individual interrupts, and the I2CABTSRC register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I2CABTSRC register for an exception to clearing I2CABTSRC.	R

31.2.2.14 I2CCRXUF

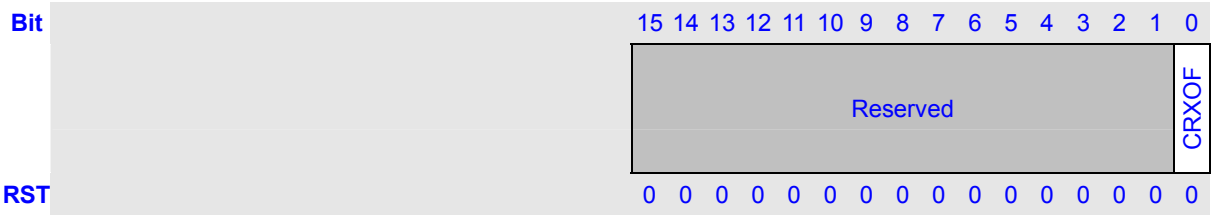
I2CCRXUF BASE + 0x44



Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXUF	Read this register to clear the RXUF interrupt (bit 0) of the I2CINTST register.	R

31.2.2.15 I2CCRXOF

I2CCRXOF BASE + 0x48

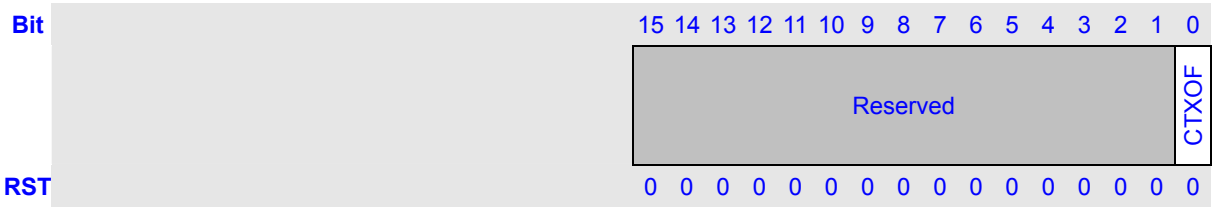


Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXOF	Read this register to clear the RXOF interrupt (bit 1) of the I2CINTST register.	R

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31.2.2.16 I2CCTXOF

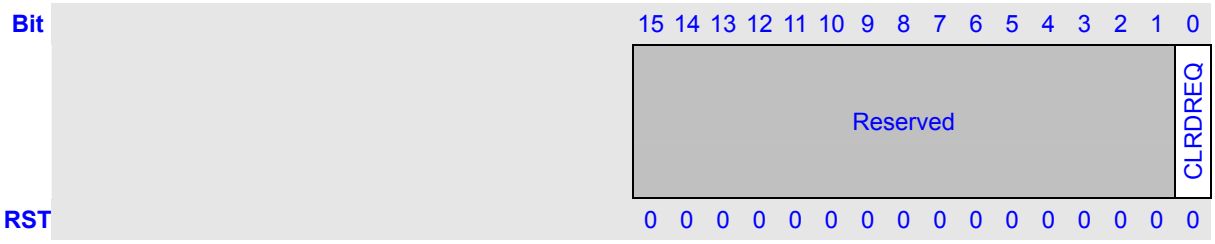
I2CCTXOF BASE + 0x4C



Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CTXOF	Read this register to clear the TX_OVER interrupt (bit 3) of the I2CINTST register.	R

31.2.2.17 I2CCRXREQ

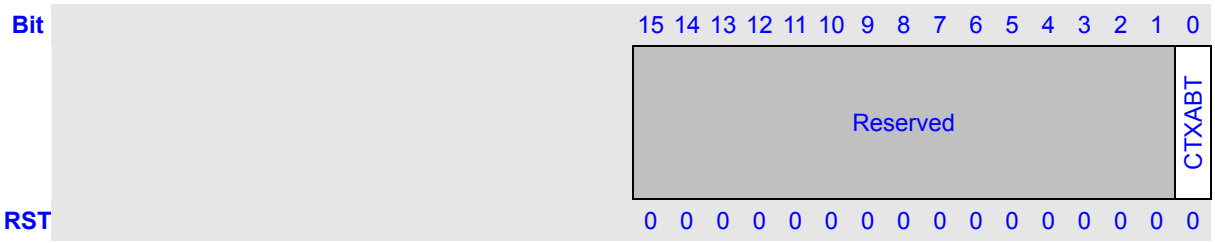
I2CCRXREQ BASE + 0x50



Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CLRDREQ	Read this register to clear the RDREQ interrupt (bit 5) of the I2CINTST register.	R

31.2.2.18 I2CCTXABT

I2CCTXABT BASE + 0x54



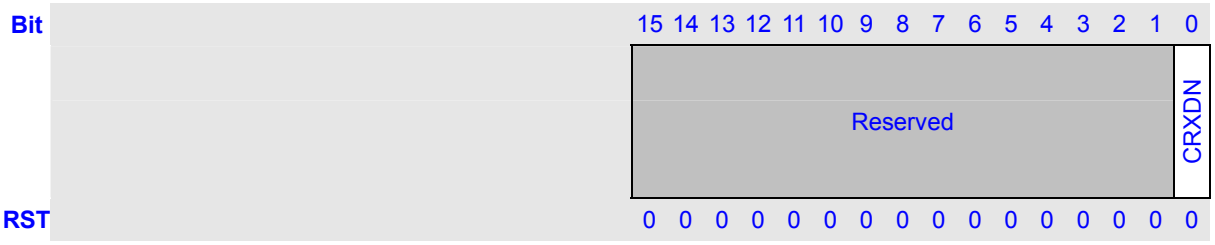
Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R

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0	CTXABT	Read this register to clear the TX_ABRT interrupt (bit 6) of the I2CINTST register, and the I2CABTSRC register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I2CABTSRC register for an exception to clearing I2CABTSRC.	R

31.2.2.19 I2CCRXDN

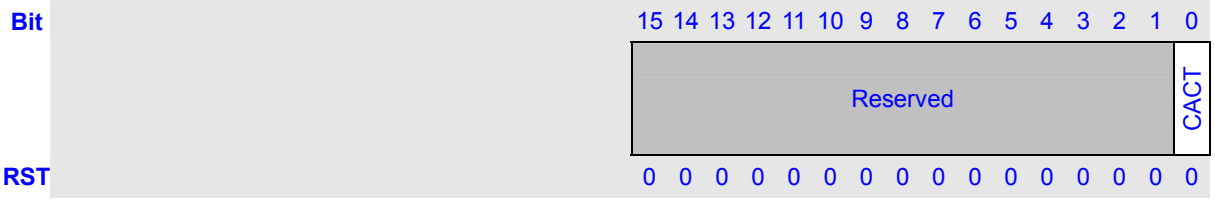
I2CCRXDN BASE + 0x58



Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXDN	Read this register to clear the RX_DONE interrupt (bit 7) of the I2CINTST register.	R

31.2.2.20 I2CCACT

I2CCACT BASE + 0x5C



Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CACT	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the I2CINTST register.	R

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31.2.2.21 I2CCSTP

I2CCSTP BASE + 0x60

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CSTP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTP	Read this register to clear the STOP interrupt (bit 9) of the I2CINTST register.	R

31.2.2.22 I2CCSTT

I2CCSTT BASE + 0x64

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CSTT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTT	Read this register to clear the START interrupt (bit 10) of the I2CINTST register.	R

31.2.2.23 I2CCGC

I2CCGC BASE + 0x68

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CGC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CGC	Read this register to clear the GEN_CALL interrupt (bit 11) of I2CINTST register.	R

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31.2.2.24 I2CENB

I2CENB BASE + 0x6C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															I2CENB
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	I2CENB	Controls whether the I2C is enabled. 0: Disables I2C (TX and RX FIFOs are held in an erased state) 1: Enables I2C Software can disable I2C while it is active. However, it is important that care be taken to ensure that I2C is disabled properly. When I2C is disabled, the following occurs: – The TX FIFO and RX FIFO get flushed. – Status bits in the I2CINTST register are still active until I2C goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the I2C stops the current transfer at the end of the current byte and does not acknowledge the transfer.	R

31.2.2.25 I2CST

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the I2C is disabled by writing 0 in bit 0 of the I2CENB register:

– Bits 1 and 2 are set to 1

– Bits 3 and 4 are set to 0

When the master or slave state machine goes to idle and ic_en=0:

– Bits 5 and 6 are set to 0

I2CST BASE + 0x70

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									SLVACT	MSTACT	RFF	RFNE	TFE	TFNF	ACT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

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Bits	Name	Description	R/W
15:7	Reserved	Writing has no effect, read as zero.	R
6	SLVACT	Slave FSM Activity Status. 0: Slave FSM is in IDLE state 1: Slave FSM is not in IDLE state	R
5	MSTACT	Master FSM Activity Status. 0: Master FSM is in IDLE state 1: Master FSM is not in IDLE state	R
4	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full	R
3	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty	R
2	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	R
1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full	R
0	ACT	I2C Activity Status. The OR of SLVACT and MSTACT bits.	R

31.2.2.26 I2CABTSRC

This register has 16 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the I2CCTXABT register or the I2CCINT register is read. To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; RESTART must be enabled (I2CCON[5]=1), the SPECIAL bit must be cleared (I2CTAR[11]), or the GC_OR_START bit must be cleared (I2CTAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

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I2CABTSRC **BASE + 0x80**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLVRD_INTX	SLV_ARBLOST	SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	SBYTE_NORSTRT	ABRT_HS_NORSTRT	SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_N	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15	SLVRD_INTX	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of I2CDC register.	R
14	SLV_ARBLOST	1: Slave lost the bus while transmitting data to a remote master. I2CABTSRC[12] is set at the same time. **NOTE:** Even though the slave never “owns” the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then I2C no longer own the bus. Reset value: 0x0.	R
13	SLVFLUSH_TXFIFO	1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Reset value: 0x0.	R
12	ARB_LOST	1: Master has lost arbitration, or if I2CABTSRC[14] is also set, then the slave transmitter has lost arbitration. **NOTE:** I2C can be both master and slave at the same time. Reset value: 0x0.	R
11	ABRT_MASTER_DIS	1: User tries to initiate a Master operation with the Master mode disabled. Reset value: 0x0.	R
10	ABRT_10B_RD_NORSTRT	1: The restart is disabled (I2CRESTART_EN bit (I2CCON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Reset value: 0x0.	R
9	SBYTE_NORSTRT	To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; restart must be enabled (I2CCON[5]=1), the SPECIAL bit must be cleared (I2CTAR[11]), or the GC_OR_START bit must be	R

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		cleared (I2CTAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (I2CRESTART_EN bit (I2CCON[5]) = 0) and the user is trying to send a START Byte. Reset value: 0x0.	
8	ABRT_HS_NORSTRT	1: The restart is disabled (I2CRESTART_EN bit (I2CCON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Reset value: 0x0.	R
7	SBYTE_ACKDET	1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Reset value: 0x0.	R
6	ABRT_HS_ACKDET	1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Reset value: 0x0.	R
5	ABRT_GCALL_READ	1: I2C in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (I2CDC[9] is set to 1). Reset value: 0x0.	R
4	ABRT_GCALL_NOACK	1: I2C in master mode sent a General Call and no slave on the bus acknowledged the General Call. Reset value: 0x0.	R
3	ABRT_TXDATA_NOACK	1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledgement from the remote slave(s). Reset value: 0x0.	R
2	ABRT_10ADDR2_NOACK	1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Reset value: 0x0.	R
1	ABRT_10ADDR1_NOACK	1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0.	R
0	ABRT_7B_ADDR_NOACK	1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Reset value: 0x0.	R

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31.2.2.27 I2CDMACR

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of i2c enable.

I2CDMACR BASE + 0x88

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TDEN	RDEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:2	Reserved	Writing has no effect, read as zero.	R
1	TDEN	**Transmit DMA Enable**. This bit enables/disables the transmit DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled	R/W
0	RDEN	**Receive DMA Enable**. This bit enables/disables the receive DMA channel. 0: Receive DMA disabled 1: Receive DMA enabled	R/W

31.2.2.28 I2CDMATDLR

The register is used to config dma transmit data level.

I2CDMACR BASE + 0x8c

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TDLR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	TDLR	**DMA Transmit Data Level**. This bit field controls the level at which a DMA request is made by the transmit logic. The dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value.	R/W

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31.2.2.29 I2CDMARDLR

The register is used to config dma receive data level.

I2CDMACR																BASE + 0x90
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											RDLR				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	RDLR	**DMA Receive Data Level**. This bit field controls the level at which a DMA request is made by the receive logic. The dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1.	R/W

31.2.2.30 I2CSDASU

This register controls the amount of time delay (in terms of number of i2c_clk clock periods) introduced in the rising edge of SCL, relative to SDA changing, when I2C services a read request in a slave-transmitter operation. The relevant I2C requirement is tSU:DAT (NOTE 2) as detailed in the I2C Bus Specification.

NOTE: The length of setup time is calculated using [(I2CSDASU - 1) * (ic_clk_period)], so if the user requires 10 ic_clk periods of setup time, they should program a value of 11.

A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max}$ + $t_{SU;DAT}$ = 1000 +250 =1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. (Refer to ' Philips Semiconductor, *THE I²C-BUS SPECIFICATION*, Version 2.1. Jan, 2000')

I2CSDASU																BASE + 0x94
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									SDASU						
RST	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	R/W
15:8	Reserved	Writing has no effect, read as zero.	R

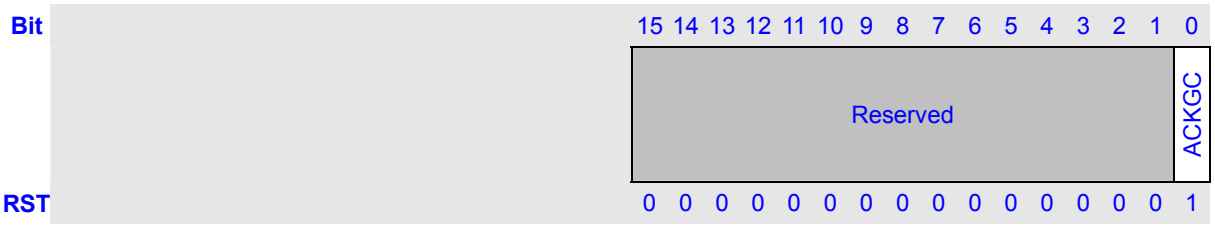
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7:0	SDASU	SDA Setup. It is recommended that if the required delay is 1000ns, then for an i2c_clk frequency of 10 MHz, I2CSDASU should be programmed to a value of 11.	R/W

31.2.2.31 I2CACKGC

The register controls whether I2C responds with an ACK or NACK when it receives an I2C General Call address.

I2CACKGC **BASE + 0x98**



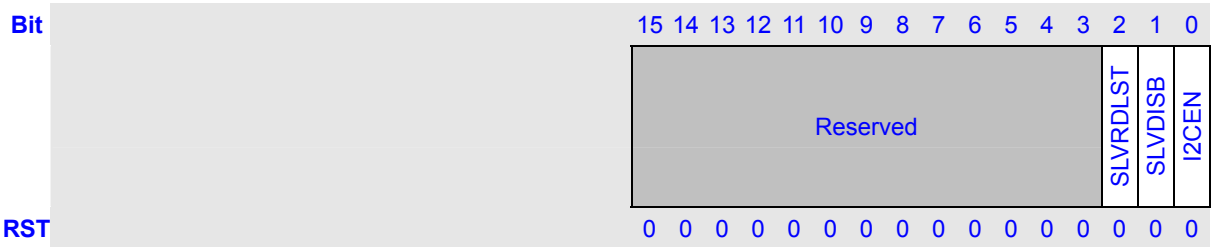
Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	ACKGC	ACK General Call. When set to 1, I2C responds with an ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the I2C does not generate General Call interrupts.	R/W

31.2.2.32 I2CENBST

The register is used to report the I2C hardware status when the I2CENB register is set from 1 to 0; that is, when I2C is disabled.

If I2CENB has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
If I2CENB has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.

I2CENBST **BASE + 0x9C**



Bits	Name	Description	R/W
15:3	Reserved	Writing has no effect, read as zero.	R
2	SLVRDLST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from	R

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		an I2C transfer due to the setting of I2CENB from 1 to 0. When read as 1, I2C is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. **NOTE:** If the remote I2C master terminates the transfer with a STOP condition before the I2C has a chance to NACK a transfer, and I2CENB has been set to 0, then this bit is also set to 1. When read as 0, I2C is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. **NOTE:** The CPU can safely read this bit when IC_EN (bit 0) is read as 0. Reset value: 0x0.	
1	SLVDISB	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the I2CENB register from 1 to 0. This bit is set when the CPU writes a 0 to the I2CENB register while: (a) I2C is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, I2C is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C (I2CSAR register) OR if the transfer is completed before I2CENB is set to 0 but has not taken effect. **NOTES:** 1 If the remote I2C master terminates the transfer with a STOP condition before the I2C has a chance to NACK a transfer, and I2CENB has been set to 0, then this bit will also be set to 1. When read as 0, I2C is deemed to have been disabled when there is master activity, or when the I2C bus is idle. 2 The CPU can safely read this bit when IC_EN (bit 0) is read as 0. Reset value: 0x0.	R
0	I2CEN	ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, I2C is deemed to be in an enabled state. When read as 0, I2C is deemed completely inactive. **NOTE:** The CPU can safely read this bit anytime. When this bit is read as 0, the CPU can safely read SLVRDLST (bit 2) and SLVDISB (bit 1). Reset value: 0x0.	R

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31.3 Operating Flow

This section provides information on the following topics:

- "Slave Mode Operation"
- "Master Mode Operation"
- "Disabling I2C"

NOTE: It is important to note that the I2C should only be set to operate as an I2C Master, or I2C Slave, but not both simultaneously. This is achieved by ensuring that bit 6 (I2CSLAVE_DISABLE) and 0 (I2CMASTER_MODE) of the I2CCON register are never set to 0 and 1, respectively.

31.3.1 I2C Behavior

The I2C can be controlled via software to be either:

- An I2C master only, communicating with other I2C slaves.

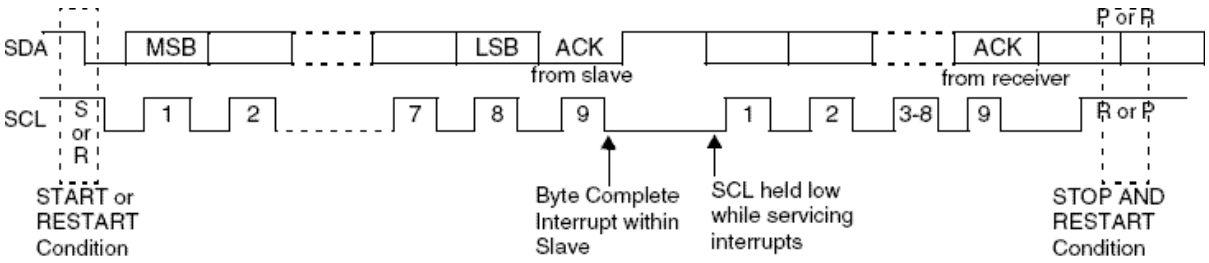
OR

- An I2C slave only, communicating with one more I2C masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The device that is receiving data, which can be either a master or a slave, sends the acknowledgement of data. As mentioned previously, the I2C protocol also allows multiple masters to reside on the I2C bus and uses an arbitration procedure to determine bus ownership.

Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledgement (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition.



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31.3.2 Master Mode Operation

This section includes the following topics:

- "Initial Configuration"
- "Dynamic I2CTAR or I2C10BITADDR_MASTER Update"
- "Master Transmit and Master Receive"

31.3.2.1 Configuration

To use the I2C as a master perform the following steps:

1 Disable the I2C by writing 0 to the I2CENB register. And wait for the I2CENBST.I2CEN = 0.

2 Write to the I2CCON register to set the speed mode supported (bits 2:1). Please note that the MATP (bit4) is NOT writable. The addressing mode is controlled by Register I2CTAR.

3 Set the expected SCL frequency. I2CCON.SPD = 2'b01, only I2CSHCNT and I2CSLCNT are needed to be configured; I2CCON.SPD = 2'b10, only I2CFHCNT and I2CFLCNT are needed to be configured.

Supposed:

T_{scl} : I2C SCL period

T_{i2c_clk} : I2C device clock period

$T_{min\_scl\_l}$: Protocol minimum SCL low time

$T_{min\_scl\_h}$: Protocol minimum SCL high time

Then can get the equation:

$T_{scl} = T_{i2c\_clk} * ((I2C*HCNT + 8) + (I2C*LCNT + 1))$

And the following conditions should be met:

$(I2C*HCNT + 8) * T_{i2c\_clk} >= T_{min\_scl\_h}$

$(I2C*LCNT + 1) * T_{i2c\_clk} >= T_{min\_scl\_l}$

I2C*HCNT >= 6

I2C*LCNT >= 8

4 Write to the I2CTAR register the address of the I2C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I2C. The addressing mode that master starts, either 7-bit or 10-bit addressing, is controlled by the I2C10BITADDR_MASTER bit field (bit 12).

5 Enable the I2C by writing a 1 into I2CENB register. And wait for the I2CENBST.I2CEN = 1.

6 Now write the transfer direction and data to be sent to the I2CDC register (This can be done by DMA). If the I2CDC register is written before the I2C is enabled, the data and commands are lost as the buffers are kept cleared when I2C is not enabled.

NOTE: For multiple I2C transfers, perform additional writes to the TX FIFO such that the TX FIFO does not become empty during the I2C transaction. If the TX FIFO is completely emptied at any stage and I2CCON.STPHLD is 0, then further writes to the TX FIFO results in an independent I2C transaction.

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31.3.2.2 Dynamic I2CTAR or I2C10BITADDR_MASTER Update

The I2C supports dynamic updating of the I2CTAR (bits 9:0) and I2C10BITADDR_MASTER (bit 12) bit fields of the I2CTAR register. You can dynamically write to the I2CTAR register provided the following conditions are met:

1 I2C is not enabled (I2CENB=0);

OR

2 I2C is enabled (I2CENB=1);
AND
I2C is NOT engaged in any Master (tx, rx) operation (I2CST[5]=0);
AND
I2C is enabled to operate in Master mode (I2CCON[0]=1);
AND
there are NO entries in the TX FIFO (I2CST[2]=0).

31.3.2.3 Master Transmit and Master Receive

The I2C supports switching back and forth between reading and writing dynamically. To transmit data, write the data to be transferred to lower byte of the I2C Rx/Tx Data Buffer and Command Register (I2CDC). The *CMD* bit (I2CDC[8]) should be written to 0 for I2C write operations.

Subsequently, a read command may be issued by writing “don’t cares” to the lower byte of the I2CDC register, and a 1 should be written to the *CMD* bit.

31.3.3 Slave Mode Operation

This section includes the following procedures:

- “Initial Configuration”
- “Slave-Transmitter Operation for a Single Byte”
- “Slave-Receiver Operation for a Single Byte”
- “Slave-Transfer Operation For Bulk Transfers”

31.3.3.1 Initial Configuration

To use the I2C as a slave, perform the following steps:

1 Disable the I2C by writing a ‘0’ to bit 0 of the I2CENB register.
2 Write to the I2CSAR register (bits 9:0) to set the slave address. This is the address to which the I2C responds.
3 Write to the I2CCON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the I2C in slave-only mode by writing a ‘0’ into bit 6 (I2CSLAVE_DISABLE) and a ‘0’ to bit 0 (MASTER_MODE).

NOTE: Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing

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and a master with 10-bit addressing, and vice versa.

4 Enable the I2C by writing a '1' in bit 0 of the I2CENB register.

NOTE: Depending on the reset values chosen, steps 2 and 3 may not be necessary because the reset values can be configured. For instance, if the device is only going to be a master, there would be no need to set the slave address because you can configure I2C to have the slave disabled after reset and to enable the master after reset. The values stored are static and do not need to be reprogrammed if the I2C is disabled.

31.3.3.2 Slave-Transmitter Operation for a Single Byte

When another I2C master device on the bus addresses the I2C and requests data, the I2C acts as a slave-transmitter and the following steps occur:

1 The other I2C master device initiates an I2C transfer with an address that matches the slave address in the I2CSAR register of the I2C.
2 The I2C acknowledges the sent address and recognizes the direction of the transfer to indicate that it is acting as a slave-transmitter.
3 The I2C asserts the RDREQ interrupt (bit 5 of the I2CINTST register) and holds the SCL line low. It is in a wait state until software responds.
If the RDREQ interrupt has been masked, due to I2CINTM[5] register (MRDREQ bit field) being set to 0, then it is recommended that a hardware and/or software timing routine be used to instruct the CPU to perform periodic reads of the I2CINTST register.
   a Reads that indicate I2CINTST[5] (RDREQ bit field) being set to 1 must be treated as the equivalent of the RDREQ interrupt being asserted.
   b Software must then act to satisfy the I2C transfer.
   c The timing interval used should be in the order of 10 times the fastest SCL clock period the I2C can handle. For example, for 400 kb/s, the timing interval is 25us.

NOTE: The value of 10 is recommended here because this is approximately the amount of time required for a single byte of data transferred on the I2C bus.

4 If there is any data remaining in the TX FIFO before receiving the read request, then the I2C asserts a TX_ABRT interrupt (bit 6 of the I2CINTST register) to flush the old data from the TX FIFO.

NOTE: Because the I2C's TX FIFO is forced into a flushed/reset state whenever a TX_ABRT event occurs, it is necessary for software to release the I2C from this state by reading the I2CCTXABT register before attempting to write into the TX FIFO. See register I2CINTST for more details. If the TX_ABRT interrupt has been masked, due to of I2CINTM[6] register (MTX_ABRT bit field) being set to 0, then it is recommended that re-using the timing routine (described in the previous step), or a similar one, be used to

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read the I2CINTST register.

a Reads that indicate bit 6 (TXABT) being set to 1 must be treated as the equivalent of the TX_ABRT interrupt being asserted.
b There is no further action required from software.
c The timing interval used should be similar to that described in the previous step for the I2CINTST[5] register.

5 Software writes to the I2CDC register with the data to be written (by writing a '0' in bit 8).
6 Software must clear the RDREQ and TX_ABRT interrupts (bits 5 and 6, respectively) of the I2CINTST register before proceeding.
If the RDREQ and/or TX_ABRT interrupts have been masked, then clearing of the I2CINTST register will have already been performed when either the RDREQ or TXABT bit has been read as 1.
7 The I2C releases the SCL and transmits the byte.
8 The master may hold the I2C bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

31.3.3.3 Slave-Receiver Operation for a Single Byte

When another I2C master device on the bus addresses the I2C and is sending data, the I2C acts as a slave-receiver and the following steps occur:

1 The other I2C master device initiates an I2C transfer with an address that matches the I2C's slave address in the I2CSAR register.
2 The I2C acknowledges the sent address and recognizes the direction of the transfer to indicate that the I2C is acting as a slave-receiver.
3 I2C receives the transmitted byte and places it in the receive buffer.

NOTE: If the RX FIFO is completely filled with data when a byte is pushed, then an overflow occurs and the I2C continues with subsequent I2C transfers. Because a NACK is not generated, software must recognize the overflow when indicated by the I2C (by the RXOF bit in the I2CINTST register) and take appropriate actions to recover from lost data. Hence, there is a real time constraint on software to service the RX FIFO before the latter overflow as there is no way to re-apply pressure to the remote transmitting master. You must select a deep enough RX FIFO depth to satisfy the interrupt service interval of their system.

4 I2C asserts the RX_FULL interrupt (I2CINTST[2] register).
If the RX_FULL interrupt has been masked, due to setting I2CINTM[2] register to 0 or setting I2CTX_TL to a value larger than 0, then it is recommended that a timing routine (described in "Slave-Transmitter Operation for a Single Byte" on page 57) be implemented for periodic reads of the "I2CST" on page 136 register. Reads of the I2CST register, with bit 3 (RFNE) set at 1, must then be treated by software as the equivalent of the RX_FULL interrupt being asserted.
5 Software may read the byte from the I2CDC register (bits 7:0).

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6 The other master device may hold the I2C bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

31.3.3.4 Slave-Transfer Operation For Bulk Transfers

In the standard I2C protocol, all transactions are single byte transactions and the programmer responds to a remote master read request by writing one byte into the slave's TX FIFO.

When a slave (slave-transmitter) is issued with a read request (RDREQ) from the remote master (master-receiver), at a minimum there should be at least one entry placed into the slave-transmitter's TX FIFO.

I2C is designed to handle more data in the TX FIFO so that subsequent read requests can take that data without raising an interrupt to get more data. Ultimately, this eliminates the possibility of significant latencies being incurred between raising the interrupt for data each time had there been a restriction of having only one entry placed in the TX FIFO.

This mode only occurs when I2C is acting as a slave-transmitter. If the remote master acknowledges the data sent by the slave-transmitter and there is no data in the slave's TX FIFO, the I2C holds the I2C SCL line low while it raises the read request interrupt (RDREQ) and waits for data to be written into the TX FIFO before it can be sent to the remote master.

If the RDREQ interrupt is masked, due to bit 5 (MRDREQ) of the I2CINTST register being set to 0, then it is recommended that a timing routine be used to activate periodic reads of the I2CINTST register. Reads of I2CINTST that return bit 5 (RDREQ) set to 1 must be treated as the equivalent of the RDREQ interrupt referred to in this section.

The RDREQ interrupt is raised upon a read request, and like interrupts, must be cleared when exiting the interrupt service handling routine (ISR). The ISR allows you to either write 1 byte or more than 1 byte into the TX FIFO. During the transmission of these bytes to the master, if the master acknowledges the last byte. Then the slave must raise the RDREQ again because the master is requesting for more data.

31.3.4 Disabling I2C

The register I2CENBST is added to allow software to unambiguously determine when the hardware has completely shutdown in response to the I2CENB register being set from 1 to 0.

31.3.4.1 Procedure

1 Define a timer interval (ti2c_poll) equal to the 10 times the signaling period for the highest I2C transfer speed used in the system and supported by I2C. For example, if the highest I2C transfer mode is 400 kb/s, then this ti2c_poll is 25us.

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2 Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.

3 Execute a blocking thread/process/function that prevents any further I2C master transactions to be started by software, but allows any pending transfers to be completed.
NOTE: This step can be ignored if I2C is programmed to operate as an I2C slave only.

4 The variable POLL_COUNT is initialized to zero.

5 Set I2CENB to 0.

6 Read the I2CENBST register and test the I2C_EN bit (bit 0). Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.

7 If I2CENBST[0] is 1, then sleep for ti2c_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

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32 Synchronous Serial Interface

32.1 Overview

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSI operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 54 MHz. Serial data formats may range from 2 to 17 bits in length. The SSI provides 128 entries deep x 17 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA transfers while receiving or transmitting.

Features:

- 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
- Full-duplex or transmit-only or receive-only operation
- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 17 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SSI format
- Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

32.2 Pin Description

Table 32-1 Micro Printer Controller Pins Description

Name	I/O	Description
SSI_CLK	Output	Serial bit-rate clock
SSI_CE_	Output	First slave select enable
SSI_CE2_	Output	Second slave select enable
SSI_GPC	Output	General purpose control signal to external chip
SSI_DT	Output	Transmit data (serial data out)
SSI_DR	Input	Receive data (serial data in)

SSI_CLK is the bit-rate clock driven from the SSI to the peripheral. SSI_CLK is toggled only when data

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is actively being transmitted and received.

SSI_CE_ or SSI_CE2_ are the framing signal, indicating the beginning and the end of a serialized data word.

SSI_DT and SSI_DR are the Transmit and Receive serial data lines.

SSI_GPC is general-purpose control signal, synchronized with SSI_CLK, can be used for LCD control.

32.3 Register Description

The SSI has seven registers: one data, two control, one status, one bit-rate control, and two interval control registers. The table lists these registers.

Table 32-2 SSI Serial Port Registers

Name	RW	Reset Value	Address Offset	Access Size
SSIDR0	RW	0x??	0x10043000	32
SSICR00	RW	0x0000	0x10043004	16
SSICR10	RW	0x00087860	0x10043008	32
SSISR0	RW	0x00000098	0x1004300C	32
SSIITR0	RW	0x0000	0x10043010	16
SSIICR0	RW	0x00	0x10043014	8
SSIGR0	RW	0x0000	0x10043018	16
SSIDR1	RW	0x??	0x10045000	32
SSICR01	RW	0x0000	0x10045004	16
SSICR11	RW	0x00087860	0x10045008	32
SSISR1	RW	0x00000098	0x1004500C	32
SSIITR1	RW	0x0000	0x10045010	16
SSIICR1	RW	0x00	0x10045014	8
SSIGR1	RW	0x0000	0x10045018	16

NOTE: There two SSI controller. SSI0 whose base address is 0x100430xx and SSI1 whose base address is 0x100450xx.

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32.3.1 SSI Data Register (SSIDR)

SSIDR 0x10043000, 0x10045000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															GPC/D16	Transmit/Receive Data															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	GPC/D16	This bit can be used as normal data bus bit 16 or GPC bit alternatively. When it is used as normal data bus bit, it's readable / writable; when SSI_GPC is used, it is GPC bit for SSI_GPC pin output and it's write-only.	RW
15:0	Transmit/ Receive Data	Data word to be written to/read from Transmit/Receive FIFO. When the transfer frame length is less than 17-bit, received data is automatically right justified in the receive-FIFO and the upper unused bits are filled with '0'. For transmission, the upper unused bits of the data written into SSIDR is ignored by the transmit logic. (**NOTE:** "upper unused bits" does not include the SSIDR.GPC bit. National microwire format includes format 1 and format2, when national microwire format 2 is selected, Bit 16 of SSIDR is defined as read/write operation judge bit, if it is 0, bit 15~0 represent one read command; if it is 1, bit 15~0 represent one write command and following is the written data. So the maximum length of one command (is defined in MCOM) is 16, the maximum length of one written or read data (is defined in FLEN) can be 17. Transmit-FIFO only contain one read operation command once, or one write operation command and its data once, after transmit-FIFO is empty, next command can be filled in transmit-FIFO.	RW

32.3.2 SSI Control Register0 (SSICR0)

SSICR0 0x10043004, 0x10045004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSIE	TIE	RIE	TEIE	REIE	LOOP	RFINE	RFINC	EACLRUN	FSEL	Reserved		TFMODE	TFLUSH	RFLUSH	DISREV
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>15</td><td>SSIE</td><td>This bit is used to enable/disable SSI module. 0: disable; 1: enable.
Clearing SSIE will not reset SSI FIFO, SSICR0, SSICR1, SSIGR, SSIITR and SSIICR automatically. Software should ensure the FIFOs/registers are properly configured and be flush/reset manually when necessary before enabling SSI.</td><td>RW</td></tr>
<tr><td>14</td><td>TIE</td><td>This bit enables/disables the transmit-FIFO half-empty interrupt TXI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>13</td><td>RIE</td><td>This bit enables/disables the receive-FIFO half-full interrupt RXI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>12</td><td>TEIE</td><td>This bit enables/disables the transmit-error interrupt TEI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>11</td><td>REIE</td><td>This bit enables/disables the receive-error interrupt REI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>10</td><td>LOOP</td><td>Used for test purpose. In loop mode, the output of SSI transmit shift register is connected to input of SSI receive shift register internally. The data received should be the same as the data transmitted. And do not output any valid signals on the pins.
0: normal SSI mode; 1: LOOP mode.</td><td>RW</td></tr>
<tr><td>9</td><td>RFINE</td><td>This bit enables/disables receive finish control function.
0: disable; 1: enable.
For SSICR1.FMAT = B’10 (National Microwire format 1 is selected), SSICR0.RFINE must be 0.</td><td>The receive finish condition list below:<table><tr><th>RFINE</th><th>RFINC</th><th>Receive Finish Condition</th></tr><tr><td>0</td><td>x</td><td>Same as transmit completion condition (transmit-fifo is empty and SSICR1.UNFIN = 0)</td></tr><tr><td>1</td><td>0</td><td>Receive continue</td></tr><tr><td>1</td><td>1</td><td>Receive finish</td></tr></table></td><td>RW</td></tr>
<tr><td>8</td><td>RFINC*</td><td>Receive finish control bit.
0: receive continue
1: receive finished</td><td>RW</td></tr>
<tr><td>7</td><td>EACLRUN</td><td>0: don’t auto clear under flag, software clear under
1: software auto clear under flag when tfifo don’t empty</td><td>RW</td></tr>
<tr><td>6</td><td>FSEL</td><td>This bit sets the frame signal to be used for slave select. The unselected frame signal always output invalid level.
0: SSI_CE_ is selected
1: SSI_CE2_ is selected</td><td>RW</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>3</td><td>TFMODE</td><td>0: new fifo empty mode
1: old fifo empty mode</td><td>RW</td></tr>
<tr><td>2</td><td>TFLUSH</td><td>Flush the transmit FIFO when set to 1. Always return 0 when read.</td><td>RW</td></tr>
</table>

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1	RFLUSH	Flush the receive FIFO when set to 1. Always return 0 when read.	RW
0	DISREV	This bit enables/disables receive function. 0: enable; 1: disable.	RW

NOTE:

***:** When transmitting finished or for receive-only operation, transmit function can be disabled and this bit is used to control receiving completion, and the SSI will consume less power.

When the finish condition is set, the receiving will complete after present character is completely shifted in, then the SSI will stop the SSI_CLK and negate the SSI_CE_ / SSI_CE2_ if necessary. To make sure present transfer is completed, user must read and get SSISR.END = 1 (or SSISR.BUSY = 0).

32.3.3 SSI Control Register1 (SSICR1)

SSICR1 **0x10043008, 0x10045008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRMHL		TFVCK		TCKFI		LFST	ITFRM	UNFIN	Reserved	FMAT		TTRG		MCOM		RTRG		FLEN						Reserved				PHA		POL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:30	FRMHL	Frame valid level select, FRMHL [1: 0] correspond to SSI_CE2_ and SSI_CE_ respectively. **FRMHL[1:0]** / **Description** / 00 / SSI_CE_ is low level valid and SSI_CE2_ is low level valid / Initial value 01 / SSI_CE_ is high level valid and SSI_CE2_ is low level valid / 10 / SSI_CE_ is low level valid and SSI_CE2_ is high level valid / 11 / SSI_CE_ is high level valid and SSI_CE2_ is high level valid /	RW
29:28	TFVCK	Time from frame valid to clock start, that provide programmable time delay from frame (SSI_CE_ /SSI_CE2_) assert edge to SSI_CLK leading edge. When TFVCK = B'00, the time is fixed half SSI_CLK or one SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'01, SSICR1.TFVCK is ignored. **TFVCK[1:0]** / **Description** / 00 / Ignore (default half or one SSI_CLK / Initial value	RW

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			cycle delay time)	
		01	1 more SSI_CLK cycle delay time is added	
		10	2 more SSI_CLK cycle delay time is added	
		11	3 more SSI_CLK cycle delay time is added	
27:26	TCKFI	Time from clock stop to frame invalid, provide programmable time delay from SSI_CLK last edge to frame (SSI_CE_ /SSI_CE2_) negate edge. When TCKFI = B'00, the time is fixed one SSI_CLK or half SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'01, SSICR1.TFVCK is ignored.		RW
		TCKFI[1:0]	**Description**	
		00	Ignore (default half or one SSI_CLK cycle delay time)	Initial value
		01	1 more SSI_CLK cycle delay time is added	
		10	2 more SSI_CLK cycle delay time is added	
		11	3 more SSI_CLK cycle delay time is added	
25	LFST	Set to LSB first or MSB first when transfer. 0: MSB first; 1: LSB first.		RW
24	ITFRM	Frame during interval, selects if the Frame (SSI_CE_ /SSI_CE2_) signal is negated or not during interval time at Interval Mode (SSICR1.FMAT = B'00 and SSIITR.IVLTM ≠ H'0000). It's ignored at Normal Mode. 0: SSI_CE_ /SSI_CE2_ de-asserts during interval time at Interval Mode 1: SSI_CE_ /SSI_CE2_ keeps asserted during interval time at Interval Mode		RW
23	UNFIN	This bit controls whether the SSI finishes transmission or wait for data filling (underrun happen) after all data in transmit-FIFO are sent out during transfer. This bit must be cleared to 0 when SSICR1.FMAT = B'01. (TI's SSP format) 0: Transmit-FIFO empty means end of transmission 1: Transmission didn't finish when transmit-FIFO is empty, SSI underrun error would occur and SSI waits for data filling; SSI_CLK and SSI_CE_ /SSI_CE2_ keeps asserted, SSI_CLK stop at the current level **NOTE:** For transmit-FIFO empty before any transfer after SSI enabled, if SSICR1.UNFIN = 1 or SSICR0.RFINE = 0, SSI will wait till transmit-FIFO isn't empty then start to transfer and no underrun error will occur; if SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer.		RW

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<table>
<tr><td>22</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>21:20</td><td>FMAT</td><td>These bits set the operating transfer format.
<table>
<tr><th>FMAT[1:0]</th><th>Description</th><th></th></tr>
<tr><td>00</td><td>Motorola’s SPI format</td><td>Initial value</td></tr>
<tr><td>01</td><td>TI’s SSP format</td><td></td></tr>
<tr><td>10</td><td>National Microwire 1 format</td><td></td></tr>
<tr><td>11</td><td>National Micowire 2 format</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>19:16</td><td>TTRG</td><td>These bits define the transmit-FIFO half-empty threshold value, which when equal or less characters left in transmit-FIFO, the SSISR.TFHE will be set to ‘1’.
0000: less than or equal to 1
n: less than or equal to nx8</td><td>RW</td></tr>
<tr><td>15:12</td><td>MCOM</td><td>When SSICR1.FMAT = B’10 or B’11 (National Microwire format 1 or 2 is selected), this bit decides the length of command from 1-bit to 16-bit. The length of written or read data is defined in FLEN. For SSICR1.FMAT ≠ B’10 or B’11, this bit is ignored.
<table>
<tr><th>MCOM[1:0]</th><th>Description</th><th></th></tr>
<tr><td>0000</td><td>1-bit command selected</td><td></td></tr>
<tr><td>0001</td><td>2-bit command selected</td><td></td></tr>
<tr><td>0010</td><td>3-bit command selected</td><td></td></tr>
<tr><td>0011</td><td>4-bit command selected</td><td></td></tr>
<tr><td>0100</td><td>5-bit command selected</td><td></td></tr>
<tr><td>0101</td><td>6-bit command selected</td><td></td></tr>
<tr><td>0110</td><td>7-bit command selected</td><td></td></tr>
<tr><td>0111</td><td>8-bit command selected</td><td>Initial value</td></tr>
<tr><td>1000</td><td>9-bit command selected</td><td></td></tr>
<tr><td>1001</td><td>10-bit command selected</td><td></td></tr>
<tr><td>1010</td><td>11-bit command selected</td><td></td></tr>
<tr><td>1011</td><td>12-bit command selected</td><td></td></tr>
<tr><td>1100</td><td>13-bit command selected</td><td></td></tr>
<tr><td>1101</td><td>14-bit command selected</td><td></td></tr>
<tr><td>1110</td><td>15-bit command selected</td><td></td></tr>
<tr><td>1111</td><td>16-bit command selected</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>11:8</td><td>RTRG
(SSI1)</td><td>These bits define the receive-FIFO half-full threshold value, which when equal or more characters received in receive-FIFO, the SSISR.RFHF will be set to ‘1’.
0000: more than or equal to 1
n: more than or equal to nx8</td><td>RW</td></tr>
<tr><td>9:8</td><td>RTRG
(SSI0)</td><td>These bits define the receive-FIFO half-full threshold value, which when equal or more characters received in receive-FIFO, the SSISR.RFHF will be set to “1”.
<table>
<tr><th>RTRG[1:0]</th><th>Description</th><th></th></tr>
</table></td><td>RW</td></tr>
</table>

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00	more than or equal to 1	Initial value	
01	more than or equal to 4		
10	more than or equal to 8		
11	more than or equal to 14		

7:4	FLEN	These bits set the bit length of every character to be transmitted/received. The maximum data length can be configured is 17 bits. For data length longer than 17 bits (multiples of the SSICR1.FLEN configured length), the software should ensure properly processing. When SSI_GPC pin is used, the FLEN shouldn't be configured as B'1111 (17-bit data). When TI SSP mode is selected (FMAT = 2'b01), 2-bit data length (FLEN = 4'b0000) isn't supported.	RW

MCOM[1:0]	Description	
0000	2-bit data	
0001	3-bit data	
0010	4-bit data	
0011	5-bit data	
0100	6-bit data	
0101	7-bit data	
0110	8-bit data	Initial value
0111	9-bit data	
1000	10-bit data	
1001	11-bit data	
1010	12-bit data	
1011	13-bit data	
1100	14-bit data	
1101	15-bit data	
1110	16-bit data	
1111	17-bit data	

3:2	Reserved	Writing has no effect, read as zero.	R
1	PHA	This bit sets the phase of the SSI_CLK from the beginning of a data frame for Motorola's SPI format (SSICR1.FMAT = B'00). 0: The leading edge of SSI_CLK is used to sample data from SSI_DR after the SSI_CE_ /SSI_CE2_ goes valid, it is initial value 1: The leading edge of SSI_CLK is used to drive data onto SSI_DT after the SSI_CE_ /SSI_CE2_ goes valid	RW
0	POL	This bit sets SSI_CLK's idle state polarity for Motorola's SPI format. (SSICR1.FMAT = B'00). 0: SSI_CLK keeps low level when idle, when SSI_CE_ /SSI_CE2_ goes valid the leading clock edge is a rising edge, it is initial value 1: SSI_CLK keeps high level when idle, when SSI_CE_ /SSI_CE2_ goes valid the leading clock edge is a falling edge	RW

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32.3.4 SSI Status Register1 (SSISR)

SSISR **0x1004300C, 0x1004500C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TFIFO-NUM								RFIFO-NUM								END	BUSY	TFF	RFE	TFHE	RFHF	UNDR	OVER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	TFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R
15:8	RFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R
7	END	This bit indicates transfer end status. It is the inverse of SSISR.BUSY when transfer is in process, but it'll keep cleared at interval time before transfer is completed. It'll be set when transfer finished.	R
6	BUSY	This bit indicates SSI's working status. 0: SSI is idle or at interval time 1: Transmission and/or reception is in process	R
5	TFF	This bit denotes transmit-FIFO is full or not. 0: Transmit-FIFO is not full; 1: Transmit-FIFO is full.	R
4	RFE	This bit denotes receive-FIFO is empty or not. 0: Receive-FIFO is not empty 1: Receive-FIFO is empty	R
3	TFHE	This bit denotes whether the characters number in transmit-FIFO being less or equal to SSICR1.TTRG. 0: The data in transmit-FIFO is more than the condition set by SSICR1.TTRG 1: The data in transmit-FIFO meets the condition set by SSICR1.TTRG, If SSICR0.TIE = 1, it will generate SSI TXI interrupt	R
2	RFHF	This bit denotes whether the characters number in receive-FIFO being more or equal to the number set by SSICR1.RTRG. 0: The data in receive-FIFO is less than the condition set by SSICR1.RTRG 1: The data in receive-FIFO meets the condition set by SSICR1.RTRG, If SSICR0.RIE = 1, it will generate SSI RXI interrupt	R
1	UNDR	Transmit-FIFO underrun status. When underrun happens, SSI set this bit and keeps the current status of SSI_CLK and SSI_CE_/SSI_CE2_, waiting for transmit-FIFO filling. 0: Underrun has not occurred 1: Underrun has occurred, when SSICR0.TEIE is set, it will generate	RW

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		SSI TEI interrupt. Write '0' to clear this bit, writing '1' has no effect	
0	OVER	Receive-FIFO overrun status, new received data will lose. 0: Overrun has not occurred 1: Overrun has occurred; When SSICR0.REIE is set, it will generate SSI REI interrupt. Write '0' to clear this bit, writing '1' has no effect	RW

32.3.5 SSI Interval Time Control Register (SSIITR)

SSIITR 0x10043010, 0x10045010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CNTCLK	IVLTM														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	CNTCLK	Counting clock source select. 0: Use SSI bit clock (SSI_CLK) as the interval counter clock source 1: Use 32K clock as the interval counter clock source	RW
14:0	IVLTM	Interval time set, set the cycle number of counting clock source for desired interval time. When SSIITR.IVLTM = 0x0000, normal mode is selected, and SSIITR.CNTCLK and SSIICR are ignored. When SSIITR.IVLTM ≠ 0x0000, interval mode is selected. The interval time is calculated as follows: *Interval time ≈ [CNTCLK clock period] * [Value of IVLTM]* The actual interval time is as follow: When SSIITR.CNTCLK = 0: *Interval time = [CNTCLK clock period] * [Value of IVLTM] + 3 * device_clock period* When SSIITR.CNTCLK = 1: *Interval time ≥ [CNTCLK clock period] * [Value of IVLTM + 1] + 1 * device_clock period;* *Interval time ≤ [CNTCLK clock period] * [Value of IVLTM + 2] + 2 * device_clock period*	RW

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32.3.6 SSI Interval Character-per-frame Control Register (SSIICR)

SSIICR 0x10043014, 0x10045014

Bit	7	6	5	4	3	2	1	0
	Reserved					ICC		
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2:0	ICC	Sets the fixed number of characters to be transmitted / received each time during SSI_CLK changing (and SSI_CE_ / SSI_CE2_ asserting) in interval mode for SSICR1.FMAT = B'00 (Motorola's SPI format is selected). SSIICR is ignored for SSICR1.FMAT ≠ B'00. The desired transfer number of characters-per-frame is (SSIICR set value + 1).	RW

32.3.7 SSI Clock Generator Register (SSIGR)

SSIGR 0x10043018, 0x10045018

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CGV							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CGV	Sets the frequency of serial bit clock (SSI_CLK). The serial bit clock (SSI_CLK) is generated by dividing device-clock as follows: F_{SSI_CLK} = [Frequency of device clock] / (2 * (CGV + 1)) Device clock is generated in CPM module. The value in SSIGR can be set from 0 to 255, and initialized to 0x0000 on power-on reset.	RW

32.4 Functional Description

Serial data is transferred between the processor and external peripheral through FIFO buffers in the SSI. Data transfers to system memory are handled by either the CPU (using programmed I/O) or by DMA. Operation is full duplex - separate buffers and serial data paths permit simultaneous transfers to and from the external peripheral.

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Programmed I/O transmits and receives data directly between the CPU and the transmit/receive FIFO's. The DMA controller transfers data during transmit and receive operations between memory and the FIFO's.

Transmit data is written by the CPU or DMA to the SSI's transmit FIFO. The SSI then takes the data from the FIFO, serializes it, and transmits it via the SSI_DT signal to the peripheral. Data from the peripheral is received via the SSI_DR signal, converted to parallel words and is stored in the Receive FIFO. Read operations automatically target the receive FIFO, while write operations write data to the transmit FIFO. Both the transmit and receive FIFO buffers are 128 entries deep by 17 bits wide. As the received data fills the receive FIFO, a programmable threshold triggers an interrupt to the Interrupt Controller. If enabled, an interrupt service routine responds by identifying the source of the interrupt and then performs one or several read operations from the inbound (receive) FIFO buffer.

32.5 Data Formats

Four signals are used to transfer data between the processor and external peripheral. The SSI supports three formats: Motorola SPI, Texas Instruments SSP, and National Microwire. Although they have the same basic structure the three formats have significant differences, as described below:

1 SSI_CE_/SSI_CE2_ varies for each protocol as follows:
   - For SPI and Microwire formats, SSI_CE_/SSI_CE2_ functions as a chip select to enable the external device (target of the transfer), and is held active-low during the data transfer.
   - For SSP format, this signal is pulsed high for one serial bit-clock period at the start of each frame.

2 SSI_CLK varies for each protocol as follows:
   - For Microwire, both transmit and receive data sources switch data on the falling edge of SSI_CLK, and sample incoming data on the rising edge.
   - For SSP, transmit and receive data sources switch data on the rising edge of SSI_CLK, and sample incoming data on the falling edge.
   - For SPI, the user has the choice of which edge of SSI_CLK to use for switching outgoing data, and for sampling incoming data. In addition, the user can move the phase of SSI_CLK, shifting its active state one-half period earlier or later at the start and end of a frame.

While SSP and SPI are full-duplex protocols, Microwire uses a half-duplex master-slave messaging protocol. At the start of a frame, a 1 or 2-byte control message is transmitted from the controller to the peripheral. The peripheral does not send any data. The peripheral interprets the message and, if it is a READ request, responds with requested data, one clock after the last bit of the requesting message.

The serial clock (SSI_CLK) only toggles during an active frame. At other times it is held in an inactive or idle state, as defined by its specified protocol.

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32.5.1 Motorola's SPI Format Details

32.5.1.1 General Single Transfer Formats

The figures below show the timing of general single transfer format.

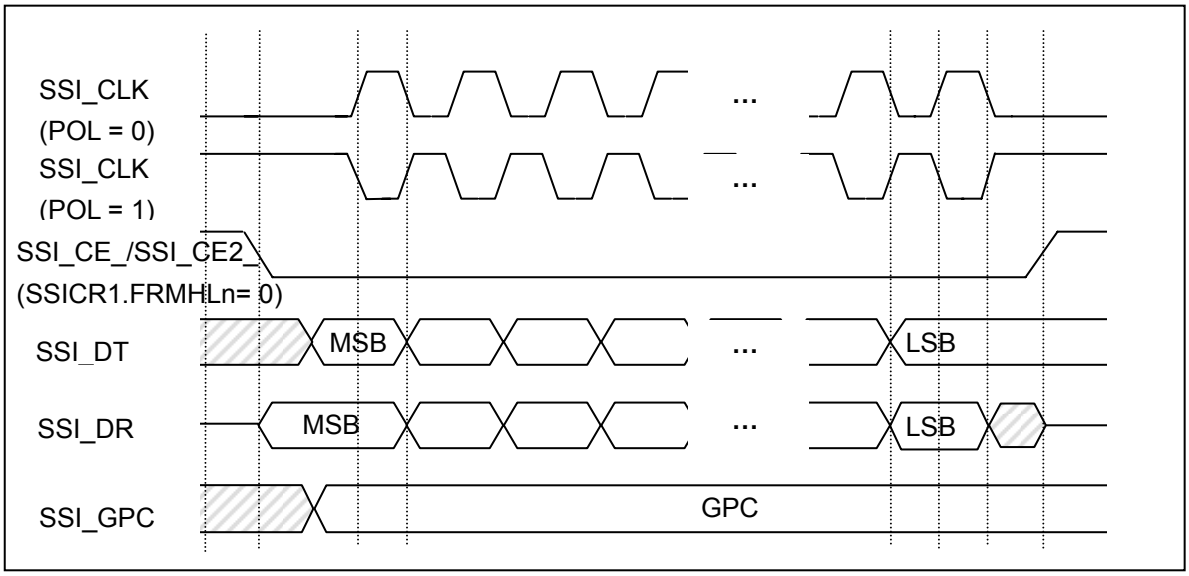


Figure 32-1 SPI Single Character Transfer Format (PHA = 0)

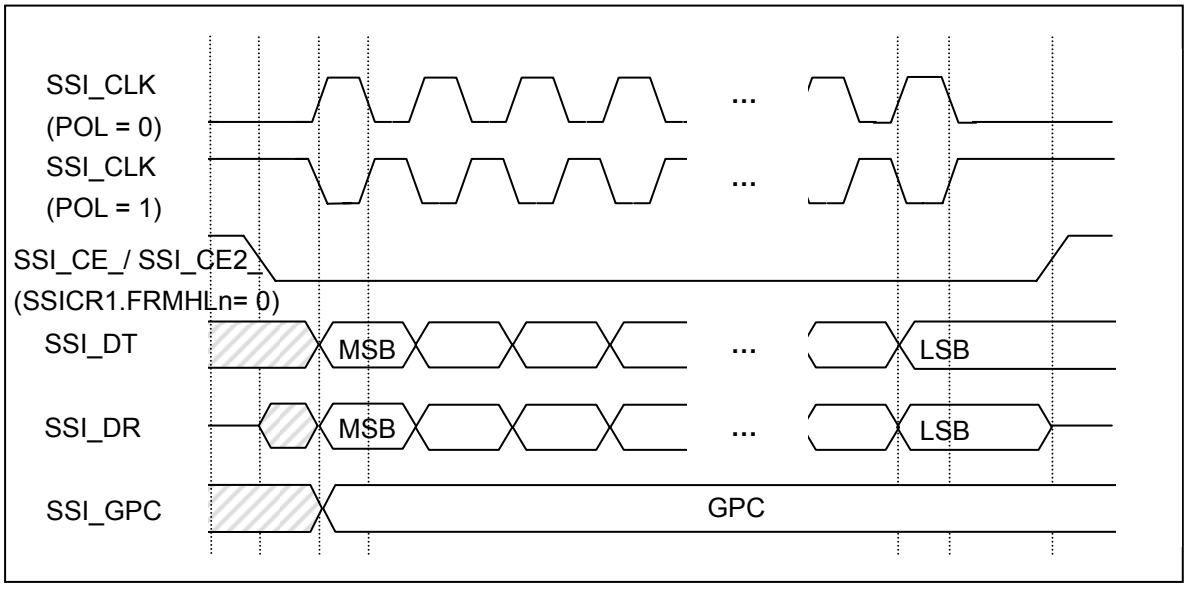


Figure 32-2 SPI Single Character Transfer Format (PHA = 1)

For SSICR1.PHA = 0, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears one SSI_CLK period after SSI_CE_ / SSI_CE2_ goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_CE_ / SSI_CE2_ negated half SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.

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For SSICR1.PHA = 1, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears half SSI_CLK period after SSI_CE_ / SSI_CE2_ goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_CE_ / SSI_CE2_ negated one SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.
Data is sampled from SSI_DR at every rising edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1) or at every falling edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0). According to SPI protocol, input data on SSI_DR should be stable at every sample clock edge.

Drive data onto SSI_DT at every rising edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0) or at every falling edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1).

32.5.1.2 Back-to-Back Transfer Formats

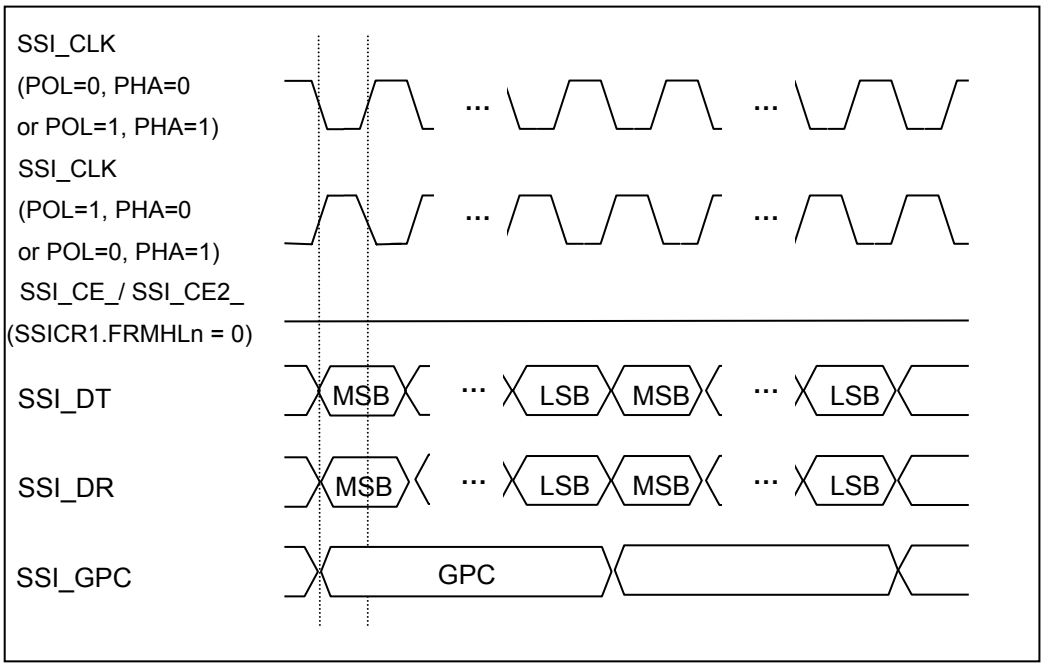


Figure 32-3 SPI Back-to-Back Transfer Format

For Motorola's SPI format transfers those continuous characters are exchanged during SSI_CE_ / SSI_CE2_ being valid, the timing is illustrated in the figure (SSICR1.LFST = 0).

Back-to-back transfer is performed as transmit-only/full-duplex operation when transmit-FIFO is not empty before the completion of the last character's transfer or performed as receive-only operation.

32.5.1.3 Frame Interval Mode Transfer Format

When in interval mode (SSIITR. IVLTM ≠ '0'), SSI always wait for an interval time (SSIITR.IVLTM), transfer fixed number of characters (SSIICR), then repeats the operation.

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When SSICR0.RFINE = 1, if transmit-FIFO is still empty after the interval time, receive-only transfer will occur.

During interval-wait time, SSI stops SSI_CLK, and when SSICR1.ITFRM = 0 it negates the SSI_CE_ / SSI_CE2_, when SSICR1.ITFRM = 1 it keeps asserting the SSI_CE_ / SSI_CE2_.

For transfers finished with transmit-FIFO empty, if the SSI transmit-FIFO is empty before fixed number of characters being loaded to transfer (SSICR1.UNFIN must be 1), then the SSI will set SSISR.UNDR = 1; if enabled, it'll send out a SSI underrun interrupt. At the same time, SSI will hold the SSI_CE_ / SSI_CE2_ and SSI_CLK signals at current status and wait for the transmit-FIFO filling. The SSI will continue transfer after transmit-FIFO being filled. The SSI always stops after completion of fixed number of characters' transfer (SSICR1.UNFIN must be 0) with transmit-FIFO empty.

For transfers finished by SSICR0.RFINC being valid set, the SSI will stop after finished current character transfer and needn't wait for a whole completion of fixed number of characters' transfer.

Two Interval transfer mode are illustrated in the following figures. In these timing diagram, SSICR1.PHA = 0, SSICR1.POL = 0 and SSIICR = 0.

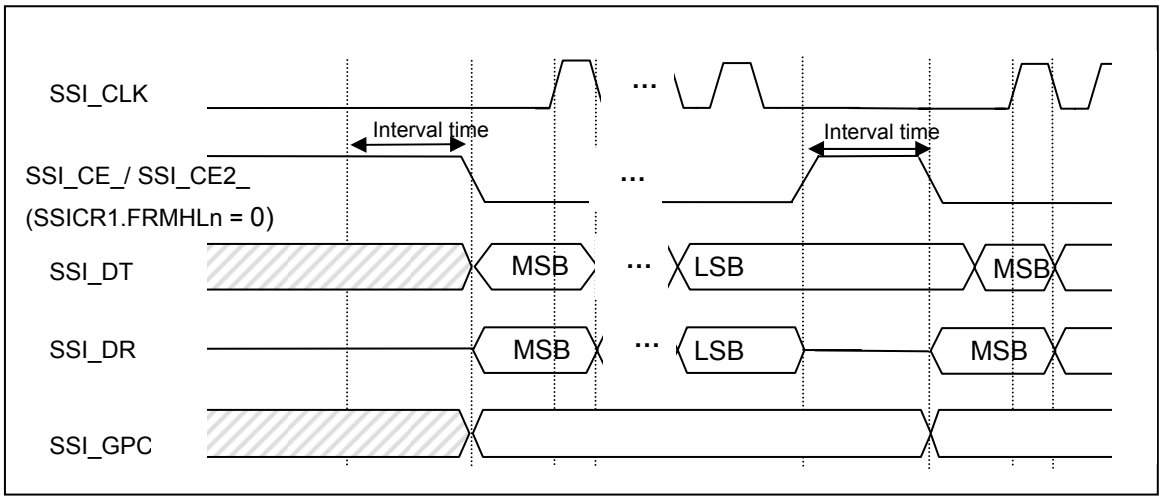


Figure 32-4 SPI Frame Interval Mode Transfer Format (ITFRM = 0, LFST = 0)

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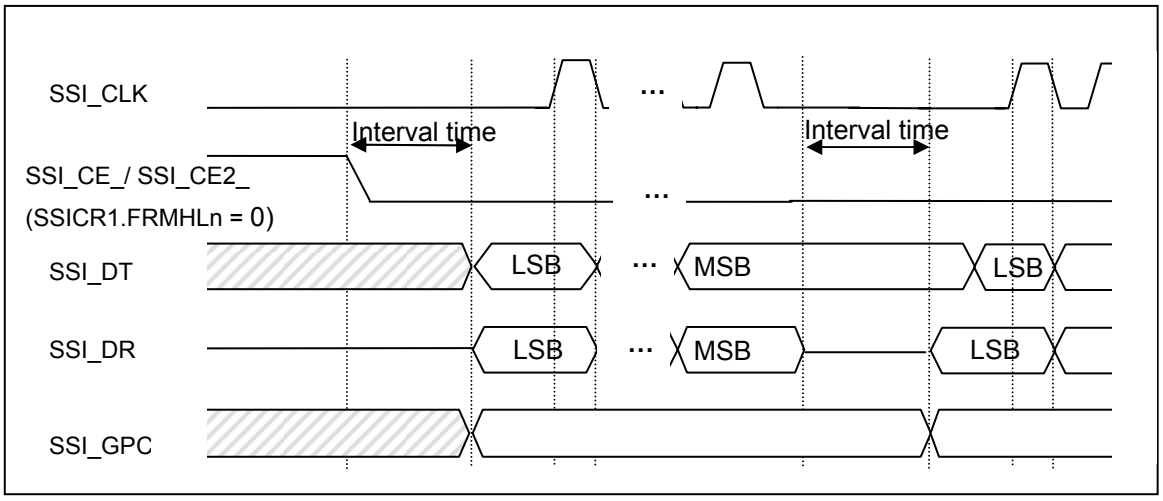


Figure 32-5 SPI Frame Interval Mode Transfer Format (ITFRM = 1, LFST = 1)

32.5.2 TI's SSP Format Details

In this format, each transfer begins with SSI_CE_ pulsed high for one SSI_CLK period. Then both master and slave drive data at SSI_CLK's rising edge and sample data at the falling edge. Data are transferred with MSB first or LSB first. At the end of the transfer, SSI_DT retains the value of the last bit sent through the next idle period.

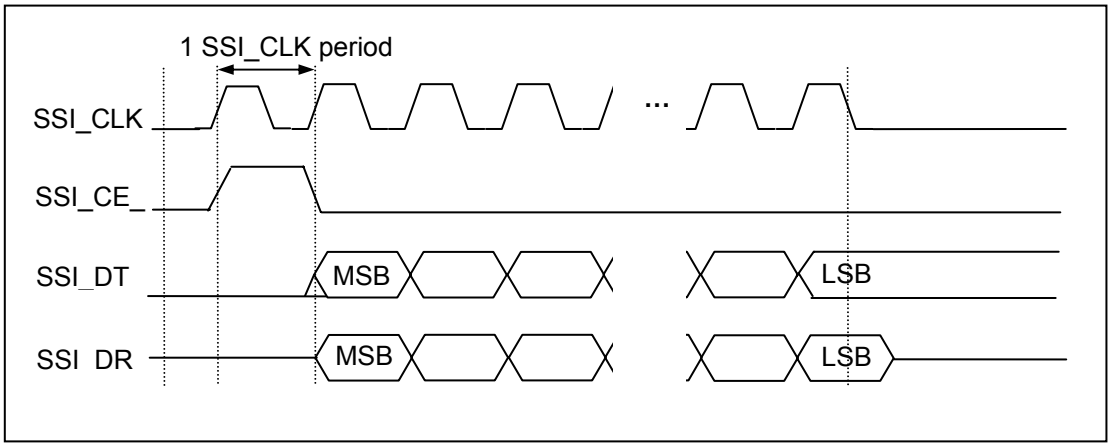


Figure 32-6 TI's SSP Single Transfer Format

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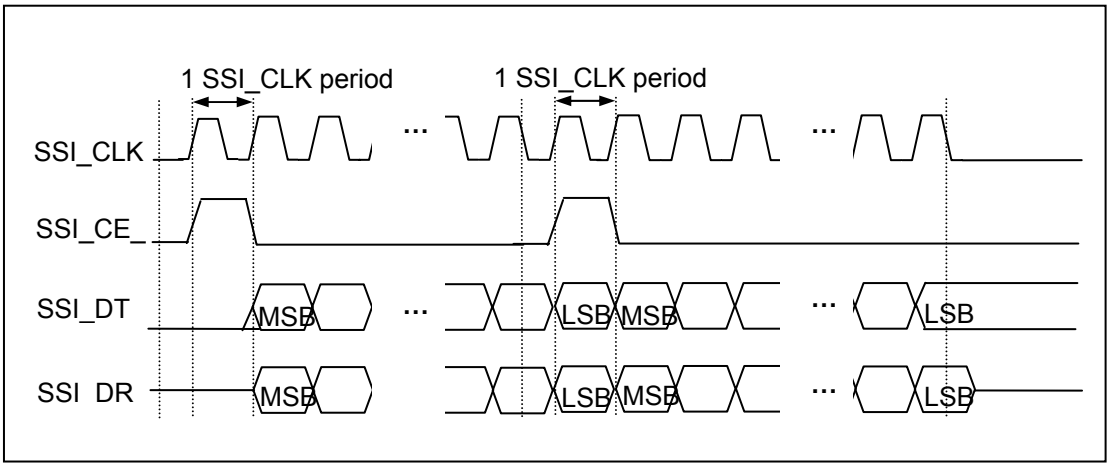


Figure 32-7 TI's SSP Back-to-back Transfer Format

32.5.3 National Microwire Format Details

It supports format 1 and format 2. If format 1 is selected, both master and slave drive data at SSI_CLK falling edge and sample data at the rising edge. If format 2 is selected, master drive and sample data at SSI_CLK falling edge, slave drive and sample data at SSI_CLK rising edge. SSI_CLK goes high midway through the command's most significant bit (or LSB) and continues to toggle at the bit rate. One bit clock (format 1) or half one bit clock (format 2) period after the last command bit, the external slave must return the serial data requested, with most significant bit first (or LSB first) on SSI_DR. SSI_CE_ / SSI_CE2 de-asserts high half clock (SSI_CLK) period (and 1/2/3 additional clock periods) later. Format 1 support back-to-back transfer, the start and end of back-to-back transfers are similar to those of a single transfer. However, SSI_CE_ / SSI_CE2 remains asserted throughout the transfer. The end of a character data on SSI_DR is immediately followed by the start of the next command byte on SSI_DT.

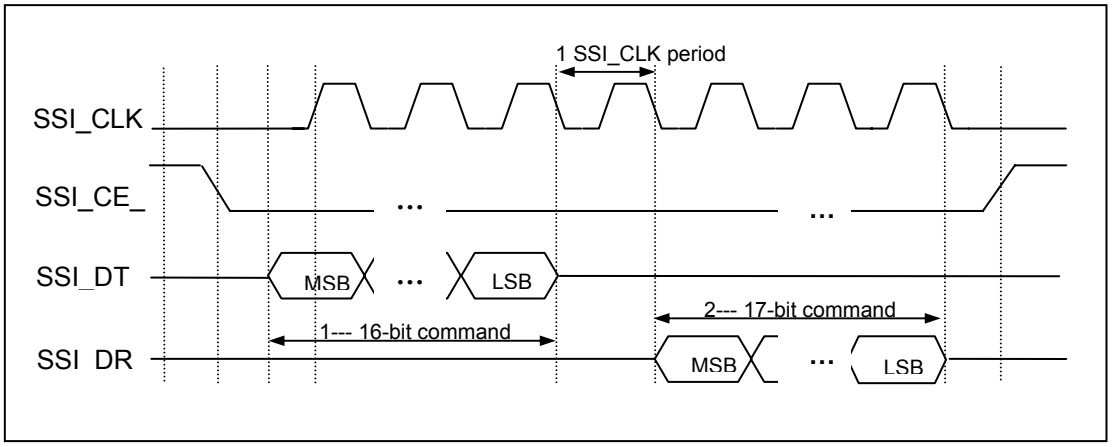


Figure 32-8 National Microwire Format 1 Single Transfer

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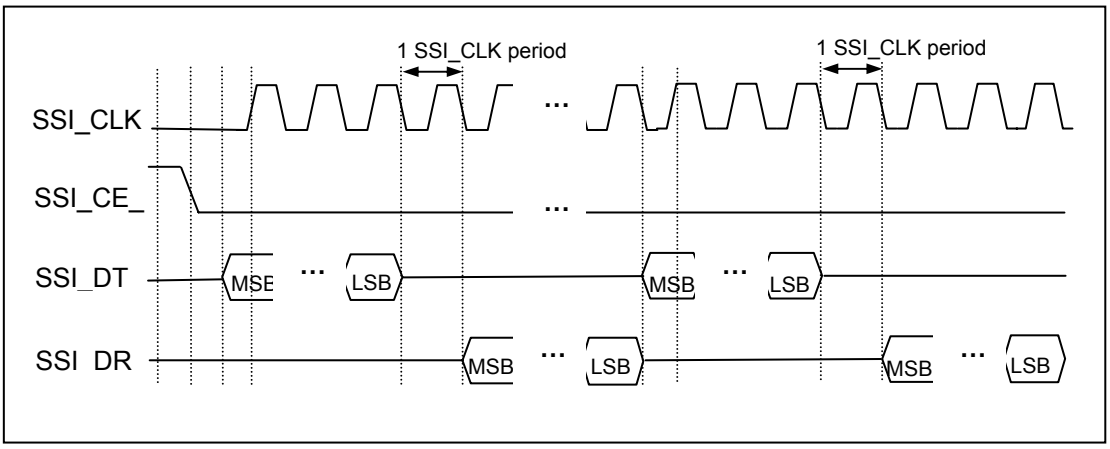


Figure 32-9 National Microwire Format 1 Back-to-back Transfer

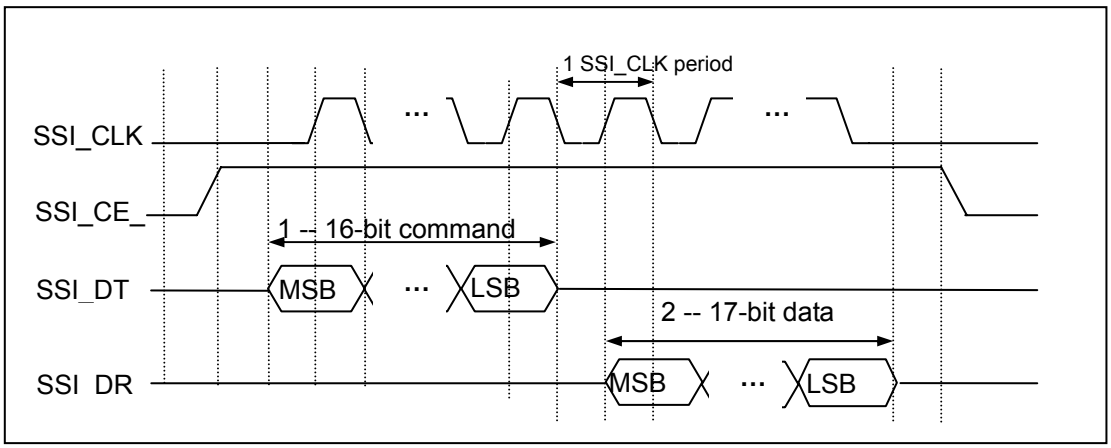


Figure 32-10 National Microwire Format 2 Read Timing

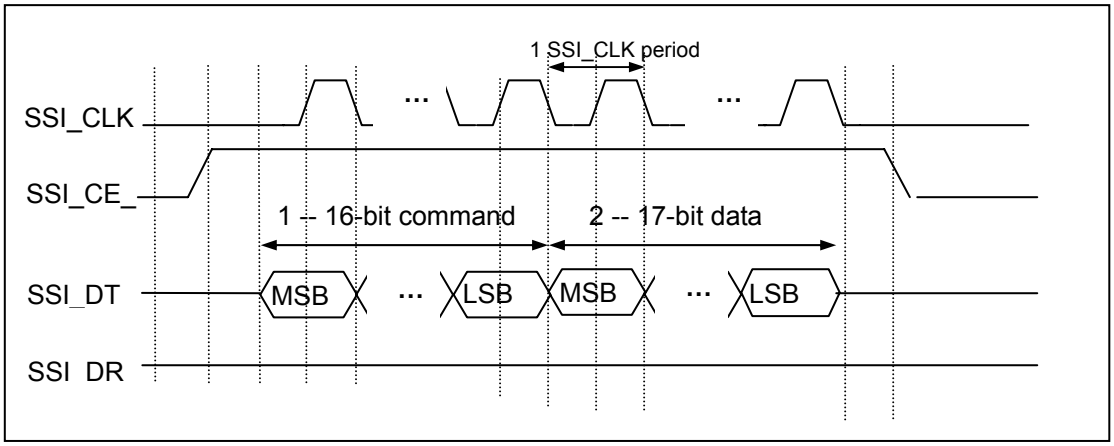


Figure 32-11 National Microwire Format 2 Write Timing

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32.6 Interrupt Operation

In SSI, there are TXI, RXI, TEI and REI total 4 interrupts, all these interrupts are combined together to make one SSI interrupt, which can be masked by writing '1' into corresponding mask bit in INTC interrupt mask register (IMR).

Table 32-3 SSI Interrupts

Operation	Condition	Flag Bit	Mask Bit	Interrupt	DMAC Activation
Transmit	T-FIFO is half-empty or less	SSISR.TFHE	SSICR0.TIE	**TXI**	Possible
	Transmit underrun error	SSISR.UNDR	SSICR0.TEIE	**TEI**	Impossible
Receive	R-FIFO is half-full or more	SSISR.RFHF	SSICR0.RIE	**RXI**	Possible
	Receive overrun error	SSISR.OVER	SSICR0.REIE	**REI**	Impossible

Either SSISR.TFHE or SSISR.RFHF can activate DMA transferring when corresponding individual interrupt mask bit in SSICR0 is cleared (masked) and DMA is enabled and configured.

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33 One-Wire Bus Interface

33.1 Overview

The OWI has the following features:

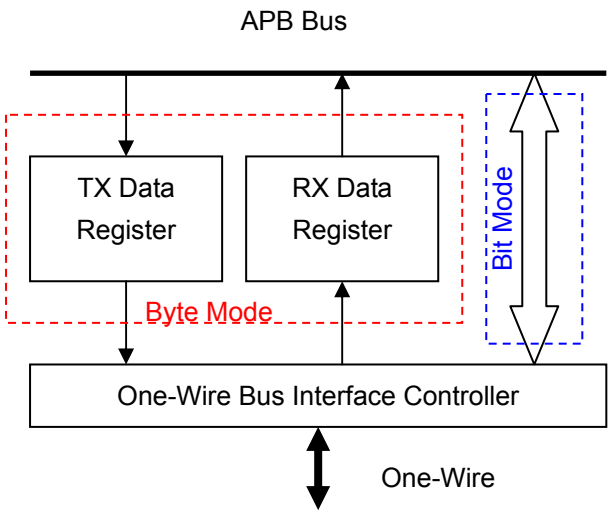
- Support 1-wire bus protocol
- Support Overdrive speed mode and Regular speed mode
- Data is transferred with the LSB first
- Support bit operate mode and byte operate mode
- OWI is the only master on the bus

33.2 Pin Description

Table 33-1 One-Wire Controller Pins Description

Name	I/O	Description
OWDAT	Input/Output	One-Wire Data signal

33.3 Structure



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33.4 Register Description

Table 33-2 OWI Registers Description

Name	Description	RW	Reset Value	Address	Access Size
OWCFG	Configure Register	RW	0x00	0x10072000	8
OWCTL	Control Register	RW	0x00	0x10072004	8
OWSTS	Status Register	RW	0x00	0x10072008	8
OWDAT	Data Register	RW	0x00	0x1007200C	8
OWDIV	Clock Divide Register	RW	0x00	0x10072010	8

33.4.1 One-Wire Configure Register (OWCFG)

OWCFG **0x10072000**

Bit	7	6	5	4	3	2	1	0
	MODE	RDDATA	WRDATA	RDST	WR1/RD	WR0	RST	ENA
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	MODE	OWI mode select. 0: Regular speed mode 1: Overdrive speed mode	RW
6	RDDATA	Receive a byte from one-wire bus. This bit is cleared when receive data is complete. The value of received data is stored in OWDAT, and is valid after RDDATA is self-cleared. 0:Do nothing/Receive data is completed 1:Receive data from one-wire bus and stored in OWDAT	RW
5	WRDATA	Transmit the data in OWDAT. This bit is cleared when the transmission of data is complete. 0: Do nothing/Transmission of data completed 1: Transmit the data in OWDAT	RW
4	RDST	Read status. This bit is valid after the WR1/RD bit is self-cleared. 0: 0 was sampled during a read 1: 1 was sampled during a read	R
3	WR1/RD	Write 1/ Read. This bit is cleared when the write of the bit is complete. The valve of one wire can be read, since the Write 1 and Read timing are identical. The value of the read bit is stored in RDST, and is valid after WR1/RD is self-cleared. 0: Do nothing/Write 1 sequence completed	RW

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		1: Generate Write 1 sequence on line	
2	WR0	Write 0 on line. This bit is cleared after the presence is determined. 0: Do nothing/Write 0 sequence completed 1: Generate Write 0 sequence on line	RW
1	RST	Reset presence pulse. This bit is cleared after the presence is determined. 0: Do nothing. Reset pulse completed 1: Generate reset pulse and sample slaves presence pulse	RW
0	ENA	Enable of OWI operation. 1: Write 1 to this bit to enable the OWI operation 0: Write 0 to this bit to disable the OWI operation	RW

NOTE: To make the OWI operate normally, only one of the RST, RDDATA, WRDATA, WR1/RD and WR0 is equal to 1.

33.4.2 One-Wire Control Register (OWCTL)

OWCTL **0x10072004**

Bit	7	6	5	4	3	2	1	0
	Reserved					EBYTE	EBIT	ERST
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	EBYTE	Enable byte write / read interrupt.	RW
1	EBIT	Enable bit write / read interrupt.	RW
0	ERST	Enable reset sequence finished interrupt.	RW

33.4.3 One-Wire Status Register (OWSTS)

OWSTS **0x10072008**

Bit	7	6	5	4	3	2	1	0
	PST	Reserved				BYTE_RDY	BIT_RDY	PST_RDY
RST	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
7	PST	Whether the 1-wire bus has device or not. This bit is valid after the RST bit is self-cleared. 1:The 1-wire bus has device on it 0:The 1-wire bus has no device on it	RW
6:3	Reserved	Writing has no effect, read as zero.	R
2	BYTE_RDY	Have received or transmitted a data.	RW
1	BIT_RDY	Have received or transmitted a bit.	RW
0	PST_RDY	Have finished a reset pulse.	RW

33.4.4 One-Wire Data Register (OWDAT)

OWDAT **0x1007200C**

Bit	7	6	5	4	3	2	1	0
	DATA							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	DATA	Store the received data and is valid after RDDATA is self-cleared. Prepare the transmission data for transmitting.	RW

33.4.5 One-Wire Clock Divide Register (OWDIV)

OWDIV **0x1007200C**

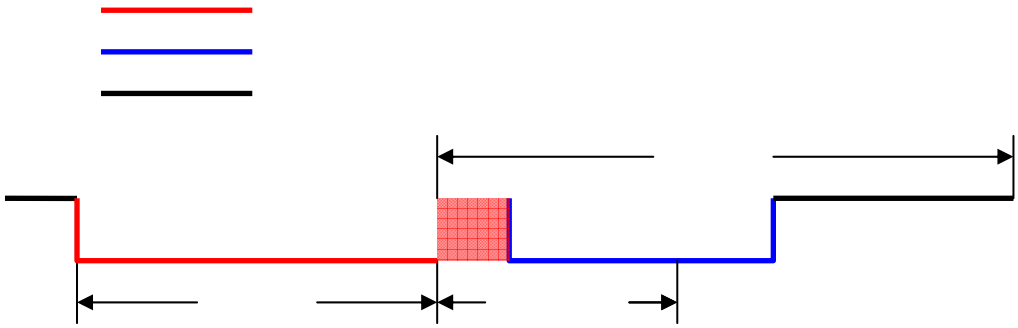
Bit	7	6	5	4	3	2	1	0
	Reserved		CLKDIV					
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	CLKDIV	Controls the divider used to create the DEV_CLK based upon the CPM_OWI_SYSCLK. When the OWI work in the regular speed mode: 1 MHz = DEV_CLK = CPM_OWI_SYSCLK / (CLKDIV + 1). When the OWI work in the overdrive speed mode: 4 MHz = DEV_CLK = CPM_OWI_SYSCLK / (CLKDIV + 1).	RW

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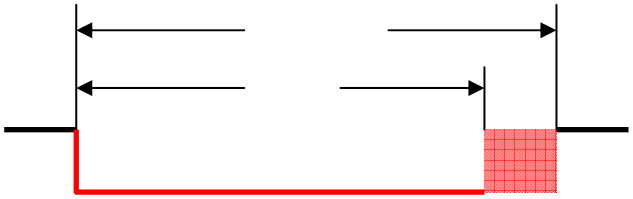
33.5 One-Wire Bus Protocol

33.5.1 Reset Timing and ACK Timing



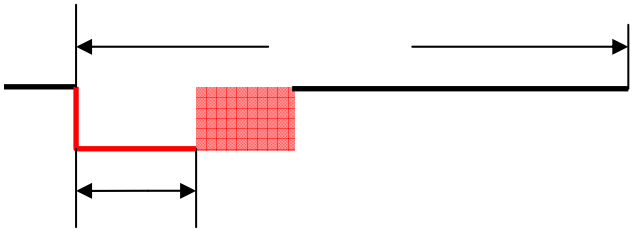
	RSTH	RSTL	RSTS
Regular Speed mode	512us	512us	68us
Overdrive Speed mode	64us	64us	8us

33.5.2 Write 0 Timing



	SLOT	LOW0
Regular Speed mode	128us	100us
Overdrive Speed mode	16us	12us

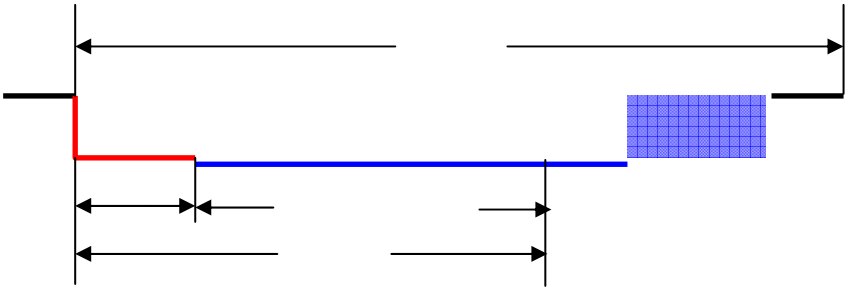
33.5.3 Write 1 Timing



	SLOT	LOW1
Regular Speed mode	128us	5us
Overdrive Speed mode	16us	1.25us

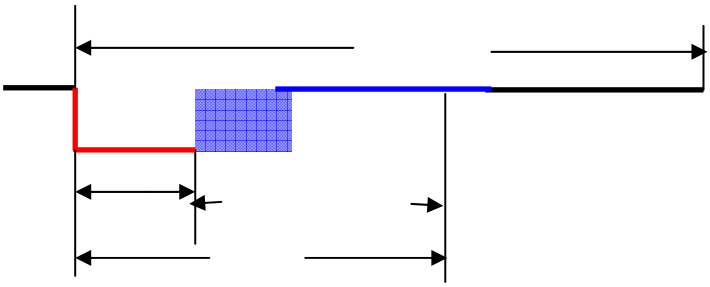
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33.5.4 Read0 Timing



	SLOT	LOWR	RDS
Regular Speed mode	128us	5us	13us
Overdrive Speed mode	16us	1.25us	1.75us

33.5.5 Read1 Timing



	SLOT	LOWR	RDS
Regular Speed mode	128us	5us	13us
Overdrive Speed mode	16us	1.25us	1.75us

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33.6 One-Wire Operation Guide

- **Interrupt operation guide:**
  1 Write the frequency divider to I2CGR.
  2 Set OWSTS to clear the flag.
  3 Set OWCTL to enable the operation interrupt.
  4 Select OWI mode (Regular speed mode or Overdrive speed mode).
  5 Set RST, RDDATA, WRDATA, WR1/RD or WR0 to choose one kind of operation.
  6 Set ENA to enable OWI.
  7 Wait till the interrupt happened, and the operation is finished.
  8 If you want to disable OWI when OWI is working, you should set ENA to 0 and till ENA is really set to 0, then you can do next operation.

- **CPU operation guide:**
  1 Write the frequency divider to I2CGR.
  2 Select OWI mode (Regular speed mode or Overdrive speed mode).
  3 Set RST, RDDATA, WRDATA, WR1/RD or WR0 to choose one kind of operation.
  4 Set ENA to enable OWI.
  5 Wait the ENA is cleared, and the operation is finished.
  6 If you want to disable OWI when OWI is working, you should set ENA to 0 and till ENA is really set to 0, then you can do next operation.

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34 USB Host Controller

34.1 Overview

This chapter describes the Universal Serial Bus host controller (UHC) implemented in the XBurst processor.

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals can be attached, configured, used, and detached, while the host and other peripherals continue operation.

Familiarity with the *Universal Serial Bus Specification*, Revision 1.1 and the OHCI specification are necessary to fully understand the material contained in this section.

Features:

- USB Rev. 1.1 compatible
- Supports both low-speed and full-speed USB devices
- Open Host Controller Interface (OHCI) Rev 1.0 compatible
- Root hub supports two data ports

34.2 Pin Description

Table 34-1 UHC Pins Description

Name	Type	Description
DPLS0	Inout	Data Positive to Port 0
DPLS1	Inout	Data Positive to Port 1
DMNS0	Inout	Data Minus to Port 0
DMNS1	Inout	Data Minus to Port 1

34.3 Register Description

The Host Controller (HC) contains a set of on-chip operational registers which are mapped into a noncacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the function of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as words.

Register Name	Description	RW	Reset Value	Address	Access

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					Size
HcRevision	Control and Status group	R	0x00000010	0x13430000	32
HcControl		RW	0x00000000	0x13430004	32
HcCommandStatus		RW	0x00000000	0x13430008	32
HcInterruptStatus		RW	0x00000000	0x1343000C	32
HcInterruptEnable		RW	0x00000000	0x13430010	32
HcInterruptDisable		RW	0x00000000	0x13430014	32
HcHCCA	Memory pointer group	RW	0x00000000	0x13430018	32
HcPeriodCurrentED		R	0x00000000	0x1343001C	32
HcControlHeadED		RW	0x00000000	0x13430020	32
HcControlCurrentED		RW	0x00000000	0x13430024	32
HcBulkHeadED		RW	0x00000000	0x13430028	32
HcBulkCurrentED		RW	0x00000000	0x1343002C	32
HcDoneHead		R	0x00000000	0x13430030	32
HcFmInterval	Frame counter group	RW	0x00002EDF	0x13430034	32
HcFmRemaining		R	0x00000000	0x13430038	32
HcFmNumber		R	0x00000000	0x1343003C	32
HcPeriodicStart		RW	0x00000000	0x13430040	32
HcLSThreshold		RW	0x00000628	0x13430044	32
HcRhDescriptorA	Root hub group	R/W	0x02000902	0x13430048	32
HcRhDescriptorB		RW	0x00060000	0x1343004C	32
HcRhStatus		RW	0x00000000	0x13430050	32
HcRhPortStatus 1		RW	0x00000100	0x13430054	32
HcRhPortStatus 2		RW	0x00000100	0x13430058	32

NOTE: *Open HCI – Open Host Controller Specification for USB* for details of the each register.

34.4 Introduction

The Host Controller is the device which is located between the USB bus and the Host Controller Driver in the OpenHCI architecture. The Host Controller is charged with processing all of the Data Type lists built by the Host Controller Driver. Additionally, the USB Root Hub is attached to the Host Controller.

The main functions as following:

- **USB States**: the Host Controller Operation with respect to the possible USB Bus states.
- **Frame Management**: all aspects of managing the 1-ms USB Frame.
- **List Processing**: the main function of the Host Controller. the detailed processing of the HCD-built Data Type lists.
- **Interrupt Processing**: the interrupt events tracked by the Host Controller and how the Host Controller provides interrupts for those events.
- **Root Hub**: the Root Hub support.

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35 OTG Controller

35.1 Overview

This chapter describes the USB On-The-Go (OTG) implemented in the processor.

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can plays the role of both host and device.

Familiarity with the *Universal Serial Bus Specification*, Revision 1.1 and OTG supplement are necessary to fully understand the material contained in this section.

Features:

- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the *On-The-Go* supplement to the USB 2.0 specification
- Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- UTMI+ Level 3 Transceiver Interface
- Soft connect/disconnect
- 5 DMA channels
- Supports control, interrupt, ISO and bulk transfer

35.2 Pin Description

Table 35-1 OTG Pins Description

Name	Type	Description
DP	Inout	Data Positive
DM	Inout	Data Minus
ID	Inout	Identification
drvvbus	Out	Charge pump enable

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35.3 Register Description

The OTG Controller (OTGC) contains a set of on-chip operational registers which are mapped into a noncacheable portion of the system addressable space. These registers are used by the OTG Controller Driver.

Table 35-2 OTG Registers Description

Name	Description	RW		Reset Value	Address	Access Size
		CPU	USB			
FAddr	Function address register	RW	R	8'h00	0x13440000	8
Power	Power management register	RW	RW	8'h20	0x13440001	8
IntrTx	Interrupt register for Endpoint 0 plus TX Endpoints 1 to 15	R	S	16'h0000	0x13440002	16
IntrRx	Interrupt register for Rx Endpoints 1 to 15	R	S	16'h0000	0x13440004	16
IntrTxE	Interrupt enable register for IntrTx	RW	R	16'hffff	0x13440006	16
IntrRxE	Interrupt enable register for IntrRx	RW	R	16'hfffe	0x13440008	16
IntrUSB	Interrupt register for common USB interrupts	R	S	8'h00	0x1344000a	8
IntrUSBE	Interrupt enable register for IntrUSB	RW	R	8'h06	0x1344000b	8
Frame	Frame Number	R	W	16'h0000	0x1344000c	16
Index	Index register for selecting the endpoint status and control registers	RW	R	4'h0	0x1344000e	4
TestMode	Enables the USB 2.0 test modes	RW	R	8'h00	0x1344000f	8
TxMaxP	Maximum packet size for peripheral TX endpoint (Index register set to select Endpoints 1 – 15 only)	RW	R	16'h0000	0x13440010	16
CSR0L/H	Control Status register for Endpoint 0 (Index register set to select Endpoint 0)	RW	RW	16'h0000	0x13440012	16
TxCSRL/H	Control Status register for peripheral TX endpoint (Index register set to select Endpoints 1 – 15)					
RxMaxP	Maximum packet size for	RW	R	16'h00	0x13440014	16

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	peripheral Rx endpoint (Index register set to select Endpoints 1 – 15 only)			00		
RxCSRL/H	Control Status register for peripheral Rx endpoint (Index register set to select Endpoints 1 – 15 only)	RW	RW	16'h0000	0x13440016	16
Count0	Number of received bytes in Endpoint 0 FIFO (Index register set to select Endpoint 0)	R	W	7'h00	0x13440018	7
RxCount	Number of bytes to be read from peripheral Rx endpoint FIFO (Index register set to select Endpoints 1 – 15)					
Type0	Defines the speed of Endpoint 0 (Index register set to select Endpoint 0)	RW	R	8'h0	0x1344001a	8
TxType	Sets the transaction protocol, speed and peripheral endpoint number for the host TX endpoint (Index register set to select Endpoints 1 – 15)					
NakLimit0	Sets the NAK response timeout on Endpoint 0 (Index register set to select Endpoint 0)	RW	R	8'h00	0x1344001b	8
TxInterval	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host TX endpoint (Index register set to select Endpoints 1 – 15 only)					
RxType	Sets the transaction protocol, speed and peripheral endpoint number for the host Rx endpoint (Index register set to select Endpoints 1 – 15 only)	RW	R	8'h00	0x1344001c	8
RxInterval	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Rx endpoint (Index register set to	RW	R	8'h00	0x1344001d	8

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	select Endpoints 1 – 15 only)					
ConfigData	Returns details of core configuration (Index register set to select Endpoint 0)	R	R	8'h??	0x1344001f	8
FifoSize	Returns the configured size of the selected Rx FIFO and TX FIFOs (Endpoints 1 – 15 only)					
FIFOx	FIFOs for Endpoints 0 – 15	RW	-	32'h??	0x13440020	32
DevCtl	OTG device control register	RW	RW	8'h80	0x13440060	8
MISC	Miscellaneous Register	RW	RW	8'h00	0x13440061	8
VControl	UTMI+ PHY Vendor registers	R	R	4'h?	0x13440068	4
Vstatus	UTMI+ PHY Vendor registers	R	R	8'h??	0x1344006a	8
HWVers	Hardware Version Number Register	R	R	16'h????	0x1344006c	16
EPInfo	Information about numbers of TX and Rx endpoints	R	R	8'h??	0x13440078	8
RAMInfo	Information about the width of the RAM and the number of DMA channels	R	R	8'h??	0x13440079	8
LinkInfo	Information about delays to be applied	RW	R	8'h5c	0x1344007a	8
VPLen	Duration of the VBus pulsing charge	RW	R	8'h3c	0x1344007b	8
HS_EOF1	Time buffer available on High-Speed transactions	RW	R	8'h80	0x1344007c	8
FS_EOF1	Time buffer available on Full-Speed transactions	RW	R	8'h77	0x1344007d	8
LS_EOF1	Time buffer available on Low-Speed transactions	RW	R	8'h72	0x1344007e	8
SoftRst	Soft reset	RW	R	8'h00	0x1344007f	8
TxFuncAddr	Transmit Endpoint *n* Function Address (Host Mode only)	RW	R	7'h00	0x13440080 +8*n	7
TxHubAddr	Transmit Endpoint *n* Hub Address (Host Mode only)	RW	R	8'h00	0x13440082 +8*n	8
TxHubPort	Transmit Endpoint *n* Hub Port (Host Mode only)	RW	R	7'h00	0x13440083 +8*n	7
RxFuncAddr	Receive Endpoint *n* Function Address (Host Mode only)	RW	R	7'h00	0x13440084 +8*n	7
RxHubAddr	Receive Endpoint *n* Hub Address (Host Mode only)	RW	R	8'h00	0x13440086 +8*n	8
RxHubPort	Receive Endpoint *n* Hub Port (Host Mode only)	RW	R	7'h00	0x13440087 +8*n	7

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DMA_INTR	DMA Interupt register	RW	S	8'h00	0x13440200	8
DMA_CNTL	DMA Control Register for DMA channel n (channel 1 thru 8)	RW	R	11'h00	0x13440204 +(n-1)*0x10	11
DMA_ADDR	DMA Address Register for DMA channel n (channel 1 thru 8)	RW	RW	32'h00000000	0x13440208 +(n-1)*0x10	32
DMA_COUNT	DMA Count Register for DMA channel n (channel 1 thru 8)	RW	RW	32'h00000000	0x1344020c +(n-1)*0x10	32
RqPktCount	Number of requested packets for Receive Endpoint *n* (Endpoints 1 – 15 only)	RW	RW	16'h0000	0x13440300 +4*n	16
RmtWkIntr	Usb remote wake up interrupt register	R	S	1'b0	0x13440398	1
RmtWkIntrE	Usb remote wake up interrupt register enable	RW	R	1'b0	0x1344039c	1
RxDPktBufDis	Double Packet Buffer Disable register for Rx Endpoints 1 to 15	RW	R	16'h0000	0x13440340	16
TxDPktBufDis	Double Packet Buffer Disable register for TX Endpoints 1 to 15	RW	R	16'h0000	0x13440342	16
C_T_UCH	This register sets the Chirp Timeout Timer	RW	-	16'h?	0x13440344	16
C_T_HSRTN	This register sets the delay from the end of High Speed resume signaling to enable UTM normal operating mode	RW	-	16'h?	0x13440346	16
C_T_HSBT	HS Timeout Adder	RW	R	4'h0	0x13440348	4

NOTE:

In the following bit descriptions:

'r' means that the bit is read only 'rw' means that the bit can be both read and written.

'set' means that the bit can only be written to set it 'r/set' means that the bit can be read or set but it can't be cleared.

'clear' means that the bit can only be written to clear it 'r/clear' means that the bit can be read or cleared but it can't be set.

'self-clearing' means the bit will be cleared automatically when the associated action has been executed.

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35.4 Common registers

35.4.1 FAddr

FAddr is an 8-bit register that should be written with the 7-bit address of the peripheral part of the transaction.

When the MUSBHDRC is being used in Peripheral mode (DevCtl.D2=0), this register should be written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

NOTE: Peripheral Mode Only!!

FAddr **0x13440000**

Bit	7	6	5	4	3	2	1	0
	Unused	FAddr						
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7	-	Unused. Always 0.	R	-
6:0	FAddr	The function address.	RW	R

35.4.2 Power

Power is an 8-bit register that is used for controlling Suspend and Resume signaling, and some basic operational aspects of the MUSBHDRC.

Power **0x13440001**

Bit	7	6	5	4	3	2	1	0
	ISO Update	Soft Conn	HS Enab	HS Mode	Reset	Resume	Suspend Mode	Enable SuspendM
RST	0	0	1	0	0	0	0	0

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Bits	Name	Description	CPU	USB
7	ISO Update	When set by the CPU, the MUSBHDRC will wait for an SOF token from the time TxPktRdy is set before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be sent. **NOTE:** *Only valid in Peripheral Mode. Also, this bit only affects endpoints performing Isochronous transfers.*	P: RW H: -	P: R H: -
6	Soft Conn	If Soft Connect/Disconnect feature is enabled, then the USB D+/D- lines are enabled when this bit is set by the CPU and tri-stated when this bit is cleared by the CPU. **NOTE:** *Only valid in Peripheral Mode.*	P: RW H: -	P: R H: -
5	HS Enab	When set by the CPU, the MUSBHDRC will negotiate for High-speed mode when the device is reset by the hub. If not set, the device will only operate in Full-speed mode.	P: RW H: RW	P: R H: R
4	HS Mode	When set, this read-only bit indicates High-speed mode successfully negotiated during USB reset. In Peripheral Mode, becomes valid when USB reset completes (as indicated by USB reset interrupt). In Host Mode, becomes valid when Reset bit is cleared. Remains valid for the duration of the session. **NOTE:** Allowance is made for Tiny-J signaling in determining the transfer speed to select.	P: R H: R	P: RW H: RW
3	Reset	This bit is set when Reset signaling is present on the bus. **NOTE:** This bit is Read/Write from the CPU inHost Mode but Read-Only in Peripheral Mode.	P: R H: RW	P: RW H: RW
2	Resume	Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In Host mode, this bit is also automatically set when Resume signaling from the target is detected while the MUSBHDRC is suspended.	P: RW H: RW	P: R H: R
1	Suspend Mode	In Host mode, this bit is set by the CPU to enter Suspend mode. In Peripheral mode, this bit is set on entry into Suspend mode. It is cleared when the CPU reads the interrupt register, or sets the Resume bit above.	P: R H: set	P: RW H: clr
0	Enable SuspendM	Set by the CPU to enable the SUSPENDM output.	P: RW H: RW	P: R H: R

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35.4.3 IntrTx

IntrTx is a 16-bit read-only register that indicates which interrupts are currently active for Endpoint 0 and the Tx Endpoints 1–15.

NOTE: Bits relating to endpoints that have not been configured will always return 0. Note also that all active interrupts are cleared when this register is read.

IntrTx **0x13440002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15Tx	EP14Tx	EP13Tx	EP12Tx	EP11Tx	EP10Tx	EP9Tx	EP8Tx	EP7Tx	EP6Tx	EP5Tx	EP4Tx	EP3Tx	EP2Tx	EP1Tx	EP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	EP15Tx	Tx Endpoint 15 interrupt.	R	Set
14	EP14Tx	Tx Endpoint 14 interrupt.	R	Set
13	EP13Tx	Tx Endpoint 13 interrupt.	R	Set
12	EP12Tx	Tx Endpoint 12 interrupt.	R	Set
11	EP11Tx	Tx Endpoint 11 interrupt.	R	Set
10	EP10Tx	Tx Endpoint 10 interrupt.	R	Set
9	EP9Tx	Tx Endpoint 9 interrupt.	R	Set
8	EP8Tx	Tx Endpoint 8 interrupt.	R	Set
7	EP7Tx	Tx Endpoint 7 interrupt.	R	Set
6	EP6Tx	Tx Endpoint 6 interrupt.	R	Set
5	EP5Tx	Tx Endpoint 5 interrupt.	R	Set
4	EP4Tx	Tx Endpoint 4 interrupt.	R	Set
3	EP3Tx	Tx Endpoint 3 interrupt.	R	Set
2	EP2Tx	Tx Endpoint 2 interrupt.	R	Set
1	EP1Tx	Tx Endpoint 1 interrupt.	R	Set
0	EP0	Tx Endpoint 0 interrupt.	R	Set

35.4.4 IntrRx

IntrRx is a 16-bit read-only register that indicates which of the interrupts for Rx Endpoints 1 – 15 are currently active.

NOTE: Bits relating to endpoints that have not been configured will always return 0. Note also that all active interrupts are cleared when this register is read.

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INTRRX 0x13040004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15Rx	EP14Rx	EP13Rx	EP12Rx	EP11Rx	EP10Rx	EP9Rx	EP8Rx	EP7Rx	EP6Rx	EP5Rx	EP4Rx	EP3Rx	EP2Rx	EP1Rx	-
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	EP15Rx	Rx Endpoint 15 interrupt.	R	Set
14	EP14Rx	Rx Endpoint 14 interrupt.	R	Set
13	EP13Rx	Rx Endpoint 13 interrupt.	R	Set
12	EP12Rx	Rx Endpoint 12 interrupt.	R	Set
11	EP11Rx	Rx Endpoint 11 interrupt.	R	Set
10	EP10Rx	Rx Endpoint 10 interrupt.	R	Set
9	EP9Rx	Rx Endpoint 9 interrupt.	R	Set
8	EP8Rx	Rx Endpoint 8 interrupt.	R	Set
7	EP7Rx	Rx Endpoint 7 interrupt.	R	Set
6	EP6Rx	Rx Endpoint 6 interrupt.	R	Set
5	EP5Rx	Rx Endpoint 5 interrupt.	R	Set
4	EP4Rx	Rx Endpoint 4 interrupt.	R	Set
3	EP3Rx	Rx Endpoint 3 interrupt.	R	Set
2	EP2Rx	Rx Endpoint 2 interrupt.	R	Set
1	EP1Rx	Rx Endpoint 1 interrupt.	R	Set
0	-	Unused, always returns 0.	R	R

35.4.5 IntrTxE

IntrTxE is a 16-bit register that provides interrupt enable bits for the interrupts in IntrTx. On reset, the bits corresponding to Endpoint 0 and the Tx endpoints included in the design are set to 1, while the remaining bits are set to 0.

NOTE: Bits relating to endpoints that have not been configured will always return 0.

IntrTxE 0x13440006

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15Tx	EP14Tx	EP13Tx	EP12Tx	EP11Tx	EP10Tx	EP9Tx	EP8Tx	EP7Tx	EP6Tx	EP5Tx	EP4Tx	EP3Tx	EP2Tx	EP1Tx	EP0
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	CPU	USB
15	EP15Tx	Tx Endpoint 15 interrupt enable.	RW	R

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14	EP14Tx	Tx Endpoint 14 interrupt enable.	RW	R
13	EP13Tx	Tx Endpoint 13 interrupt enable.	RW	R
12	EP12Tx	Tx Endpoint 12 interrupt enable.	RW	R
11	EP11Tx	Tx Endpoint 11 interrupt enable.	RW	R
10	EP10Tx	Tx Endpoint 10 interrupt enable.	RW	R
9	EP9Tx	Tx Endpoint 9 interrupt enable.	RW	R
8	EP8Tx	Tx Endpoint 8 interrupt enable.	RW	R
7	EP7Tx	Tx Endpoint 7 interrupt enable.	RW	R
6	EP6Tx	Tx Endpoint 6 interrupt enable.	RW	R
5	EP5Tx	Tx Endpoint 5 interrupt enable.	RW	R
4	EP4Tx	Tx Endpoint 4 interrupt enable.	RW	R
3	EP3Tx	Tx Endpoint 3 interrupt enable.	RW	R
2	EP2Tx	Tx Endpoint 2 interrupt enable.	RW	R
1	EP1Tx	Tx Endpoint 1 interrupt enable.	RW	R
0	EP0	Tx Endpoint 0 interrupt enable.	RW	R

35.4.6 IntrRxE

IntrRxE is a 16-bit register that provides interrupt enable bits for the interrupts in IntrRx. On reset, the bits corresponding to the Rx endpoints included in the design are set to 1, while the remaining bits are set to 0.

NOTE: Bits relating to endpoints that have not been configured will always return 0.

IntrRxE **0x13440008**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15Rx	EP14Rx	EP13Rx	EP12Rx	EP11Rx	EP10Rx	EP9Rx	EP8Rx	EP7Rx	EP6Rx	EP5Rx	EP4Rx	EP3Rx	EP2Rx	EP1Rx	-
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bits	Name	Description	CPU	USB
15	EP15Rx	Rx Endpoint 15 interrupt enable.	RW	R
14	EP14Rx	Rx Endpoint 14 interrupt enable.	RW	R
13	EP13Rx	Rx Endpoint 13 interrupt enable.	RW	R
12	EP12Rx	Rx Endpoint 12 interrupt enable.	RW	R
11	EP11Rx	Rx Endpoint 11 interrupt enable.	RW	R
10	EP10Rx	Rx Endpoint 10 interrupt enable.	RW	R
9	EP9Rx	Rx Endpoint 9 interrupt enable.	RW	R
8	EP8Rx	Rx Endpoint 8 interrupt enable.	RW	R
7	EP7Rx	Rx Endpoint 7 interrupt enable.	RW	R
6	EP6Rx	Rx Endpoint 6 interrupt enable.	RW	R

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5	EP5Rx	Rx Endpoint 5 interrupt enable.	RW	R
4	EP4Rx	Rx Endpoint 4 interrupt enable.	RW	R
3	EP3Rx	Rx Endpoint 3 interrupt enable.	RW	R
2	EP2Rx	Rx Endpoint 2 interrupt enable.	RW	R
1	EP1Rx	Rx Endpoint 1 interrupt enable.	RW	R
0	-	Unused, always returns 0.	R	R

35.4.7 IntrUSB

IntrUSB is an 8-bit read-only register that indicates which USB interrupts are currently active. All active interrupts will be cleared when this register is read.

IntrUSB 0x1344000a

Bit	7	6	5	4	3	2	1	0
	VBus Error	Sess Req	Discon	Conn	SOF	Reset/Babble	Resume	Suspend
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7	Vbus Error	Set when VBus drops below the VBus Valid threshold during a session. *Only valid when MUSBHDRC is 'A' device.*	R	Set
6	Sess Req	Set when Session Request signaling has been detected. *Only valid when MUSBHDRC is 'A' device.*	R	Set
5	Discon	Set in Host mode when a device disconnect is detected. Set in Peripheral mode when a session ends. *Valid at all transaction speeds.*	R	Set
4	Conn	Set when a device connection is detected. *Only valid in Host mode. Valid at all transaction speeds.*	R	Set
3	SOF	Set when a new frame starts.	R	Set
2	Reset	Set in Peripheral mode when Reset signaling is detected on the D2 e bus.	R	Set
	Babble	Set in Host mode when babble is detected.		
1	Resume	Set when Resume signaling is detected on the bus while the MUSBHDRC is in Suspend mode.	R	Set
0	Suspend	Set when Suspend signaling is detected on the bus. *Only valid in Peripheral mode.*	R	Set

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35.4.8 IntrUSBE

IntrUSBE is an 8-bit register that provides interrupt enable bits for each of the interrupts in IntrUSB.

IntrUSBE **0x1344000b**

Bit	7	6	5	4	3	2	1	0
	VBus Error	Sess Req	Discon	Conn	SOF	Reset/Babble	Resume	Suspend
RST	0	0	0	0	0	1	1	0

Bits	Name	Description	CPU	USB
7	Vbus Error	Interrupt enable.	RW	R
6	Sess Req	Interrupt enable.	RW	R
5	Discon	Interrupt enable.	RW	R
4	Conn	Interrupt enable.	RW	R
3	SOF	Interrupt enable.	RW	R
2	Reset Babble	Interrupt enable.	RW	R
1	Resume	Interrupt enable.	RW	R
0	Suspend	Interrupt enable.	RW	R

35.4.9 Frame

Frame is a 16-bit read-only register that holds the last received frame number.

Frame **0x1344000C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0					Frame Number										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15:11	-	Always 0.	R	W
10:0	Frame Number	Frame number.	R	W

35.4.10 Index

Each Tx endpoint and each Rx endpoint have their own set of control/status registers located between 100h – 1FFh. In addition one set of Tx control/status and one set of Rx control/status registers appear at 10h – 19h. Index is a 4-bit register that determines which endpoint control/status registers are accessed.

Before accessing an endpoint's control/status registers at 10h – 19h, the endpoint number should be

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written to the Index register to ensure that the correct control/status registers appear in the memory map.

Index					0x1344000e
Bit				3	2	1	0
				Selected Endpoint			
RST				0	0	0	0

Bits	Name	Description	CPU	USB
3:0	Selected Endpoint	Selected endpoint.	RW	R

35.4.11 TestMode

Testmode is an 8-bit register that is primarily used to put the MUSBHDRC into one of the four test modes for High-speed operation described in the USB 2.0 specification – in response to a SET FEATURE: TESTMODE command. It is not used in normal operation.

NOTE: Only one of Bits D0 – D6 should be set at any time.

TestMode								0x1344000f
Bit	7	6	5	4	3	2	1	0
	Force_Host	FIFO_Access(self-clr)	Force_FS	Force_HS	Test_Packet	Test_K	Test_J	Test_SE0_NAK
RST	0	0	0	0	0	0	0	0

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Bits	Name	Description	CPU	USB
7	Force_Host	The CPU sets this bit to instruct the core to enter Host mode when the Session bit is set, regardless of whether it is connected to any peripheral. The state of the CID input, HostDisconnect and LineState signals are ignored. The core will then remain in Host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set. While in this mode, the status of the HOSTDISCON signal from the PHY may be read from bit 7 of the DevCtl register. The operating speed is determined from the Force_HS and Force_FS bits as follows: <table><tr><th>Force_HS</th><th>Force_FS</th><th>Operating Speed</th></tr><tr><td>0</td><td>0</td><td>Low Speed</td></tr><tr><td>0</td><td>1</td><td>Full Speed</td></tr><tr><td>1</td><td>0</td><td>High Speed</td></tr><tr><td>1</td><td>1</td><td>Undefined</td></tr></table>	RW	R
6	FIFO_Access	The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically.	Set	R
5	Force_FS	The CPU sets this bit either in conjunction with bit 7 above or to force the MUSBHDRC into Full-speed mode when it receives a USB reset.	RW	R
4	Force_HS	The CPU sets this bit either in conjunction with bit 7 above or to force the MUSBHDRC into High-speed mode when it receives a USB reset.	RW	R
3	Test_Packet	*(High-speed mode)* The CPU sets this bit to enter the Test_Packet test mode. In this mode, the MUSBHDRC repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the *Universal Serial Bus Specification* Revision 2.0, Section 7.1.20 (and in the MUSBHDRC Programmer's Guide). **NOTE:** The test packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.	RW	R

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2	Test_K	*(High-speed mode)* The CPU sets this bit to enter the Test_K test mode. In this mode, the MUSBHDRC transmits a continuous K on the bus.	RW	R
1	Test_J	*(High-speed mode)* The CPU sets this bit to enter the Test_J test mode. In this mode, the MUSBHDRC transmits a continuous J on the bus.	RW	R
0	Test_SE0_NAK	*(High-speed mode)* The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the MUSBHDRC remains in High-speed mode but responds to any valid IN token with a NAK.	RW	R

35.4.12 DevCtl

DevCtl is an 8-bit register that is used to select whether the MUSBHDRC is operating in Peripheral mode or in Host mode, and for controlling and monitoring the USB VBus line.

DevCtl **0x13440060**

Bit	7	6	5	4	3	2	1	0
	B-Device	FSDev	LSDev	VBus[1]	VBus[0]	Host Mode	Host Req	Session
RST	1	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7	B-Device	This Read-only bit indicates whether the MUSBHDRC is operating as the 'A' device or the 'B' device. 0 => 'A' device; 1 => 'B' device. *Only valid while a session is in progress.* **NOTE:** If the core is in Force_Host mode (i.e. a session has been started with Testmode.D7 = 1), this bit will indicate the state of the HOSTDISCON input signal from the PHY.	R	RW

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6	FSDev	This Read-only bit is set when a full-speed or high-speed device has been detected being connected to the port. (High-speed devices are distinguished from full-speed by checking for high-speed chirps when the device is reset.) *Only valid in Host mode*.	R	RW
5	LSDev	This Read-only bit is set when a low-speed device has been detected being connected to the port. *Only valid in Host mode*.	R	RW
4:3	VBus	These Read-only bits encode the current VBus level as follows: D4 / D3 / Meaning 0 / 0 / Below SessionEnd 0 / 1 / Above SessionEnd, below AValid 1 / 0 / Above AValid, below VBusValid 1 / 1 / Above VBusValid	R	RW
2	Host Mode	This Read-only bit is set when the MUSBHDRC is acting as a Host.	R	RW
1	Host Req	When set, the MUSBHDRC will initiate the Host Negotiation when Suspend mode is entered. It is cleared when Host Negotiation is completed. See Section 15. *('B' device only)*	RW	R/clr
0	Session	*When operating as an 'A' device,* this bit is set or cleared by the CPU to start or end a session. *When operating as a 'B' device,* this bit is set/cleared by the MUSBHDRC when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol. When the MUSBHDRC is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect.	RW	RW

35.5 Indexed Register

NOTE: The action of the following registers when the selected endpoint has not been configured is undefined.

35.5.1 CSR0

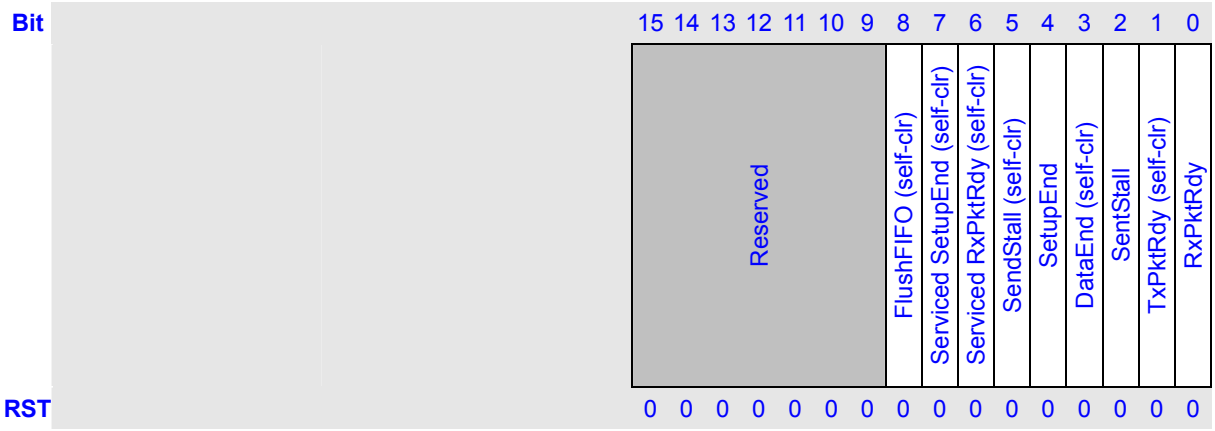
CSR0 is a 16-bit register that provides control and status bits for Endpoint 0.

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NOTE: The interpretation of the register depends on whether the MUSBHDRC is acting as a peripheral or as a host. Users should also be aware that the value returned when the register is read reflects the status attained e.g. as a result of writing to the register. (with the Index register set to 0)

Peripheral Mode:

CSR0 **0x13440012**



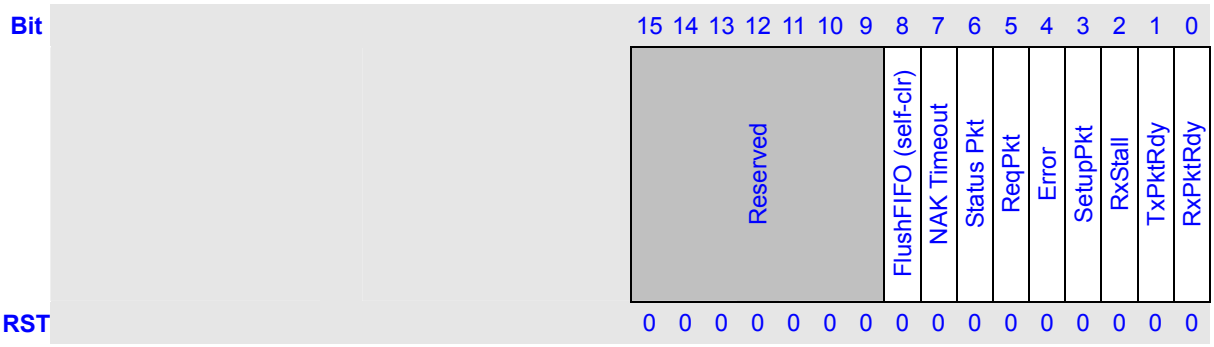
Bits	Name	Description	CPU	USB
15:9	Reserved	*Unused. Return 0 when read.*	R	R
8	FlushFIFO	The CPU writes a 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. **NOTE:** FlushFIFO has no effect unless TxPktRdy/RxPktRdy is set.	Set	R
7	Serviced SetupEnd	The CPU writes a 1 to this bit to clear the SetupEnd bit. It is cleared automatically.	Set	R
6	Serviced RxPKtRdy	The CPU writes a 1 to this bit to clear the RxPktRdy bit. It is cleared automatically.	Set	R
5	SendStall	The CPU writes a 1 to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically.	Set	R
4	SetupEnd	This bit will be set when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing a 1 to the ServicedSetupEnd bit.	R	Set

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3	DataEnd	The CPU sets this bit: 1 When setting TxPktRdy for the last data packet. 2 When clearing RxPktRdy after unloading the last data packet. 3 When setting TxPktRdy for a zero length data packet. It is cleared automatically.	Set	R
2	SentStall	This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.	R/clr	Set
1	TxPKtRdy	The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).	R/set	R
0	RxPKtRdy	This bit is set when a data packet has been received. An interrupt is generated when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.	R	Set

Host Mode:

CSR0 **0x13440012**



Bits	Name	Description	CPU	USB
15:9	Reserved	*Unused. Return 0 when read.*	R	R
8	FlushFIFO	The CPU writes a 1 to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. **NOTE:** FlushFIFO has no effect unless TxPktRdy/RxPktRdy is set.	Set	R

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7	NAK Timeout	This bit will be set when Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLimit0 register. The CPU should clear this bit to allow the endpoint to continue.	R/clr	Set
6	StatusPkt	The CPU sets this bit at the same time as the TxPktRdy or ReqPkt bit is set, to perform a status stage transaction. Setting this bit ensures that the data toggle is set to 1 so that a DATA1 packet is used for the Status Stage transaction.	RW	R
5	ReqPkt	The CPU sets this bit to request an IN transaction. It is cleared when RxPktRdy is set.	RW	RW
4	Error	This bit will be set when three attempts have been made to perform a transaction with no response from the peripheral. The CPU should clear this bit. An interrupt is generated when this bit is set.	R	Set
3	SetupPkt	The CPU sets this bit, at the same time as the TxPktRdy bit is set, to send a SETUP token instead of an OUT token for the transaction.	RW	RW
2	RxStall	This bit is set when a STALL handshake is received. The CPU should clear this bit.	R/clr	Set
1	TxPktRdy	The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when the data packet has been transmitted. An interrupt is generated (if enabled) when the bit is cleared.	R/set	Clr
0	RxPktRdy	This bit is set when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU should clear this bit when the packet has been read from the FIFO.	R/clr	RW

35.5.2 Count0

Count0 is a 7-bit read-only register that indicates the number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while RxPktRdy (CSR0.D0) is set.

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Count0 0x13440018

Bit	6	5	4	3	2	1	0
	Endpoint 0 Rx Count						
RST	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
6:0	Endpoint 0 Rx Count	Number of received data bytes in the endpoint 0 FIFO.	R	W

35.5.3 ConfigData

ConfigData is an 8-bit Read-Only register that returns information about the selected core configuration.

ConfigData 0x1344001f

Bit	7	6	5	4	3	2	1	0
	MPRxE	MPTxE	BigEndian	HBRxE	HBTxE	DynFIFOSizing	SoftConE	UTMI Data Width
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	CPU	USB
7	MPRxE	When set to ‘1’, automatic amalgamation of bulk packets is selected.	R	R
6	MPTxE	When set to ‘1’, automatic splitting of bulk packets is selected.	R	R
5	BigEndian	When set to ‘1’ indicates Big Endian ordering is selected.	R	R
4	HBRxE	When set to ‘1’ indicates High-bandwidth Rx ISO Endpoint Support selected.	R	R
3	HBTxE	When set to ‘1’ indicates High-bandwidth Tx ISO Endpoint Support selected.	R	R
2	DynFIFOSizing	When set to ‘1’ indicates Dynamic FIFO Sizing option selected.	R	R
1	SoftConE	When set to ‘1’ indicates Soft Connect/Disconnect option selected.	R	R
0	UTMI Data Width	Indicates selected UTMI+ data width. 0 => 8 bits; 1 => 16 bits.	R	R

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35.5.4 NakLimit0 (Host Mode Only)

NAKLimit0 is a 5-bit register that sets the number of frames/microframes (High-Speed transfers) after which Endpoint 0 should timeout on receiving a stream of NAK responses. (Equivalent settings for other endpoints can be made through their TxInterval and RxInterval registers.
The number of frames/microframes selected is $2_{(m-1)}$ (where *m* is the value set in the register, valid values 2 – 16). If the host receives NAK responses from the target for more frames than the number represented by the Limit set in this register, the endpoint will be halted.

NOTE: A value of 0 or 1 disables the NAK timeout function.

NakLimit0 **0x1344001b**

Bit	4	3	2	1	0
	Endpoint 0 NAK Limit				
RST	0	0	0	0	0

Bits	Name	Description	CPU	USB
4:0	Endpoint 0 NAK Limit	Endpoint 0 NAK limit.	RW	R

35.5.5 TxMaxP

The TxMaxP register defines the maximum amount of data that can be transferred through the selected Tx endpoint in a single operation. There is a TxMaxP register for each Tx endpoint (except Endpoint 0).
Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full speed and High-speed operations.

Where the option of High-bandwidth Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier *m* which is equal to one more than the value recorded.

In the case of Bulk endpoints with the packet splitting option enabled, the multiplier *m* can be up to 32 and defines the maximum number of 'USB' packets (i.e. packets for transmission over the USB) of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. (If the packet splitting option is not enabled, D15–D13 is not implemented and D12–D11 (if included) is ignored.) **NOTE:** The data packet is required to be an exact multiple of the payload specified by bits 10:0, which is itself required to be either 8, 16, 32, 64 or (in the case of High Speed transfers) 512 bytes.

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For Isochronous/Interrupt endpoints operating in High-Speed mode and with the High-bandwidth option enabled, *m* may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-zero, the MUSBHDRC will automatically split any data packet written to the FIFO into up to 2 or 3 'USB' packets, each containing the specified payload (or less). The maximum payload for each transaction is 1024 bytes, so this allows up to 3072 bytes to be transmitted in each microframe. (For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.)

The value written to bits 10:0 (multiplied by *m* in the case of high-bandwidth Isochronous/Interrupt transfers) must match the value given in the *wMaxPacketSize* field of the Standard Endpoint Descriptor for the associated endpoint (see *USB Specification* Revision 2.0, Chapter 9). A mismatch could cause unexpected results. The total amount of data represented by the value written to this register (specified payload × *m*) must not exceed the FIFO size for the Tx endpoint, and should not exceed half the FIFO size if double-buffering is required.

If this register is changed after packets have been sent from the endpoint, the Tx endpoint FIFO should be completely flushed (using the FlushFIFO bit in TxCSR) after writing the new value to this register.

TxMaxP **0x13440010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	m-1					Maximum Payload/transaction										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15/12:11	m-1	Multiplier.	RW	R
10:0	Maximum Payload/transaction	Maximum payload transmitted in a single transaction.	RW	R

35.5.6 TxCSR

TxCSR is a 16-bit register that provides control and status bits for transfers through the currently-selected Tx endpoint. There is a TxCSR register for each configured Tx endpoint (not including Endpoint 0).

NOTE: The interpretation of the register depends on whether the MUSBHDRC is acting as a peripheral or as a host. Users should also be aware that the value returned when the register is read reflects the status attained e.g. as a result of writing to the register.

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Peripheral Mode

TxCSR **0x13440012**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AutoSet	ISO	Mode	DMAReqEnab	FrcDataTog	DMAReqMode	Reserved		IncompTx	ClrDataTog	SentStall	SendStall	FlushFIFO(sefl-clr)	UnderRun	FIFO NotEmpty	TxPktRdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	AutoSet	If the CPU sets this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. **NOTE:** *Should not be set for high-bandwidth Isochronous endpoints.*	RW	R
14	ISO	The CPU sets this bit to enable the Tx endpoint for Isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. **NOTE:** *This bit only has any effect in Peripheral mode. In Host mode,* it always returns zero.	RW	R
13	Mode	The CPU sets this bit to enable the endpoint direction as Tx, and clears the bit to enable it as Rx. **NOTE:** This bit *only* has any effect where the same endpoint FIFO is used for both Tx and Rx transactions.	RW	R
12	DMAReqEnab	The CPU sets this bit to enable the DMA request for the Tx endpoint.	RW	R
11	FrcDataTog	The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.	RW	R

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10	DMAReqMode	The CPU sets this bit to select DMA. Request Mode 1 and clears it to select DMA. Request Mode 0. **NOTE:** This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared.	RW	R
9:8	Reserved	Unused, always return 0.	R	R
7	InCompTx	When the endpoint is being used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. **NOTE:** *In anything other than a high-bandwidth transfer, this bit will always return 0.*	R/clr	Set
6	ClrDataTog	The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.	Set	R/clr
5	SentStall	This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared (see below). The CPU should clear this bit.	R/clr	Set
4	SendStall	The CPU writes a 1 to this bit to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. **NOTE:** *This bit has no effect where the endpoint is being used for Isochronous transfers.*	RW	R
3	FlushFIFO	The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. **NOTE:** FlushFIFO has no effect unless TxPktRdy is set. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.	Set	R
2	UnderRun	The USB sets this bit if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit.	R/clr	Set

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1	FIFONotEmpty	The USB sets this bit when there is at least 1 packet in the Tx FIFO.	R/clr	Set
0	TxPktRdy	The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (but no interrupt is generated) prior to loading a second packet into a double-buffered FIFO.	R/set	Clr

Host Mode:

TxCSR **0x13440012**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AutoSet	Reserved	Mode	DMAReqEnab	FrcDataTog	DMAReqMode	Reserved		NAK Timeout	ClrDataTog	RxStall	Reserved	FlushFIFO (self-lcr)	Error	FIFONotEmpty	TxPktRdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	AutoSet	If the CPU sets this bit, TxPktRdy will be automatically set when a packet of the maximum packet size (TxMaxP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. **NOTE:** *Should not be set for high-bandwidth Isochronous endpoints.*	RW	R
14	Reserved	Unused, always returns zero.	RW	R
13	Mode	The CPU sets this bit to enable the endpoint direction as Tx, and clears it to enable the endpoint direction as Rx. **NOTE:** *This bit only has any effect where the same endpoint FIFO is used for both Tx and Rx transactions.*	RW	R
12	DMAReqEnab	The CPU sets this bit to enable the DMA request for the Tx endpoint.	RW	R

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11	FrcDataTog	The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.	RW	R
10	DMAReqMode	The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **NOTE:** *This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared*.	RW	R
9:8	Reserved	Unused, always returns 0.	R	R
7	NAKTimeout	This bit will be set when the Tx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register. The CPU should clear this bit to allow the endpoint to continue. **NOTE:** *Valid only for Bulk endpoints.*	R/clr	Set
6	ClrDataTog	The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.	Set	R/clr
5	RxStall	This bit is set when a STALL handshake is received. When this bit is set, any DMA request that is in progress is stopped, the FIFO is completely flushed and the TxPktRdy bit is cleared (see below). The CPU should clear this bit.	R/clr	Set
4	Reserved	Unused, always returns 0.	R	R
3	FlushFIFO	The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. **NOTE:** FlushFIFO has no effect unless TxPktRdy is set. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.	Set	R

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2	Error	The USB sets this bit when 3 attempts have been made to send a packet and no handshake packet has been received. When the bit is set, an interrupt is generated, TxPktRdy is cleared and the FIFO is completely flushed. The CPU should clear this bit. *Valid only when the endpoint is operating in Bulk or Interrupt mode.*	R/clr	RW
1	FIFONotEmpty	The USB sets this bit when there is at least 1 packet in the Tx FIFO.	R/clr	Set
0	TxPktRdy	The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared (but no interrupt is generated) prior to loading a second packet into a double-buffered FIFO.	R/set	Clr

35.5.7 RxMaxP

The RxMaxP register defines the maximum amount of data that can be transferred through the selected Rx endpoint in a single operation. There is a RxMaxP register for each Rx endpoint (except Endpoint 0).

Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full speed and High-speed operations.

Where the option of High-bandwidth Isochronous/Interrupt endpoints or of combining Bulk packets has been taken when the core is configured, the register includes either 2 or 5 further bits that define a multiplier *m* which is equal to one more than the value recorded.

For Bulk endpoints with the packet combining option enabled, the multiplier *m* can be up to 32 and defines the number of USB packets of the specified payload which are to be combined into a single data packet within the FIFO. (If the packet splitting option is not enabled, D15–D13 is not implemented and D12–D11 (if included) is ignored.)

For Isochronous/Interrupt endpoints operating in High-Speed mode and with the High-bandwidth option enabled, *m* may only be either 2 or 3 (corresponding to bit 11 set or bit 12 set, respectively) and it specifies the maximum number of such transactions that can take place in a single microframe. If either bit 11 or bit 12 is non-zero, the MUSBHDRC will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. The maximum payload for

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each transaction is 1024 bytes, so this allows up to 3072 bytes to be received in each microframe. (For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bits 11 and 12 are ignored.)

The value written to bits 10:0 (multiplied by *m* in the case of high-bandwidth Isochronous/Interrupt transfers) must match the value given in the *wMaxPacketSize* field of the Standard Endpoint Descriptor for the associated endpoint (see *USB Specification* Revision 2.0, Chapter 9). A mismatch could cause unexpected results.

The total amount of data represented by the value written to this register (specified payload × *m*) must not exceed the FIFO size for the OUT endpoint, and should not exceed half the FIFO size if double-buffering is required.

RxMaxP **0x13440014**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	m-1					Maximum Payload/transaction										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15/12:11	m-1	Multiplier.	RW	R
10:0	Maximum Payload/transaction	Maximum payload transmitted in a single transaction.	RW	R

35.5.8 RxCSR

RxCSR is an 16-bit register that provides control and status bits for transfers through the currently-selected Rx endpoint. There is an RxCSR register for each configured Rx endpoint (not including Endpoint 0).

NOTE: The interpretation of the register depends on whether the MUSBHDRC is acting as a peripheral or as a host. Users should also be aware that the value returned when the register is read reflects the status attained e.g. as a result of writing to the register.

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Peripheral Mode:

RxCSR **0x13440016**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AutoClear	ISO	DMAReqEnab	DisNyet	DMAReqMode	Reserved		IncompRx	ClrDataTog	SentStall	SendStall	FlushFIFO(sefl-clr)	DataError	OverRun	FIFOFull (self-clr)	RxPktRdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	AutoClear	If the CPU sets this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the Rx FIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. **NOTE:** *Should not be set for highbandwidth* Isochronous endpoints.	RW	R
14	ISO	The CPU sets this bit to enable the Rx endpoint for Isochronous transfers, and clears it to enable the Rx endpoint for Bulk/Interrupt transfers.	RW	R
13	DMAReqEnab	The CPU sets this bit to enable the DMA request for the Rx endpoint.	RW	R
12	DisNyet	The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. **NOTE:** *This bit only has any effect in High-speed mode, in which mode it should be set for all Interrupt endpoints.*	RW	R
11	DMAReqMode	The CPU sets this bit to select DMA. Request Mode 1 and clears it to select DMA. Request Mode 0.	RW	R
10:9	Reserved	Unused, always return zero.	R	R

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8	IncompRx	This bit is set in a high-bandwidth Isochronous transfer if the packet in the Rx FIFO is incomplete because parts of the data were not received. It is cleared when RxPktRdy is cleared. **NOTE:** *In anything* other than a high-bandwidth Isochronous transfer, this bit will always return 0.	R	Set
7	ClrDataTog	The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.	R	R/clr
6	SentStall	This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.	R/clr	Set
5	SendStall	The CPU writes a 1 to this bit to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. **NOTE:** *This bit has no effect where the endpoint is being used for Isochronous transfers.*	RW	R
4	FlushFIFO	The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. **NOTE:** FlushFIFO has no effect unless RxPktRdy is set. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.	Set	R
3	DataError	This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared. **NOTE:** *This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.*	R	Set
2	OverRun	This bit is set if an OUT packet cannot be loaded into the Rx FIFO. The CPU should clear this bit. **NOTE:** *This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.*	R/clr	Set
1	FIFOFull	This bit is set when no more packets can be loaded into the Rx FIFO.	R	Set

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0	RxPktRdy	This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set.	R/clr	Set

Host Mode:

RxCSR **0x13440016**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AutoClear	AutoReq	DMAReqEnab	DisNyet	DMAReqMode	Reserved		IncompRx	ClrDataTog	RxStall	ReqPkt	FlushFIFO(sefl-clr)	DataError/NAKTimeout	Error	FIFOFull (self-clr)	RxPktRdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	AutoClear	If the CPU sets this bit then the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the Rx FIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. **NOTE:** *Should not be set for highbandwidth Isochronous endpoints.*	RW	R
14	AutoReq	If the CPU sets this bit, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared.	RW	R
13	DMAReqEnab	The CPU sets this bit to enable the DMA request for the Rx endpoint.	RW	R
12	DisNyet	The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. **NOTE:** *This bit only has any effect in High-speed mode, in which mode it should be set for all Interrupt endpoints.*	RW	R
11	DMAReqMode	The CPU sets this bit to select DMA. Request Mode 1 and clears it to select DMA. Request Mode 0.	RW	R

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10:9	Reserved	Unused, always return 0.	R	R
8	IncompRx	This bit will be set in a high-bandwidth Isochronous transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared. **NOTE:** *If USB protocols are followed correctly, this bit should never be set. The bit becoming set indicates a failure of the associated Peripheral device to behave correctly. (In anything other than a high-bandwidth Isochronous transfer, this bit will always return 0.)*	R	Set
7	ClrDataTog	The CPU writes a 1 to this bit to reset the endpoint data toggle to 0.	Set	R/clr
6	RxStall	When a STALL handshake is received, this bit is set and an interrupt is generated. The CPU should clear this bit.	R/clr	Set
5	ReqPkt	The CPU writes a 1 to this bit to request an IN transaction. It is cleared when RxPktRdy is set.	RW	RW
4	FlushFIFO	The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. **NOTE:** FlushFIFO has no effect unless RxPktRdy is set. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.	Set	R
3	DataError/NAKTimeout	When operating in ISO mode, this bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared. In Bulk mode, this bit will be set when the Rx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register. The CPU should clear this bit to allow the endpoint to continue.	R/clr	Set

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2	Error	The USB sets this bit when 3 attempts have been made to receive a packet and no data packet has been received. The CPU should clear this bit. An interrupt is generated when the bit is set. **NOTE:** *This bit is only valid when the Tx endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.*	R/clr	Set
1	FIFOFull	This bit is set when no more packets can be loaded into the Rx FIFO.	R	Set
0	RxPktRdy	This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set.	R/clr	Set

35.5.9 RxCount

RxCount is a 13-bit read-only register that holds the number of received data bytes in the packet in the Rx FIFO.

NOTE: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (RxCSR.D0) is set.

RxCount **0x13440018**

Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
	Endpoint Rx Count												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
12:0	Endpoint Rx Count	Number of received data bytes in the packet in the Rx FIFO.	R	W

35.5.10 TxType (Host Mode Only)

TxType is a 6-bit register that should be written with the endpoint number to be targeted by the endpoint in the lower 4 bits, and the transaction protocol to use for the currently-selected Tx endpoint in the upper 2 bits. There is a TxType register for each configured Tx endpoint (except Endpoint 0).

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TxType 0x1344001a

Bit	5	4	3	2	1	0
	Protocol		Target Endpoint Number			
RST	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
5:4	Protocol	The CPU should set this to select the required protocol for the Tx endpoint. 00: Illegal 01: Isochronous 10: Bulk 11: Interrupt	RW	R
3:0	Target Endpoint Number	The CPU should set this value to the endpoint number contained in the Tx endpoint descriptor returned to the MUSBHDRC during device enumeration.	RW	R

35.5.11 TxInterval (Host Mode Only)

TxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Tx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured Tx endpoint (except Endpoint 0).

In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	LS or FS	1-255	Polling interval is *m* frames
	HS	1-16	Polling interval is $2^{(m-1)}$ microframes
Isochronous	FS or HS	1-16	Polling interval is $2^{(m-1)}$ frames/microframes
Bulk	FS or HS	2-16	NAK Limit is $2^{(m-1)}$ frames/microframes **NOTE:** A value of 0 or 1 disables the NAK timeout function.

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TxInterval 0x1344001b

Bit	7	6	5	4	3	2	1	0
	Tx Polling Interval/ NAK Limit (m)							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7:0	Tx Polling Interval/NAK Limit	For interrupt and isochronous transfers, defines the polling interval for the currently selected Tx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses.	RW	R

35.5.12 RxType (Host Mode Only)

RxType is a 6-bit register that should be written with the endpoint number to be targeted by the endpoint in the lower 4 bits, and the transaction protocol to use for the currently-selected Rx endpoint in the upper 2 bits. There is an RxType register for each configured Rx endpoint (except Endpoint 0).

RxType 0x1344001c

Bit	5	4	3	2	1	0
	Protocol		Target Endpoint Number			
RST	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
5:4	Protocol	The CPU should set this to select the required protocol for the Rx endpoint. 00: Illegal 01: Isochronous 10: Bulk 11: Interrupt	RW	R
3:0	Target Endpoint Number	The CPU should set this value to the endpoint number contained in the Rx endpoint descriptor returned to the MUSBHDRC during device enumeration.	RW	R

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35.5.13 RxInterval

RxInterval is an 8-bit register that, for Interrupt and Isochronous transfers, defines the polling interval for the currently-selected Rx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured Rx endpoint (except Endpoint 0). In each case the value that is set defines a number of frames/microframes (High Speed transfers), as follows:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	LS or FS	1-255	Polling interval is *m* frames
	HS	1-16	Polling interval is $2^{(m-1)}$ microframes
Isochronous	FS or HS	1-16	Polling interval is $2^{(m-1)}$ frames/microframes
Bulk	FS or HS	2-16	NAK Limit is $2^{(m-1)}$ frames/microframes **NOTE:** A value of 0 or 1 disables the NAK timeout function.

RxInterval **0x1344001d**

Bit	7	6	5	4	3	2	1	0
	Rx Polling Interval/ NAK Limit (m)							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7:0	Rx Polling Interval/NAK Limit	For interrupt and isochronous transfers, defines the polling interval for the currently selected Tx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses.	RW	R

35.5.14 FifoSize

FIFOSize is an 8-bit Read-Only register that returns the sizes of the FIFOs associated with the selected additional Tx/Rx endpoints. The lower nibble encodes the size of the selected Tx endpoint FIFO; the upper nibble encodes the size of the selected Rx endpoint FIFO. Values of 3 – 13 correspond to a FIFO size of 2^n bytes (8 – 8192 bytes). If an endpoint has not been configured, a value of 0 will be displayed. Where the Tx and Rx endpoints share the same FIFO, the Rx FIFO size will be encoded as 0xF.

NOTE: The register only has this interpretation when the Index register is set to select one of Endpoints 1 – 15 and Dynamic Sizing is not selected. It has a special interpretation when the Index register is set to select Endpoint 0 (see Section 5.3.3), while the result returned is not

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valid where Dynamic FIFO sizing is used. (Index register set to select Endpoints 1 – 15 only)

FifoSize 0x1344001f

Bit	7	6	5	4	3	2	1	0
	Rx FIFO Size				Tx FIFO Size			
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	CPU	USB
7:4	Rx FIFO Size	the sizes of the FIFOs associated with the selected additional Rx endpoints.	R	R
3:0	Tx FIFO Size	the sizes of the FIFOs associated with the selected additional Tx endpoints.	R	R

35.5.15 FIFOx

This address range provides 16 addresses for CPU access to the FIFOs for each endpoint. Writing to these addresses loads data into the TxFIFO for the corresponding endpoint. Reading from these addresses unloads data from the RxFIFO for the corresponding endpoint.

The address range is 20h – 5Fh and the FIFOs are located on 32-bit double-word boundaries (Endpoint 0 at 20h, Endpoint 1 at 24h ... Endpoint 15 at 5Ch).

35.6 Additional Multipoint Control / Status Registers

The following subsections detail additional control and status registers that are only valid when the multipoint option is enabled in the configuration GUI. If the multipoint option is not enabled these reregisters should not be accessed.

35.6.1 TxFuncAddr / RxFuncAddr

NOTE: REQUIRED IN HOST MODE!

TxFuncAddr and RxFuncAddr are 7-bit read/write registers that record the address of the target function that is to be accessed through the associated endpoint (EP*n*). TxFuncAddr needs to be defined for each TX endpoint that is used; RxFuncAddr needs to be defined for each Rx endpoint that is used.

NOTE: TxFuncAddr must be defined for Endpoint 0. The RxFuncAddr register does not exist on EP0.

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TxFuncAddr/RxFuncAddr								0x13440080+8*n / 0x13440084+8*n
Bit		6	5	4	3	2	1	0
		Addr of Target Function						
RST		0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
6:0	Addr of Target Function	read/write registers that record the address of the target function that is to be accessed through the associated endpoint.	RW	R

35.6.2 TxHubAddr/RxHubAddr

NOTE: RELEVANT IN HOST MODE ONLY!

TxHubAddr and RxHubAddr are 8-bit read/write registers which, like TxHubPort and RxHubPort, only need to be written where a full- or low-speed device is connected to TX/Rx Endpoint EP*n* via a high-speed USB 2.0 hub which carries out the necessary transaction translation to convert between high-speed transmission and full-/low-speed transmission. In such circumstances:

- the lower 7 bits should record the address of this USB 2.0 hub.
- the top bit should record whether the hub has multiple transaction translators (set to '0' if single transaction translator; set to '1' if multiple transaction translators).

NOTE: If Endpoint 0 is connected to a hub, then TxHubAddr must be defined for EP0. The RxHubAddr register does not exist on EP0.

TxHubAddr/RxHubAddr								0x13440082+8*n / 0x13440086+8*n
Bit	7	6	5	4	3	2	1	0
	Multi-Translators	HubAddr						
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7	Multi-Translators	0: single transaction translator 1: multiple transaction translators	RW	R
6:0	HubAddr	Hub Address.	RW	R

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35.6.3 TxHubPort / RxHubPort

NOTE: RELEVANT IN HOST MODE ONLY!

TxHubPort and RxHubPort only need to be written where a full- or low-speed device is connected to TX/Rx Endpoint EP*n* via a high-speed USB 2.0 hub which carries out the necessary transaction translation. In such circumstances, these 7-bit read/write registers need to be used to record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed.

NOTE: If Endpoint 0 is connected to a hub, then TxHubPort must be defined. The RxHubPort register does not exist on EP0.

TxHubPort/RxHubPort **0x13440083+8*n / 0x13440087+8*n**

Bit	6	5	4	3	2	1	0
	Hub Port						
RST	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
6:0	Hub Port	record the port of that USB 2.0 hub through which the target associated with the endpoint is accessed.	RW	R

35.7 Additional Control/Status Registers

35.7.1 VControl

NOTE: WRITE ONLY!

VControl is a UTMI+ PHY Vendor register that may optionally be included in the core when the core is configured. Its size is also configurable and may be up to 32 bits. The structure of the register is up to the system designer, though users should note that the UTMI+ specification defines a 4-bit VControl register.

Vcontrol **0x13440068**

Bit	3	2	1	0
	Vcontrol			
RST	?	?	?	?

Bits	Name	Description	CPU	USB
3:0	VControl	UTMI+ PHY Vendor registers.	RW	-

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35.7.2 VStatus

NOTE: READ ONLY!

VStatus is a UTMI+ PHY Vendor register that may optionally be included in the core when the core is configured. Its size is also configurable and may be up to 32 bits. The structure of the register is up to the system designer, though users should note that the UTMI+ specification defines an 8-bit VStatus register.

VStatus									0x1344006b
Bit									7 6 5 4 3 2 1 0
									VStatus
RST									? ? ? ? ? ? ? ?

Bits	Name	Description	CPU	USB
7:0	VStatus	UTMI+ PHY Vendor registers.	RW	-

35.7.3 Hwvers

HWVers register is a 16-bit read-only register that returns information about the version of the RTL from which the core hardware was generated, in particular the RTL version number (v*xx.yyy*).

Hwvers															0x1344006c
Bit															15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
															RC xx yyy
RST															? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?

Bits	Name	Description	CPU	USB
15	RC	Set to '1' if RTL used from a Release Candidate rather than from a full release of the core.	R	R
14:10	xx	Major Version Number. (Range 0 – 31)	R	R
9:0	yyy	Minor Version Number. (Range 0 – 999)	R	R

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35.8 Additional Configuration Registers

35.8.1 EPInfo

This 8-bit read-only register allows read-back of the number of TX and Rx endpoints included in the design.

EPInfo **0x13440078**

	7	6	5	4	3	2	1	0
	RxEdps				TxEdps			
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	CPU	USB
7:4	RxEdps	The number of Rx endpoints implemented in the design.	R	R
3:0	TxEdps	The number of TX endpoints implemented in the design.	R	R

35.8.2 RAMInfo

This 8-bit read-only register provides information about the width of the RAM.

RAMInfo **0x13440079**

Bit	7	6	5	4	3	2	1	0
	DMAChans				RAMBits			
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	CPU	USB
7:4	DMAChans	The number of DMA channels implemented in the design.	R	R
3:0	RAMBits	The width of the RAM address bus.	R	R

35.8.3 LinkInfo

This 8-bit register allows some delays to be specified.

LinkInfo **0x1344007a**

Bit	7	6	5	4	3	2	1	0
	WTCon				WTID			
	0	1	0	1	1	1	0	0

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Bits	Name	Description	CPU	USB
7:4	WTCon	Sets the wait to be applied to allow for the user's connect/disconnect filter in units of 533.3ns. (The default setting corresponds to 2.667μs)	RW	R
3:0	WTID	Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. (The default setting corresponds to 52.43ms)	RW	R

35.8.4 VPLen

This 8-bit register sets the duration of the VBus pulsing charge.

VPlen **0x1344007b**

Bit	7	6	5	4	3	2	1	0
	VPLen							
RST	0	0	1	1	1	1	0	0

Bits	Name	Description	CPU	USB
7:0	VPLen	Sets the duration of the VBus pulsing charge in units of 546.1 μs. (The default setting corresponds to 32.77ms)	RW	R

35.8.5 HS_EOF1

This 8-bit register sets the minimum time gap that is to be allowed between the start of the last transaction and the EOF for High-speed transactions.

HS_EOF1 **0x1344007c**

Bit	7	6	5	4	3	2	1	0
	HS_EOF1							
RST	1	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7:0	HS_EOF1	Sets for High-speed transactions the time before EOF to stop beginning new transactions, in units of 133.3ns. (The default setting corresponds to 17.07μs)	RW	R

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35.8.6 FS_EOF1

This 8-bit register sets the minimum time gap that is to be allowed between the start of the last transaction and the EOF for Full-speed transactions.

FS_EOF1 0x1344007d

Bit	7	6	5	4	3	2	1	0
	FS_EOF1							
RST	0	1	1	1	0	1	1	1

Bits	Name	Description	CPU	USB
7:0	FS_EOF1	Sets for Full-speed transactions the time before EOF to stop beginning new transactions, in units of 533.3ns. (The default setting corresponds to 63.46μs)	RW	R

35.8.7 LS_EOF1

This 8-bit register sets the minimum time gap that is to be allowed between the start of the last transaction and the EOF for Low-speed transactions.

LS_EOF1 0x1344007e

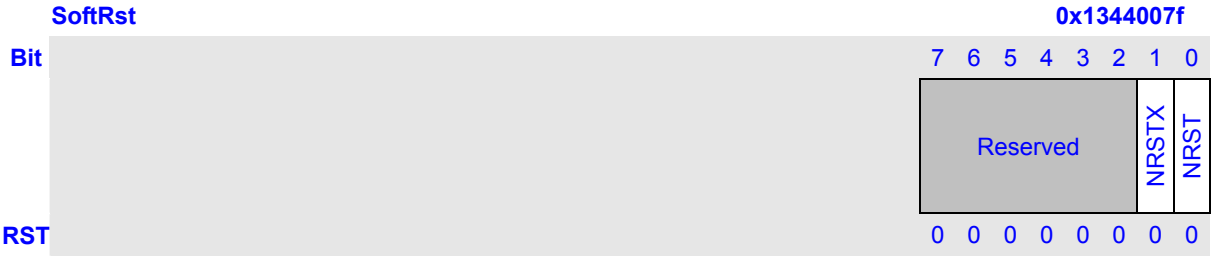
Bit	7	6	5	4	3	2	1	0
	LS_EOF1							
RST	0	1	1	1	0	0	1	0

Bits	Name	Description	CPU	USB
7:0	LS_EOF1	Sets for Low-speed transactions the time before EOF to stop beginning new transactions, in units of 1.067μs. (The default setting corresponds to 121.6μs)	RW	R

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35.8.8 SoftRst

This 8-bit register will assert LOW the output reset signals NRSTO and NRSTOX. This register is self clearing and will be reset by the input NRST.



Bits	Name	Description	CPU	USB
7:2	reserved	Unused, always returns zero.	-	-
1	NRSTX	The default value of this bit is 1'b0; When a 1 is written to this bit, the output NRSTXO will be asserted (LOW) within a minimum delay of 7 cycles of the CLK input. The output NRSTXO will be asynchronously asserted and synchronously de-asserted with respect to XCLK. This register is self clearing and will be reset by the input NRST.	RW	R
0	NRST	The default value of this bit is 1'b0; When a 1 is written to this bit, the output NRSTO will be asserted (LOW) within a minimum delay of 7 cycles of the CLK input. The output NRSTO will be asynchronously asserted and synchronously de-asserted with respect to CLK. This register is self clearing and will be reset by the input NRST.	RW	R

35.9 Extended Registers

35.9.1 RqPktCnt

NOTE: HOST MODE ONLY!

For each Rx Endpoint 1 – 15, the MUSBMHDRC provides a 16-bit RqPktCount register. This read/write register is used in Host mode to specify the number of packets that are to be transferred in a block transfer of one or more Bulk packets of length MaxP to Rx Endpoint *n*. The core uses the value recorded in this register to determine the number of requests to issue where the AutoReq option (included in the RxCSR register) has been set.

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NOTE: Multiple packets combined into a single bulk packet within the FIFO count as one packet.

RqPktCnt																0x13440300+4*n
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RqPktCnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15:0	RqPktCnt	Sets the number of packets of size MaxP that are to be transferred in a block transfer. *Only used in Host mode when AutoReq is set. Has no effect in Peripheral mode or when AutoReq is not set.*	RW	RW

35.9.2 RmtWkIntr

Usb remote wakeup interrupt. It will be generated when there's non idle signaling on the bus during system hibernate.

RmtWkIntr																0x13440398
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																RmtWkIntr
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
0	RmtWkIntr	Usb remote wakeup interrupt. Self cleared after read.	RW	S

35.9.3 RmtWkIntrE

Usb remote wakeup interrupt enable.

RmtWkIntrE																0x1344039C
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																RmtWkIntrE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	CPU	USB
0	RmtWkIntrE	Usb remote wakeup interrupt enable. High active.	RW	R

35.9.4 RxDPktBufDis

Rx DPktBufDis is a 16-bit register that indicates which of the Rx endpoints have disabled the double packet buffer functionality described in section 8.4.2.2 of the MUSBMHDRC Product Specification.

NOTE: Bits relating to endpoints that have not been configured may be asserted by writing a '1' their respective register; however the disable bit will have no observable effect.

RxDPktBufDis **0x13440340**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15_Rx_Dis	EP14_Rx_Dis	EP13_Rx_Dis	EP12_Rx_Dis	EP11_Rx_Dis	EP10_Rx_Dis	EP9_Rx_Dis	EP8_Rx_Dis	EP7_Rx_Dis	EP6_Rx_Dis	EP5_Rx_Dis	EP4_Rx_Dis	EP3_Rx_Dis	EP2_Rx_Dis	EP1_Rx_Dis	Unused
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	EP15_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 15.	RW	R
14	EP14_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 14.	RW	R
13	EP13_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 13.	RW	R
12	EP12_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 12.	RW	R
11	EP11_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 11.	RW	R
10	EP10_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 10.	RW	R
9	EP9_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 9.	RW	R
8	EP8_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 8.	RW	R
7	EP7_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 7.	RW	R
6	EP6_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 6.	RW	R
5	EP5_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 5.	RW	R
4	EP4_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 4.	RW	R
3	EP3_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 3.	RW	R
2	EP2_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 2.	RW	R
1	EP1_Rx_Dis	Rx Double Packet Buffer Disable for Endpoint 1.	RW	R
0	Unused	Reserved.	R	R

35.9.5 TxDPktBufDis

Tx DPktBufDis is a 16-bit register that indicates which of the TX endpoints have disabled the double packet buffer functionality described in section 8.4.1.2 of the MUSBMHDRC Product Specification.

NOTE: Bits relating to endpoints that have not been configured may be asserted by writing a '1' their respective register; however the disable bit will have no observable effect.

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TxDPktBufDis **0x13440342**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EP15_Tx_Dis	EP14_Tx_Dis	EP13_Tx_Dis	EP12_Tx_Dis	EP11_Tx_Dis	EP10_Tx_Dis	EP9_Tx_Dis	EP8_Tx_Dis	EP7_Tx_Dis	EP6_Tx_Dis	EP5_Tx_Dis	EP4_Tx_Dis	EP3_Tx_Dis	EP2_Tx_Dis	EP1_Tx_Dis	Unused
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
15	EP15_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 15.	RW	R
14	EP14_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 14.	RW	R
13	EP13_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 13.	RW	R
12	EP12_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 12.	RW	R
11	EP11_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 11.	RW	R
10	EP10_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 10.	RW	R
9	EP9_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 9.	RW	R
8	EP8_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 8.	RW	R
7	EP7_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 7.	RW	R
6	EP6_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 6.	RW	R
5	EP5_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 5.	RW	R
4	EP4_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 4.	RW	R
3	EP3_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 3.	RW	R
2	EP2_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 2.	RW	R
1	EP1_Tx_Dis	Tx Double Packet Buffer Disable for Endpoint 1.	RW	R
0	Unused	Reserved.	R	R

35.9.6 C_T_UCH

This register sets the chirp timeout. This number when multiplied by 4 represents the number of XCLK cycles before the timeout occurs. That is, if XCLK is 30MHz, this number represents the number of 133ns time intervals before the timeout occurs. If XCLK is 60MHz, this number represents the number of 67ns time intervals before the timeout occurs. Although this bit is written by the host in the CLK domain, the counter that utilizes this value is in the XCLK domain. No time domain crossing is provided as the value in this register is a static. The default value is the value of the compiler directive of the same name located in the configuration file musbmhdrc_cfg.v.

C_T_UCH **0x13440344**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C_T_UCH															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	CPU	USB
15:0	C_T_UCH	Configurable Chirp Timeout timer; The default value is determined by compiler directive in musbhsfc_xcfg.v file. The default value is 203Ah if the host PHY data width is 16 bits (XCLK is 30MHz) and 4074h if the PHY data width is 8 bits (XCLK is 60Mhz) corresponding to a delay of 1.1ms.	RW	-

35.9.7 C_T_HHSRTN

This register sets the delay from the end of High Speed resume signaling (acting as a Host) to enable the UTM normal operating mode. This number when multiplied by 4 represents the number of XCLK cycles before the timeout occurs. That is, if XCLK is 30MHz, this number represents the number of 33.3ns time intervals before the timeout occurs. If XCLK is 60MHz, this number represents the number of 16.7ns time intervals before the timeout occurs. Although this bit is written by the host in the CLK domain, the counter that utilizes this value is in the XCLK domain. No time domain crossing is provided as the value in this register is a static. The default value is the value of the compiler directive of the same name located in the configuration file musbmhdrc_cfg.v.

C_T_HHSRTN 0x13440346

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C_T_HHSRTN															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	CPU	USB
15:0	C_T_HHSRTN	The delay from the end of High Speed resume signaling to enabling UTM normal operating mode. The default value is determined by compiler directive in musbhsfc_xcfg.v file. The default value is 2F3h if the host PHY data width is 16 bits (XCLK is 30MHz) and 5E6h if the PHY data width is 8 bits (XCLK is 60Mhz) corresponding to a delay of 100us.	RW	-

35.9.8 C_T_HSBT

Per USB 2.0, Section 7.1.19.2, a high-speed host or device expecting a response to a transmission must not timeout the transaction if the interpacket delay is less than 736 bit times, and it must timeout the transaction if no signaling is seen within 816 bit times. This register represents the value to be

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added to the mimumum high speed timeout period of 736 bit times. The timeout period can be increased in increments of 64 high speed bit times (133 ns). There are 16 possible values. By default, the adder is 0 thus setting the high speed timeout to its minimum value. Use of this register will allow the high speed timeout to be set to values that are greater the maximum specified in USB 2.0 making the MUSBMHDRC non-compliant.

C_T_HSBT					0x13440348
Bit					3 2 1 0
					C_T_HSBT
RST					0 0 0 0

Bits	Name	Description	CPU	USB
3:0	C_T_HSBT	The value added to the minimum High Speed Timeout period (736 bit times) in increments of 64 High Speed bit times. This allows the turn around timeout period to be set to 16 possible values as follows:	RW	R

Register Value	HS Turnaround Timeout (HS Bit times)	HS Turnaround Timeout (us)
0	736	1.534
1	800	1.667
2	864	1.801
3	928	1.934
4	992	2.067
5	1056	2.201
6	1120	2.334
7	1184	2.467
8	1248	2.601
9	1312	2.734
10	1376	2.868
11	1440	3.001
12	1504	3.134
13	1568	3.268
14	1632	3.401
15	1696	3.534

35.10 DMA Registers

35.10.1 DMA_INTR

This register provides an interrupt for each DMA channel. This interrupt register is cleared when read. When any bit of this register is set, the output DMA_NINT is asserted low. Events that cause interrupts

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to be set is described in section 17 (The optional DMA Controller description). Bits in this register will only be set if the DMA Interrupt Enable bit for the corresponding channel is enabled (register DMA_CNTL.D3).

DMA_INTR **0x13440200**

Bit	7	6	5	4	3	2	1	0
	CH8_INT	CH7_INT	CH6_INT	CH5_INT	CH4_INT	CH3_INT	CH2_INT	CH1_INT
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
7	CH8_INT	Channel 8 DMA Interrupt.	RW	Set
6	CH7_INT	Channel 7 DMA Interrupt.	RW	Set
5	CH6_INT	Channel 6 DMA Interrupt.	RW	Set
4	CH5_INT	Channel 5 DMA Interrupt.	RW	Set
3	CH4_INT	Channel 4 DMA Interrupt.	RW	Set
2	CH3_INT	Channel 3 DMA Interrupt.	R	Set
1	CH2_INT	Channel 2 DMA Interrupt.	R	Set
0	CH1_INT	Channel 1 DMA Interrupt.	R	Set

35.10.2 DMA_CNTL

This register is only available if the MUSBMHDRC is configured to use at least one internal DMA channel. This register provides the DMA transfer control for each channel. The enabling, transfer direction, transfer mode, the DMA burst modes are all controlled by this register.

DMA_CNTL **0x13440204+(n-1)*0x10**

Bit	10	9	8	7	6	5	4	3	2	1	0
	DMA_BRSTM	DMA_ERR	DMAEP					DMAIE	DMAMODE	DMA_DIR	DMA_EN
RST	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	CPU	USB
10:9	DMA_BRSTM	Burst Mode. 00 : (Burst Mode 0 : Bursts of unspecified length) 01: (Burst Mode 1 : INCR4 or unspecified length) 10: (Burst Mode 2 : INCR8, INCR4 or unspecified length) 11: (Burst Mode 3 : INCR16, INCR8, INCR4 or unspecified length)	RW	R
8	DMA_ERR	Bus Error Bit. Indicates that a bus error has been observed on the input. AHB_HRESPM[1:0]. This bit is cleared by software.	RW	RW
7:4	DMAEP	The endpoint number this channel is assigned to.	RW	R
3	DMAIE	DMA Interrupt Enable.	RW	R
2	DMAMODE	This bit selects the DMA Transfer Mode. 0: DMA Mode0 Transfer 1: DMA Mode1 Transfer	RW	R
1	DMA_DIR	This bit selects the DMA Transfer Direction. 0: DMA Write (RX Endpoint) 1: DMa Read (TX Endpoint)	RW	R
0	DMA_ENAB	This bit enables the DMA transfer and will cause the transfer to begin.	RW	R

35.10.3 DMA_ADDR

This register identifies the current memory address of the corresponding DMA channel. The Initial memory address written to this register must have a value such that its modulo 4 value is equal to 0. That is, DMA_ADDR[1:0] must be equal to 2'b00. The lower two bits of this register are read only and cannot be set by software. As the DMA transfer progresses, the memory address will increment as bytes are transferred.

DMA_ADDR **0x13440208+(n-1)*0x10**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	CPU	USB
31:0	DMA_ADDR	The DMA memory address. **Note that the initial memory address written to this register must have a value such that it's modulo 4 value is equal to 0. That is, DMA_ADDR[1:0] must be equal to 2'b00. The lower two bits of this register are read only and cannot be set by software.**	RW	RW

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35.10.4 DMA_COUNT

This register identifies the current DMA count of the transfer. Software will set the initial count of the transfer which identifies the entire transfer length. As the count progresses this count is decremented as bytes are transferred.

DMA_CNT																															0x1344020c+(n-1)*0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_CNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

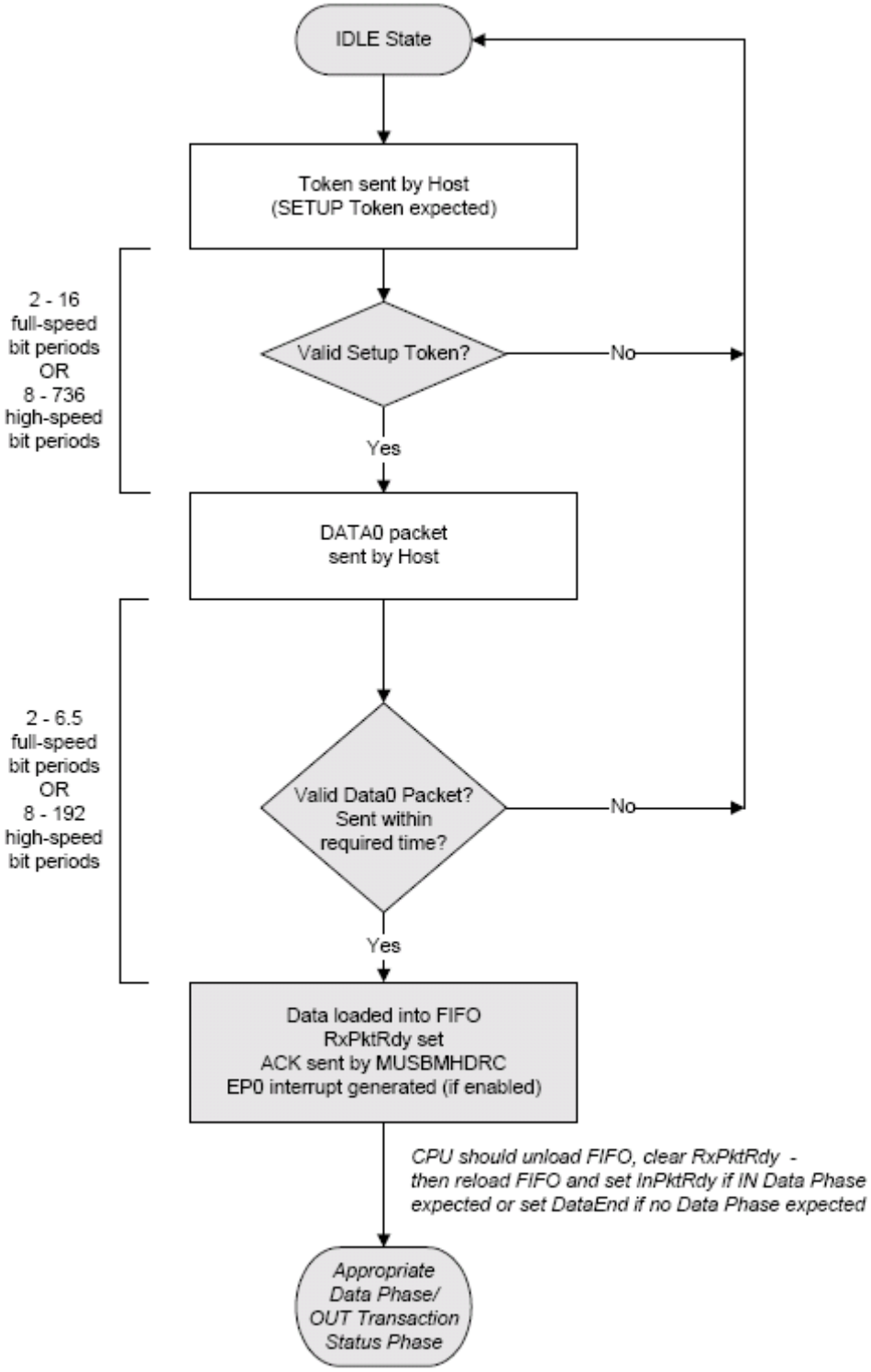
31:0	DMA_CNT	The DMA memory address for the corresponding DMA channel. **NOTE:** If DMA is enabled with a count of 0, the bus will not be requested and a DMA interrupt will be generated.	RW	RW

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35.11 Transaction flows as a peripheral

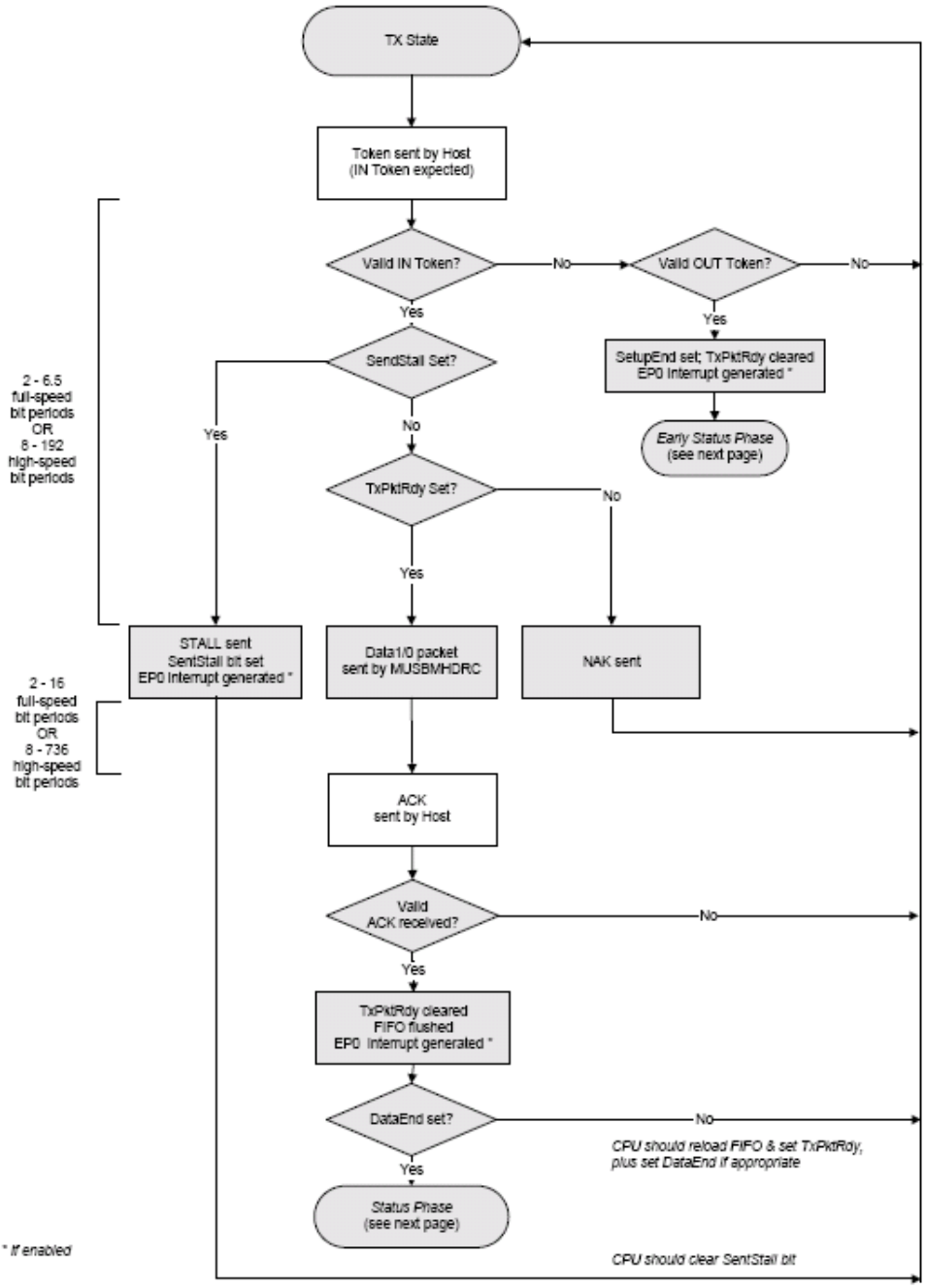
35.11.1 Control transactions

35.11.1.1 Setup phase



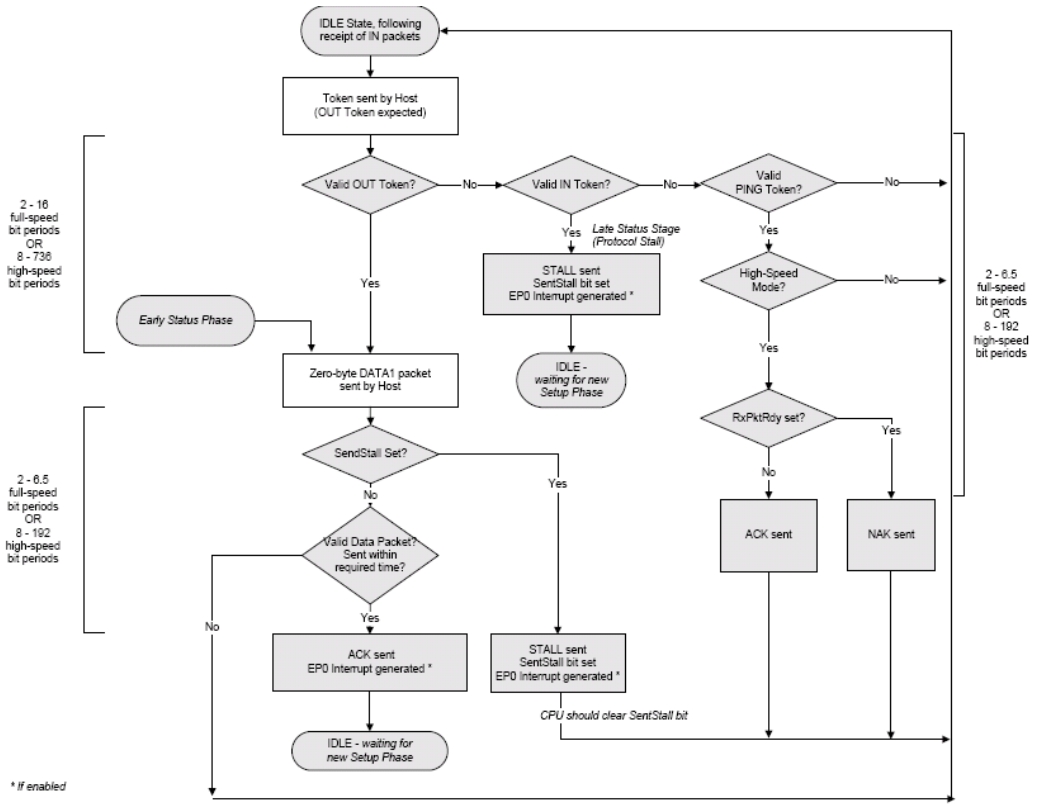
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35.11.1.2 In data phase



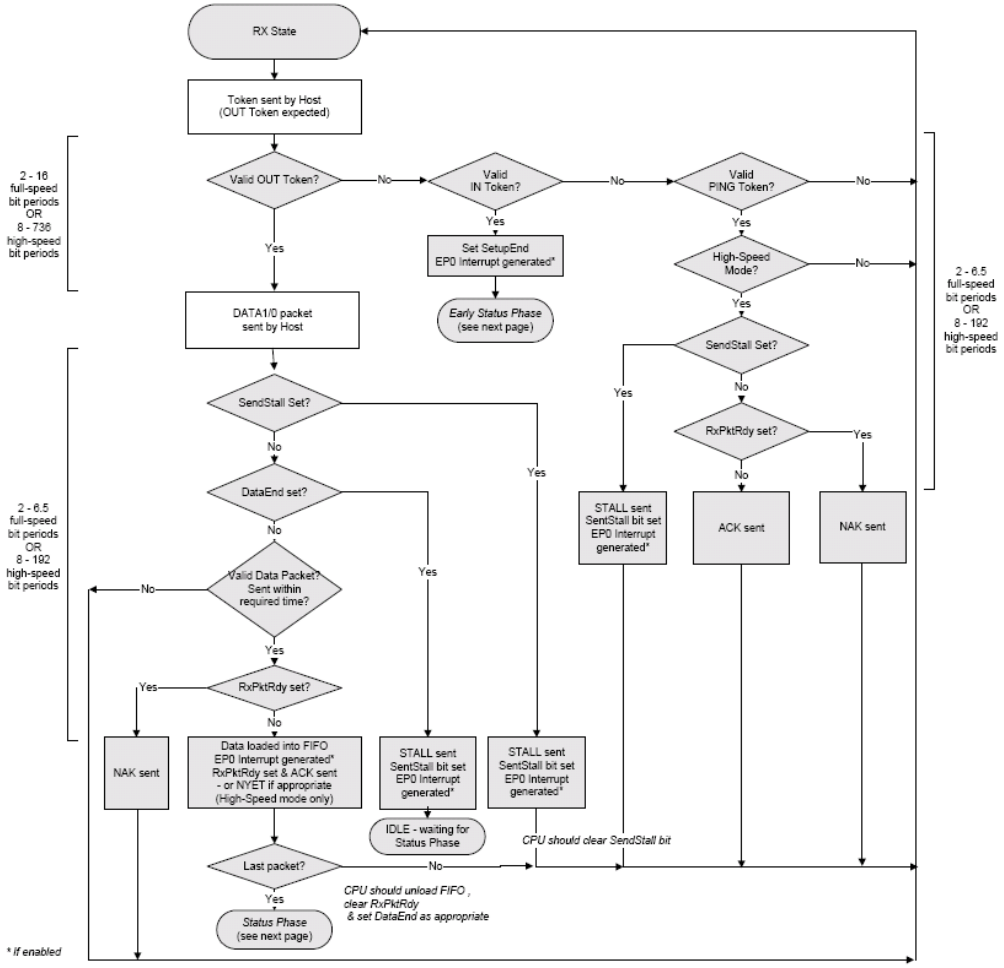
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35.11.1.3 Following the status phase



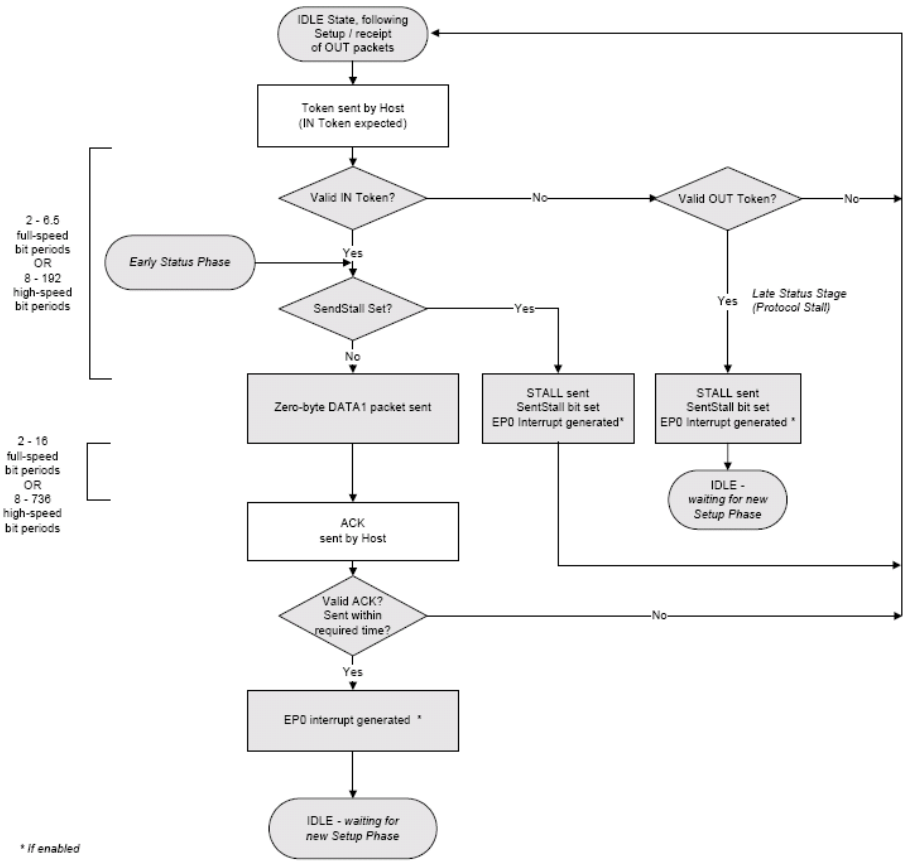
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35.11.1.4 Out data phase



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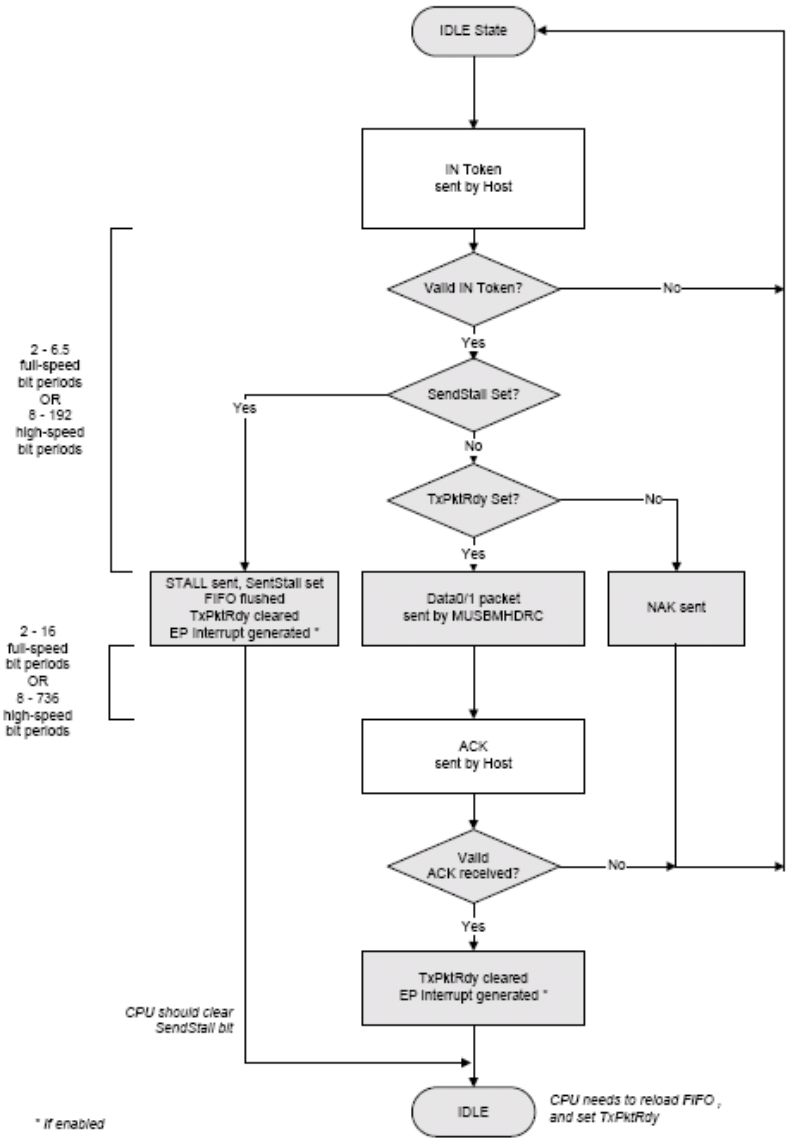
35.11.1.5 Following the status phase



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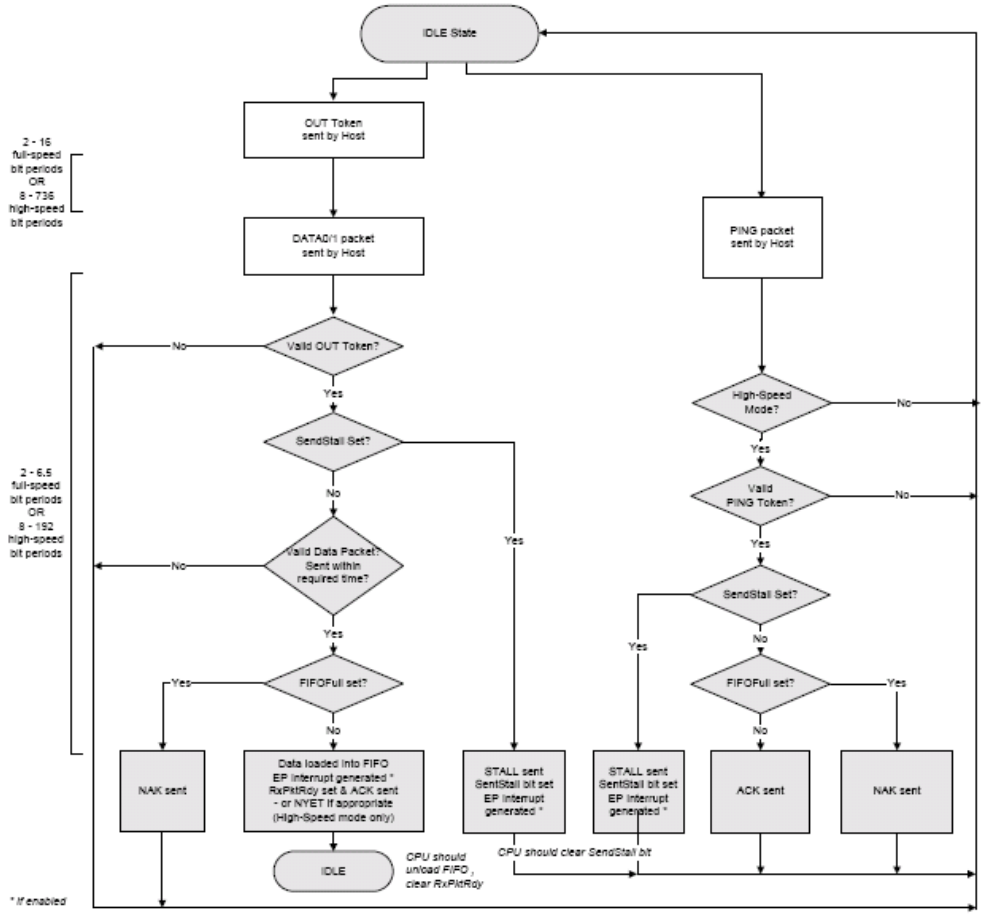
35.11.2 Bulk/Low-bandwidth interrupt transactions

35.11.2.1 In transaction



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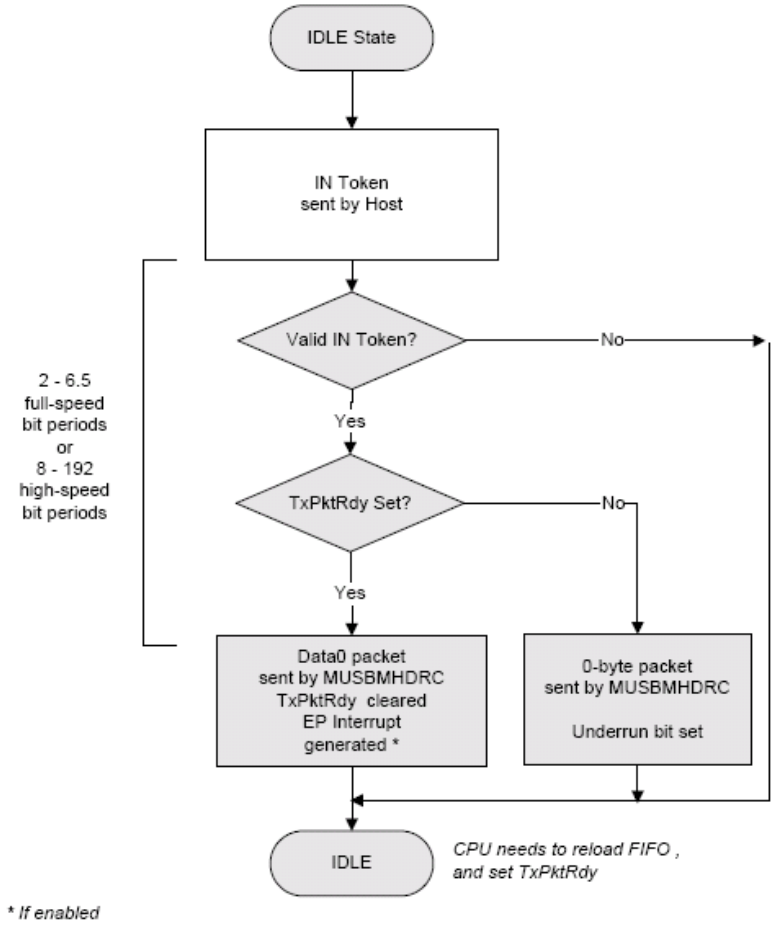
35.11.2.2 Out transaction



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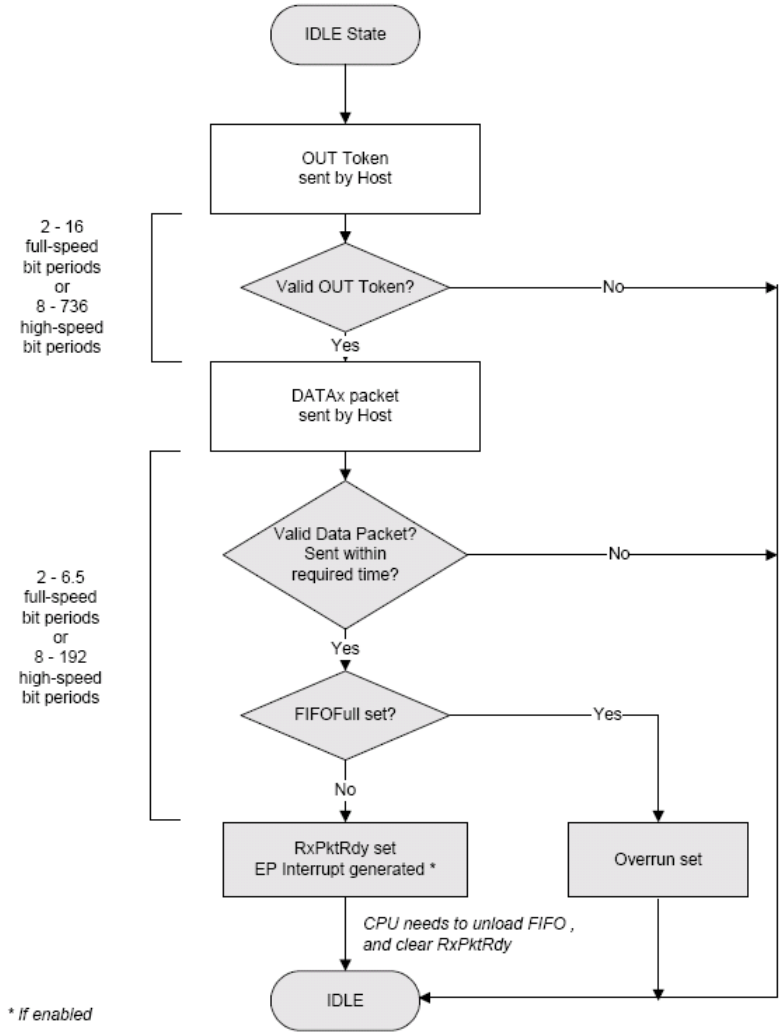
35.11.3 Full-speed/Low-bandwidth isochronous transactions

35.11.3.1 In transaction



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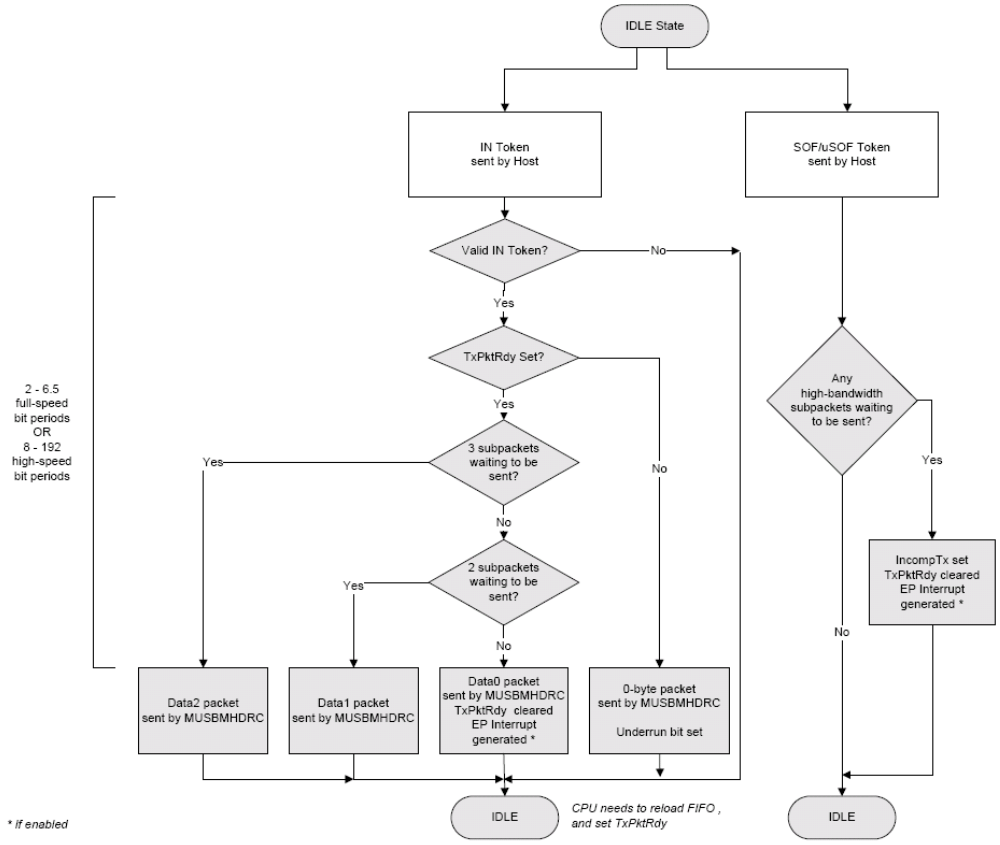
35.11.3.2 Out transaction



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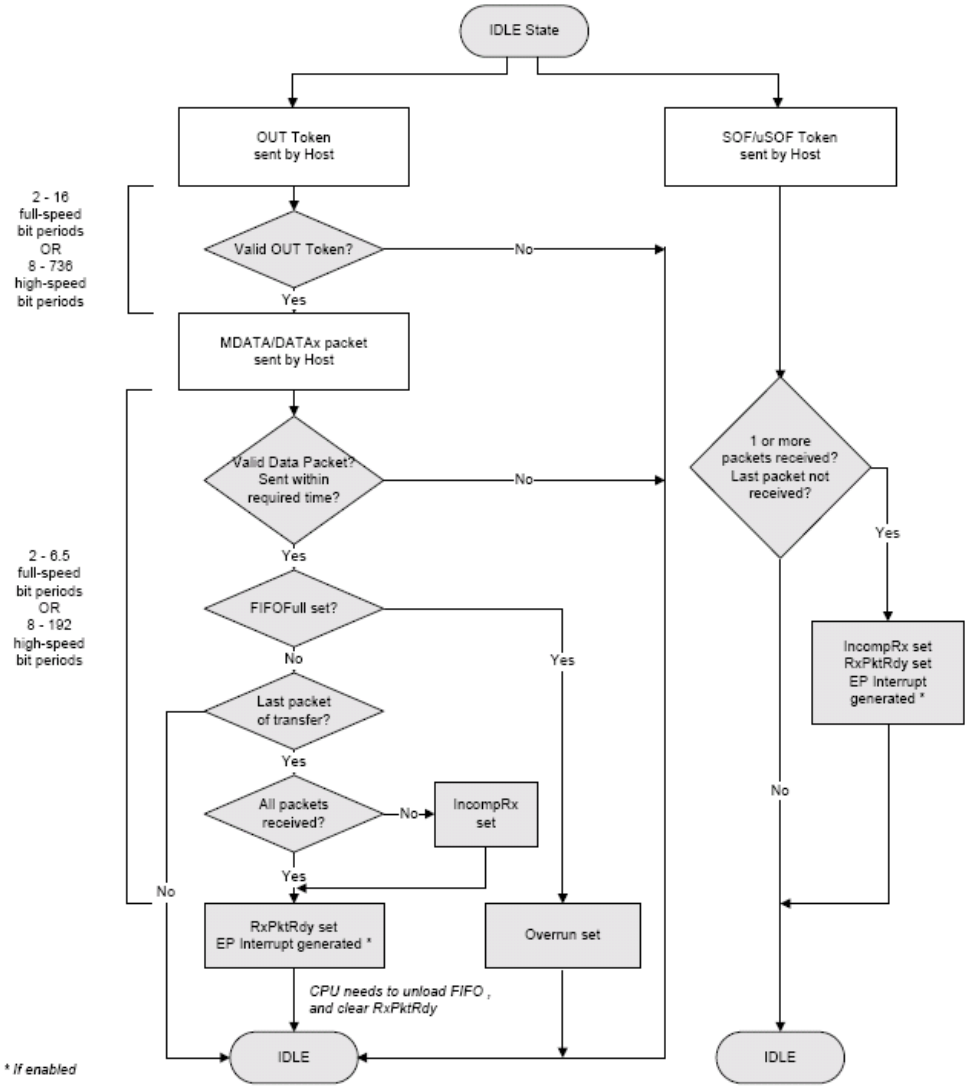
35.11.4 High-bandwidth transactions (Isochronous and interrupt)

35.11.4.1 In transaction



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35.11.4.2 Out transaction

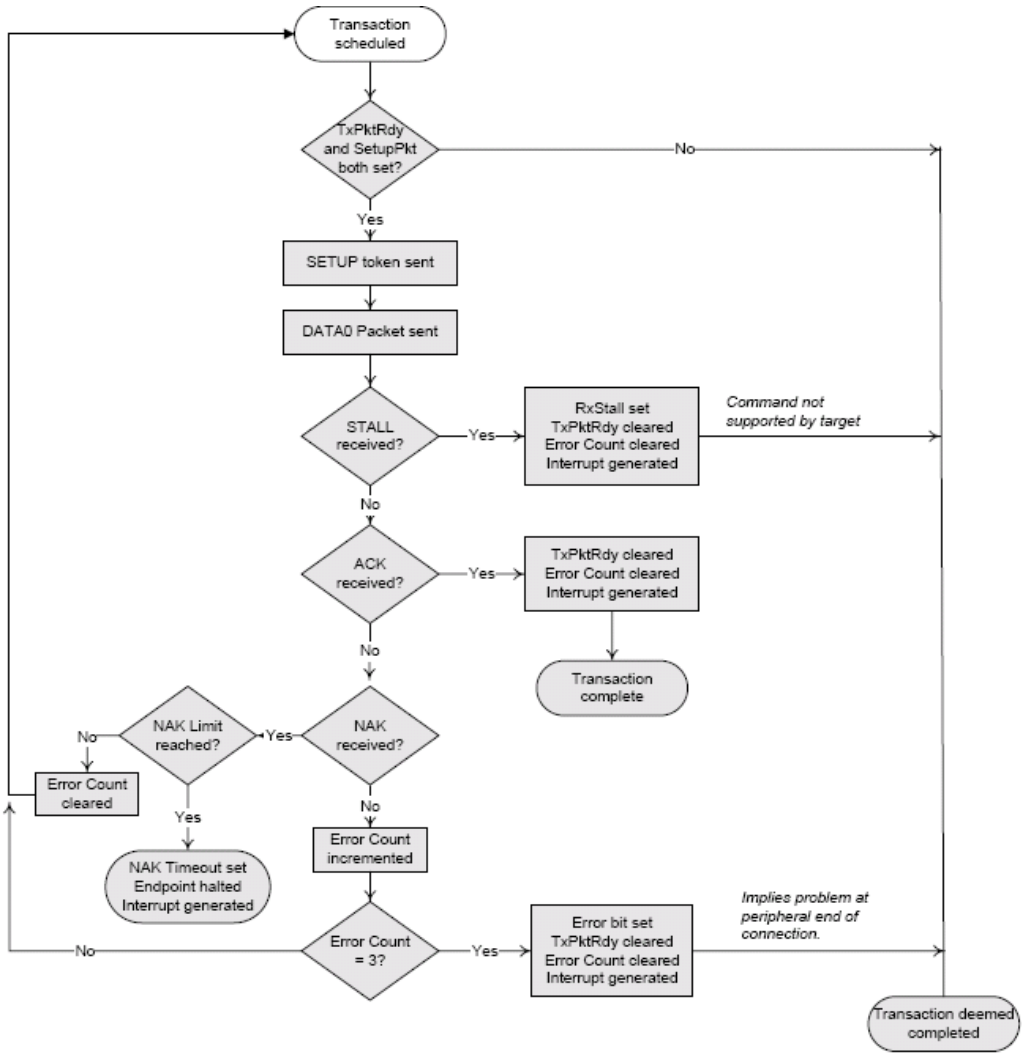


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35.12 Transaction flows as a host

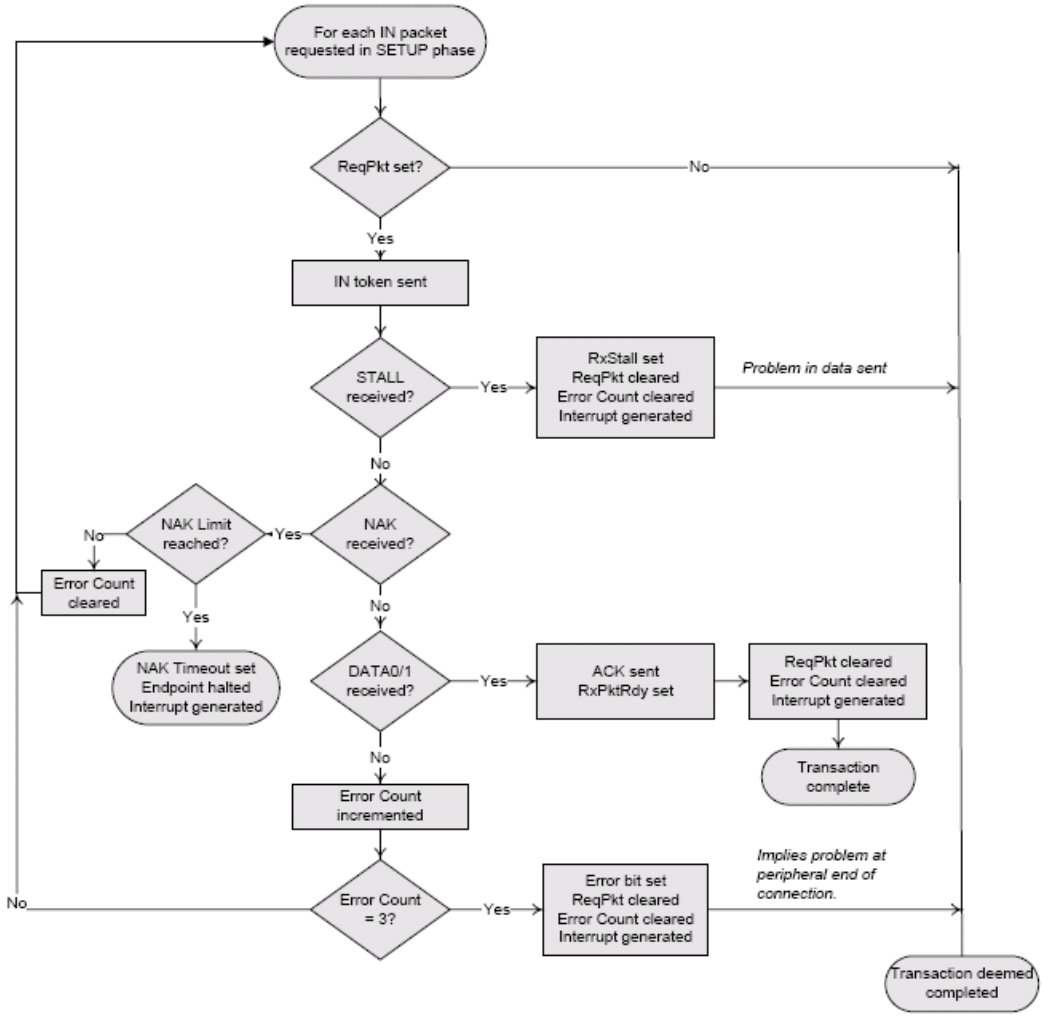
35.12.1 Control transactions

35.12.1.1 Setup phase



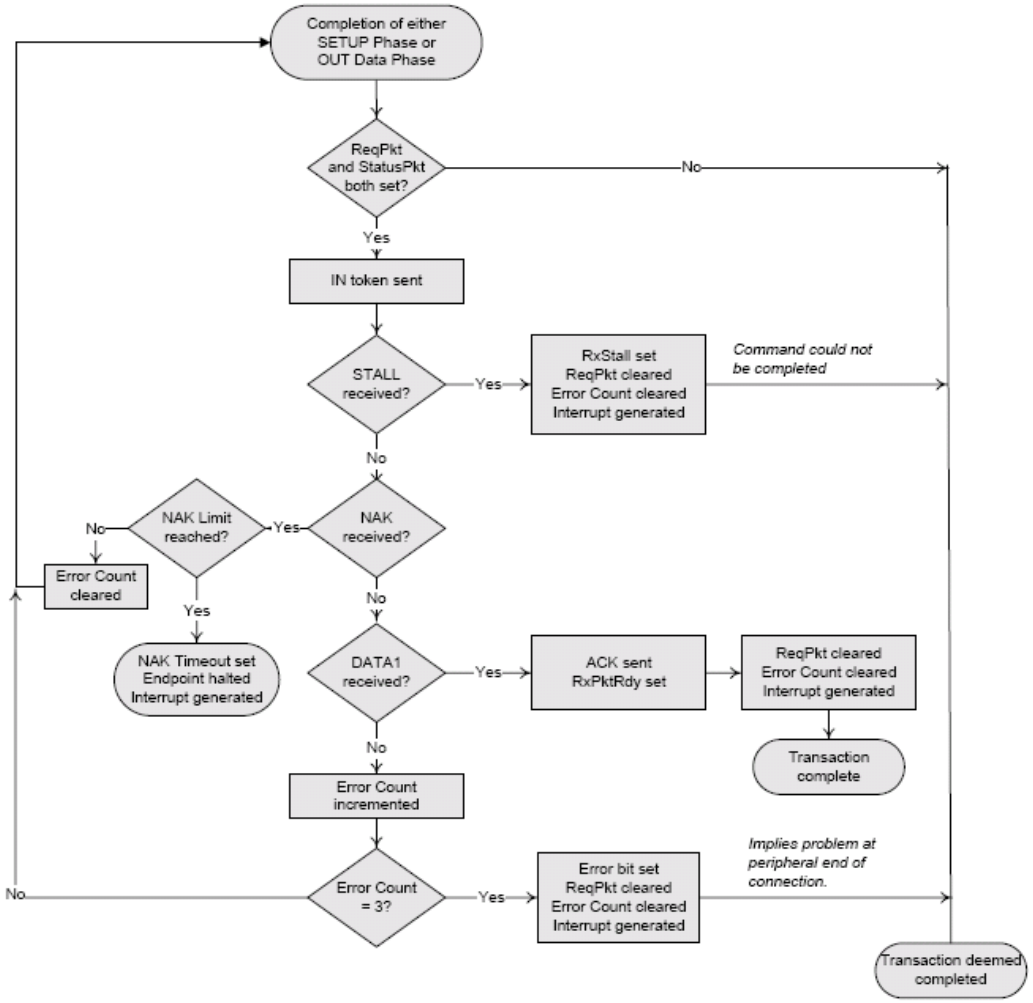
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35.12.1.2 In data phase



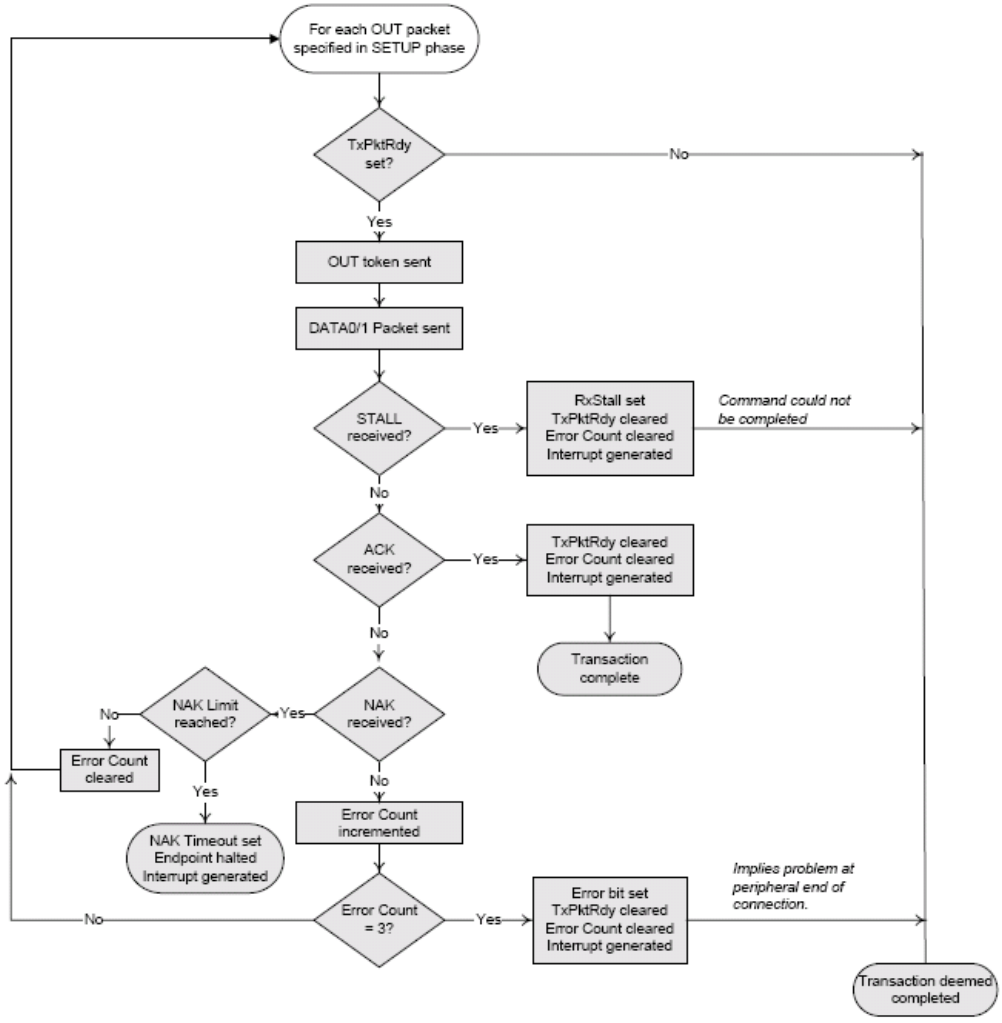
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35.12.1.3 Following the status phase



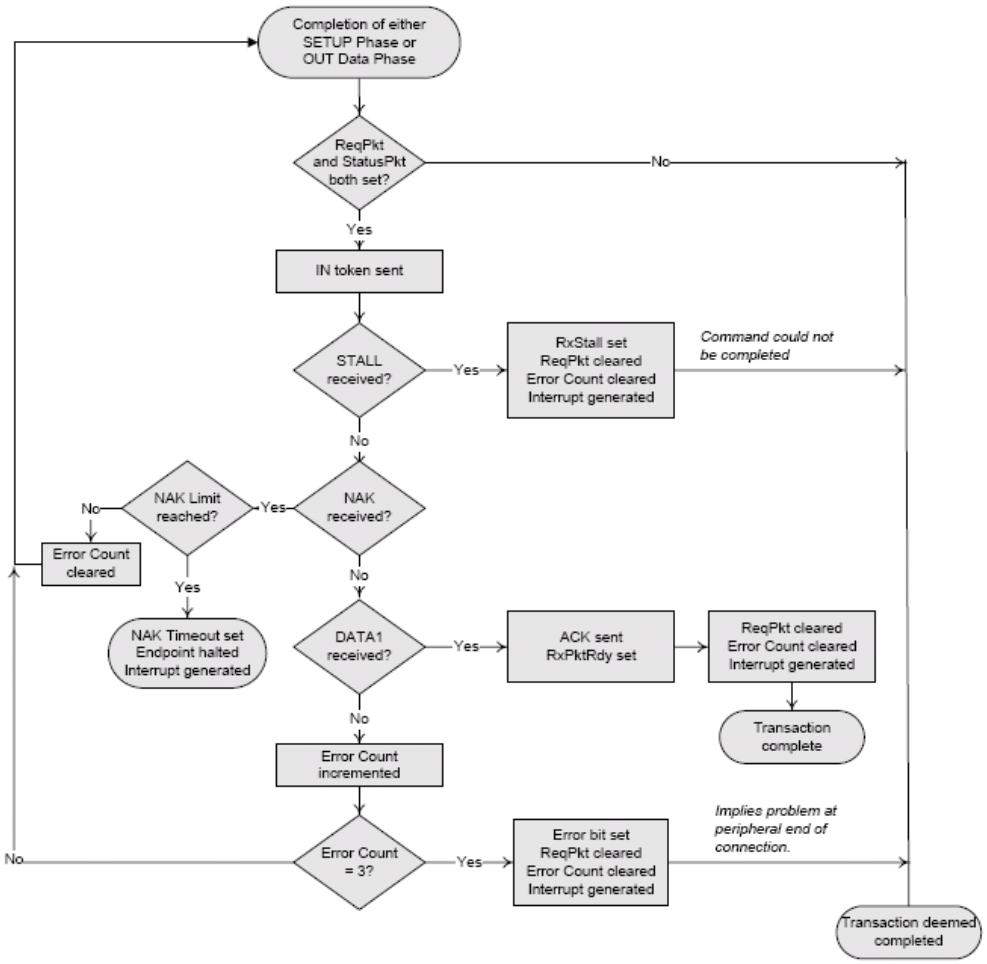
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35.12.1.4 Out data phase



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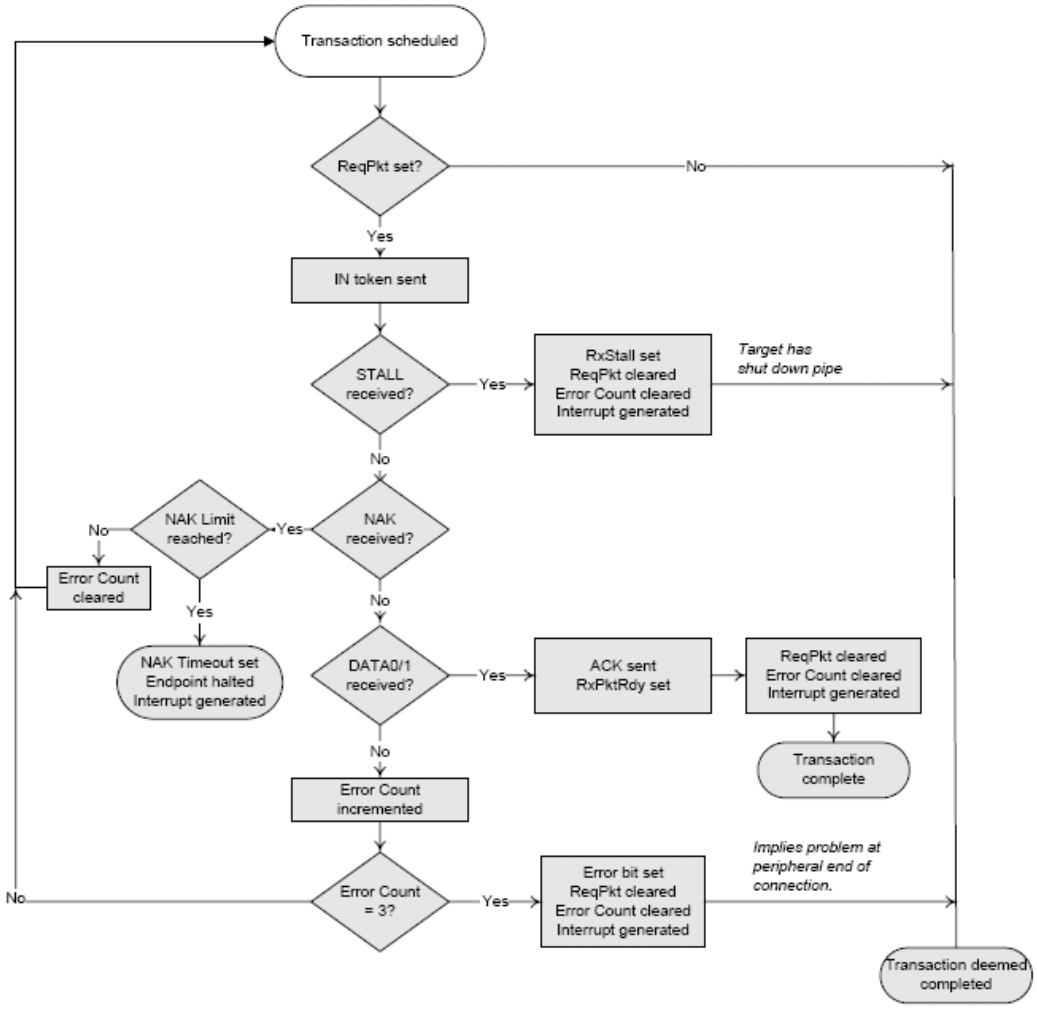
35.12.1.5 Following the status phase



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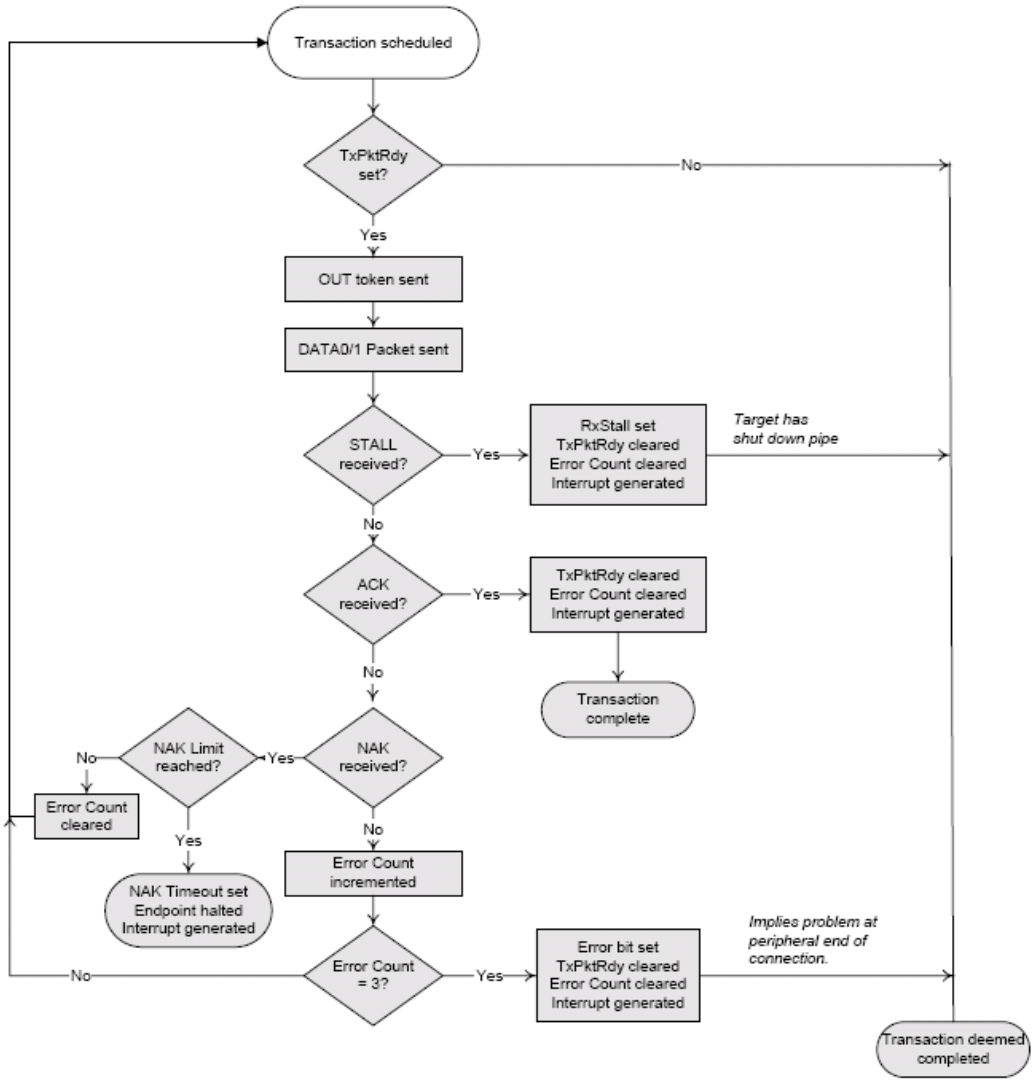
35.12.2 Bulk/Low-bandwidth interrupt transactions

35.12.2.1 In transaction



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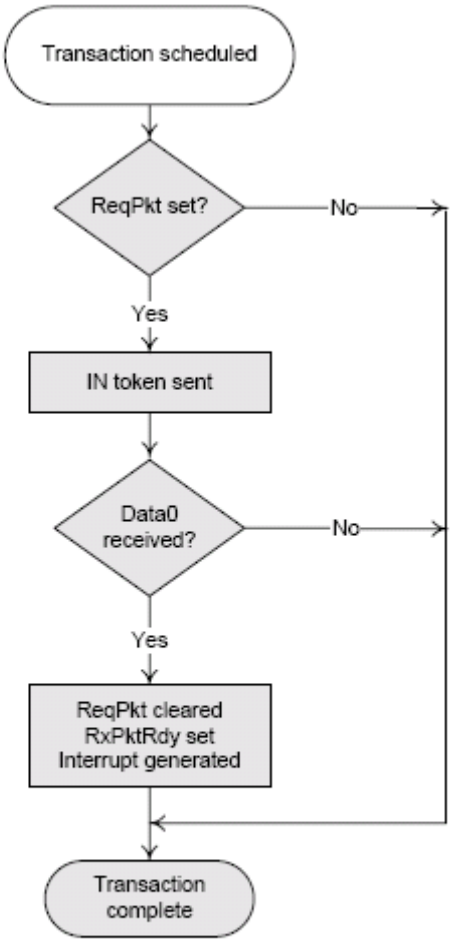
35.12.2.2 Out transaction



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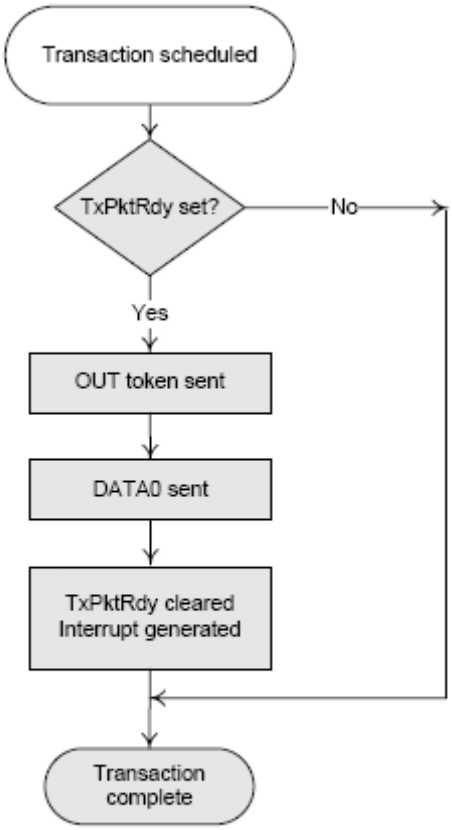
35.12.3 Full-speed/Low-bandwidth isochronous transactions

35.12.3.1 In transaction



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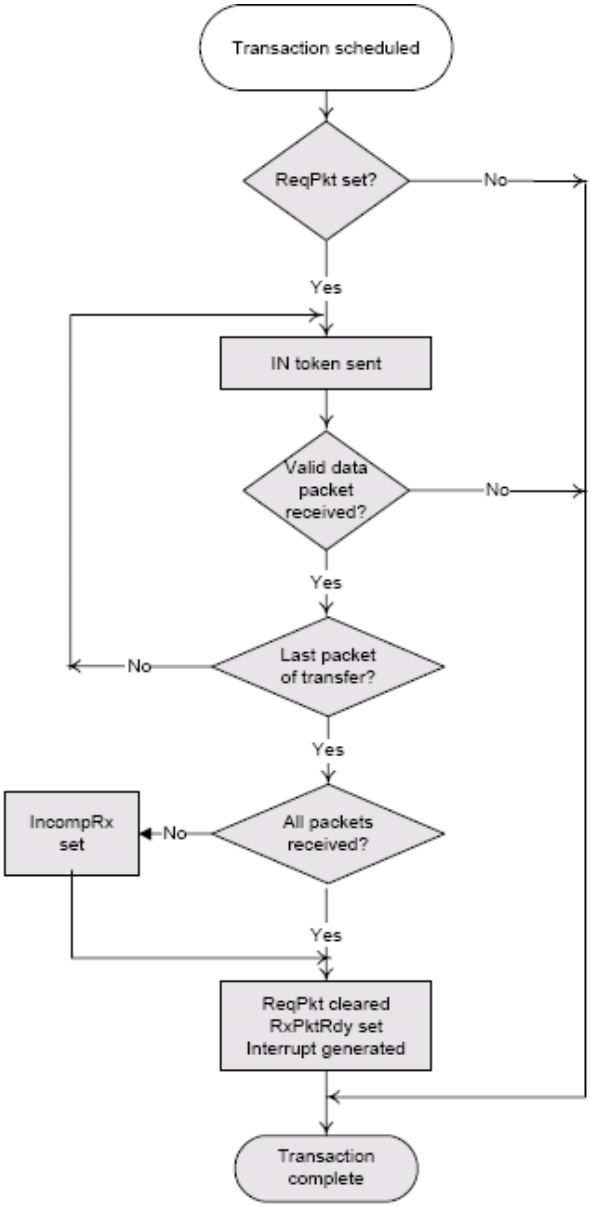
35.12.3.2 Out transaction



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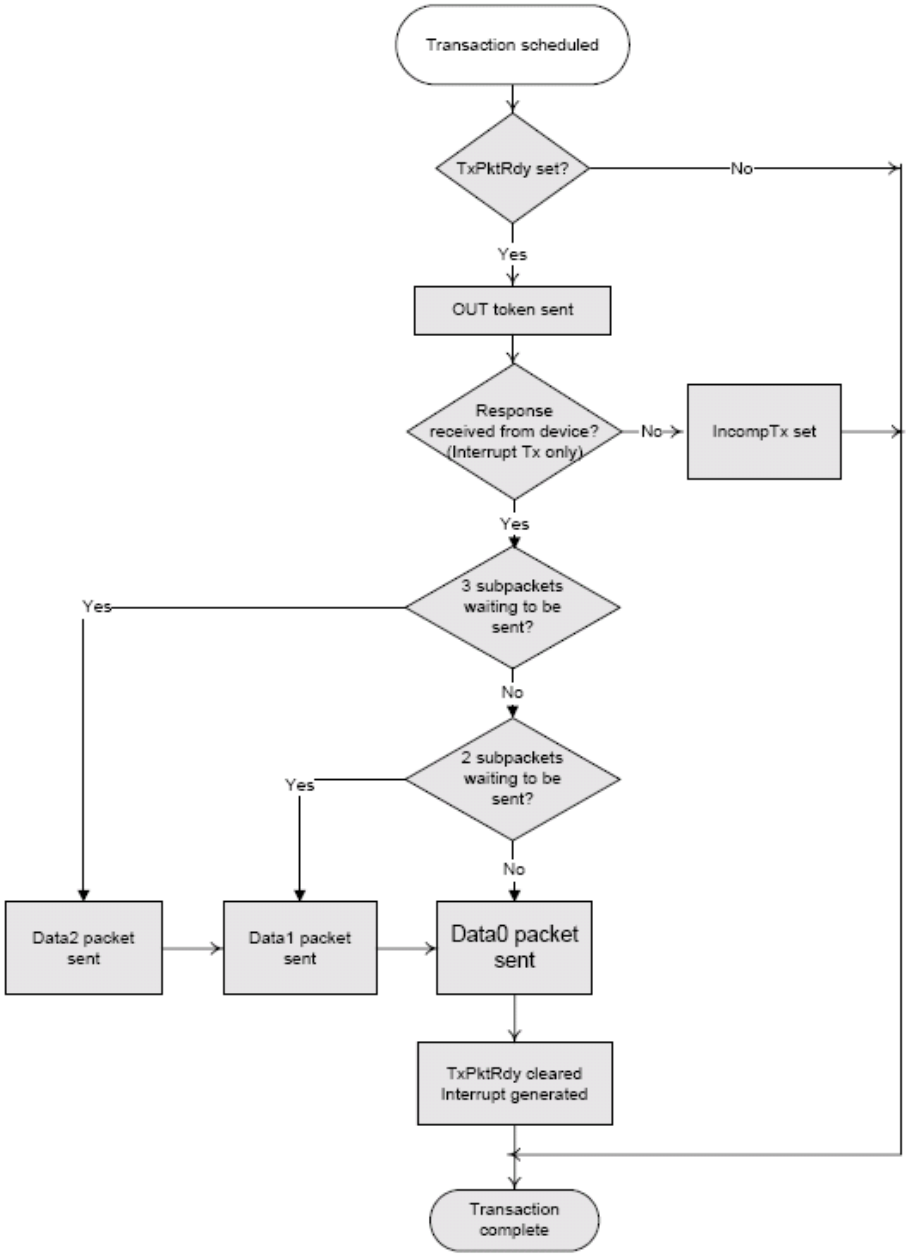
35.12.4 High-bandwidth transactions (isochronous and interrupt)

35.12.4.1 In transaction



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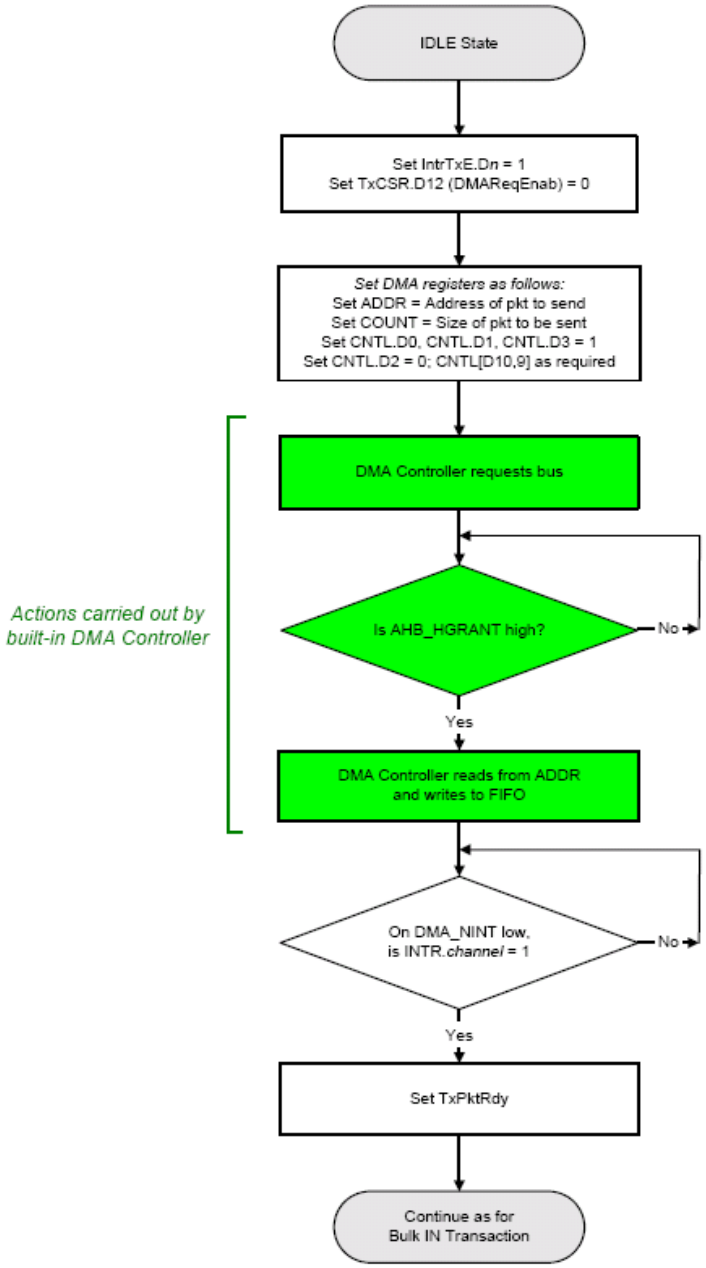
35.12.4.2 Out transaction



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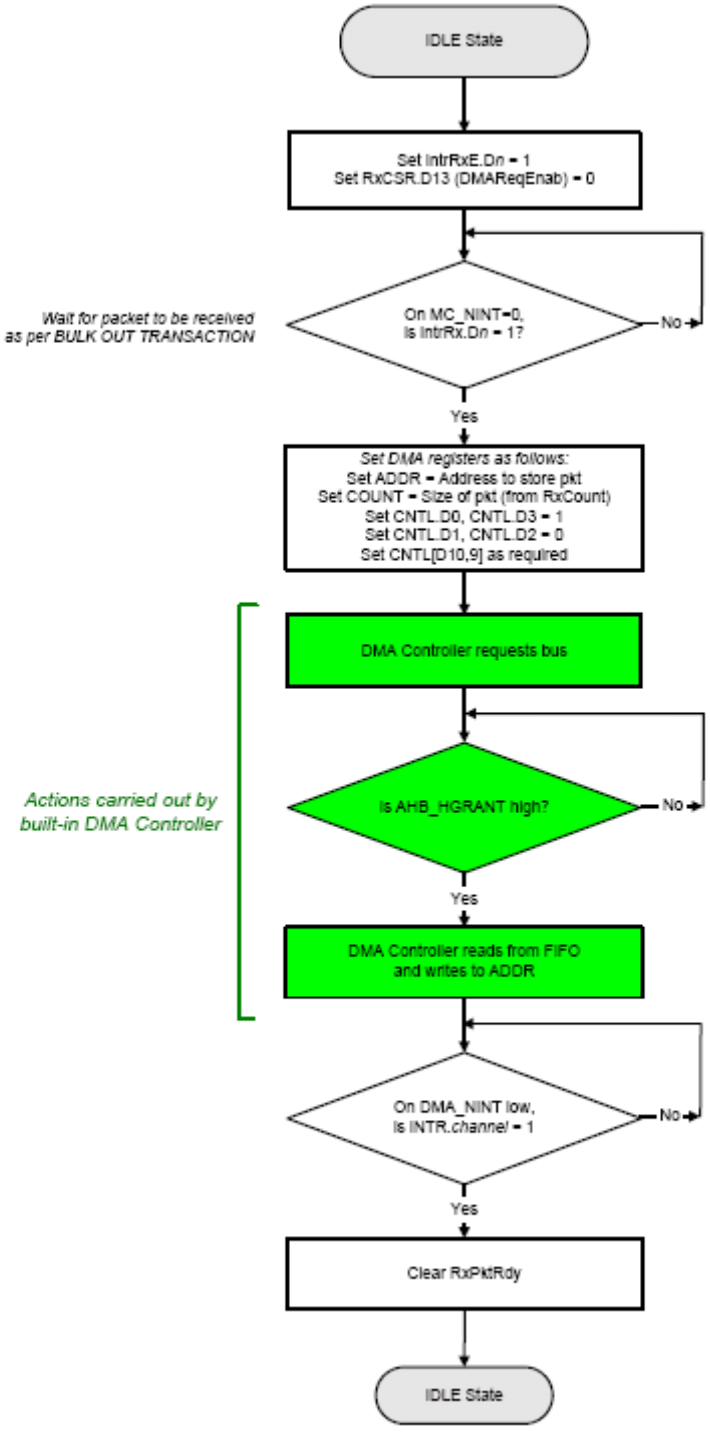
35.13 DMA operations

35.13.1 Single packet tx



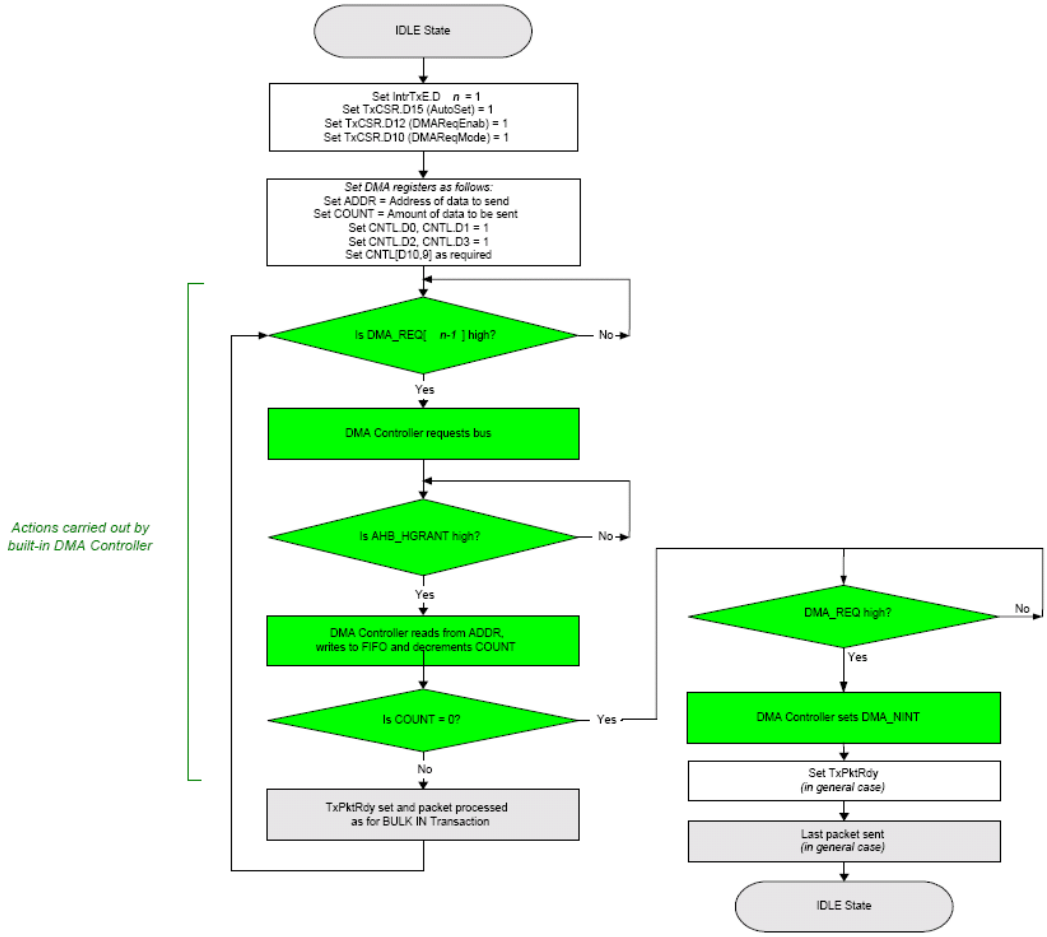
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35.13.2 Single packet rx



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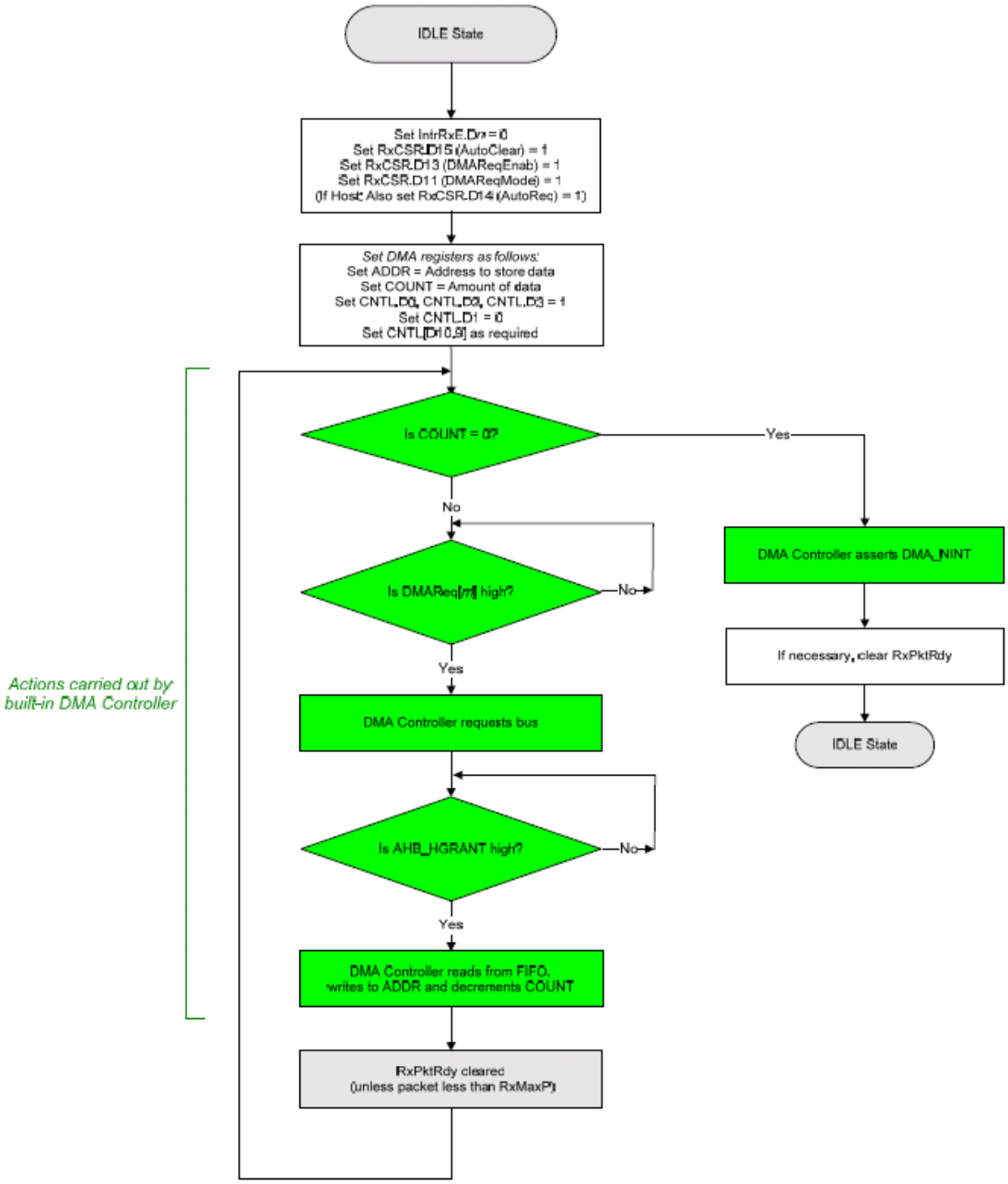
35.13.3 Multiple packet tx



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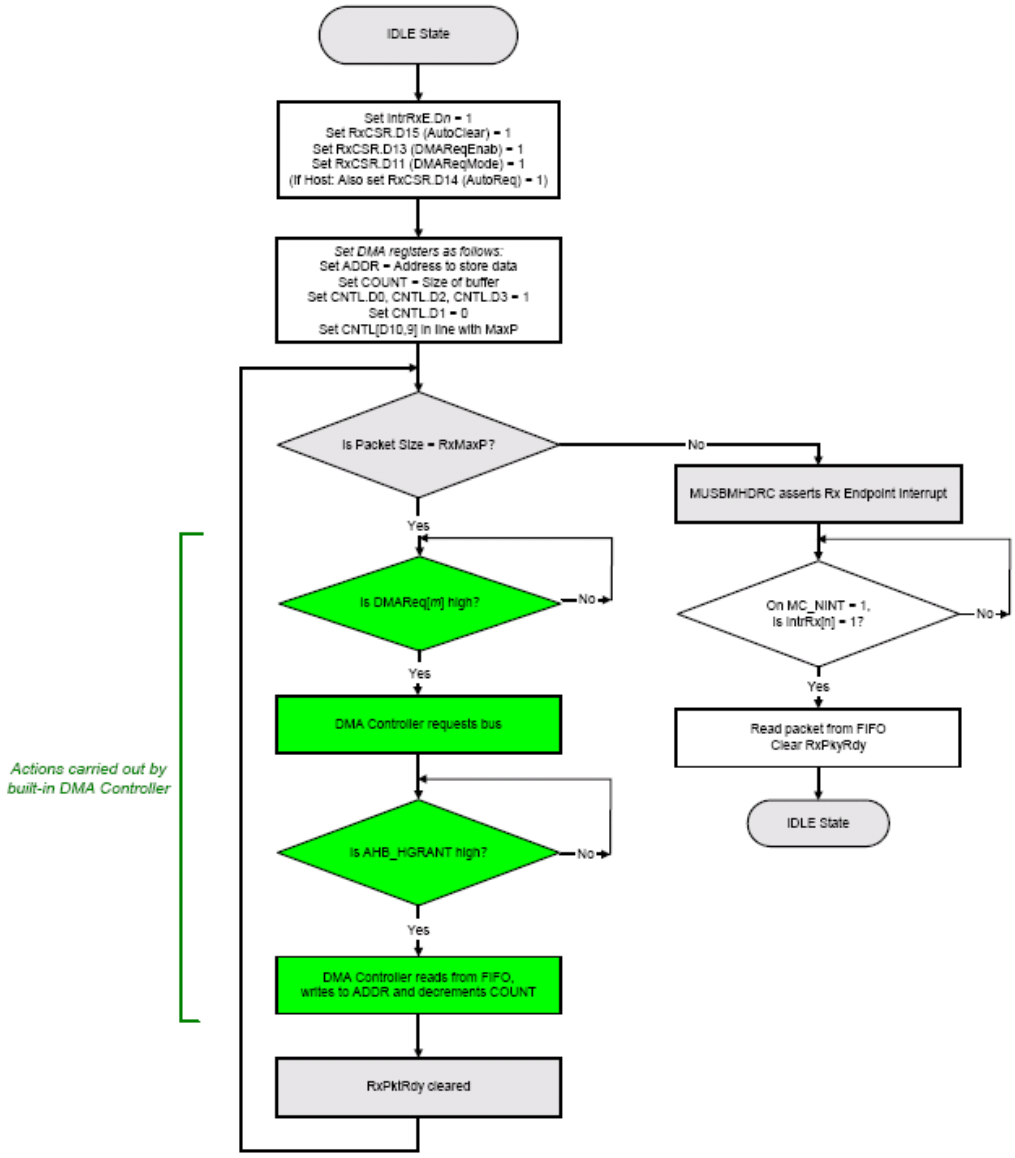
35.13.4 Multiple packet rx

If Size of Data Block Known:



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If Size of Data Block Not Known:



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36 MMC/SD CE-ATA Controller

36.1 Overview

The MultiMediaCard (MMC) is a universal low cost data storage and communication media that is designed to cover a wide area of applications such as electronic toys, organizers, PDAs, smart phones, and so on.

The Secure Digital (SD) card is an evolution of MMC, It is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are forward compatible with the MultiMediaCard with some additions. An SD card can be categorized as SD memory or SD I/O card, commonly known as SDIO. A memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard and is faster and capable of higher memory capacity. The SDIO card provides high-speed data I/O with low-power consumption for mobile electronic devices.

For CE-ATA detail protocol , please referred to WWW.CE-ATA.ORG.

Features of the MSC Controller include the following:

- Fully compatible with the *MMC System Specification version 4.2*
- Fully compatible with the *SD Memory Card Specification 2.0* and *SD I/O Specification 1.0* with 1 command channel and 4 data channels
- Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- 20-80 Mbps maximum data rate
- Support MMC data width 1bit ,4bit and 8bit
- Built-in programmable frequency divider for MMC/SD bus
- Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
- 32-entry x 32-bit built-in data FIFO
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

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36.2 Block Diagram

MSC Controller Block Diagram

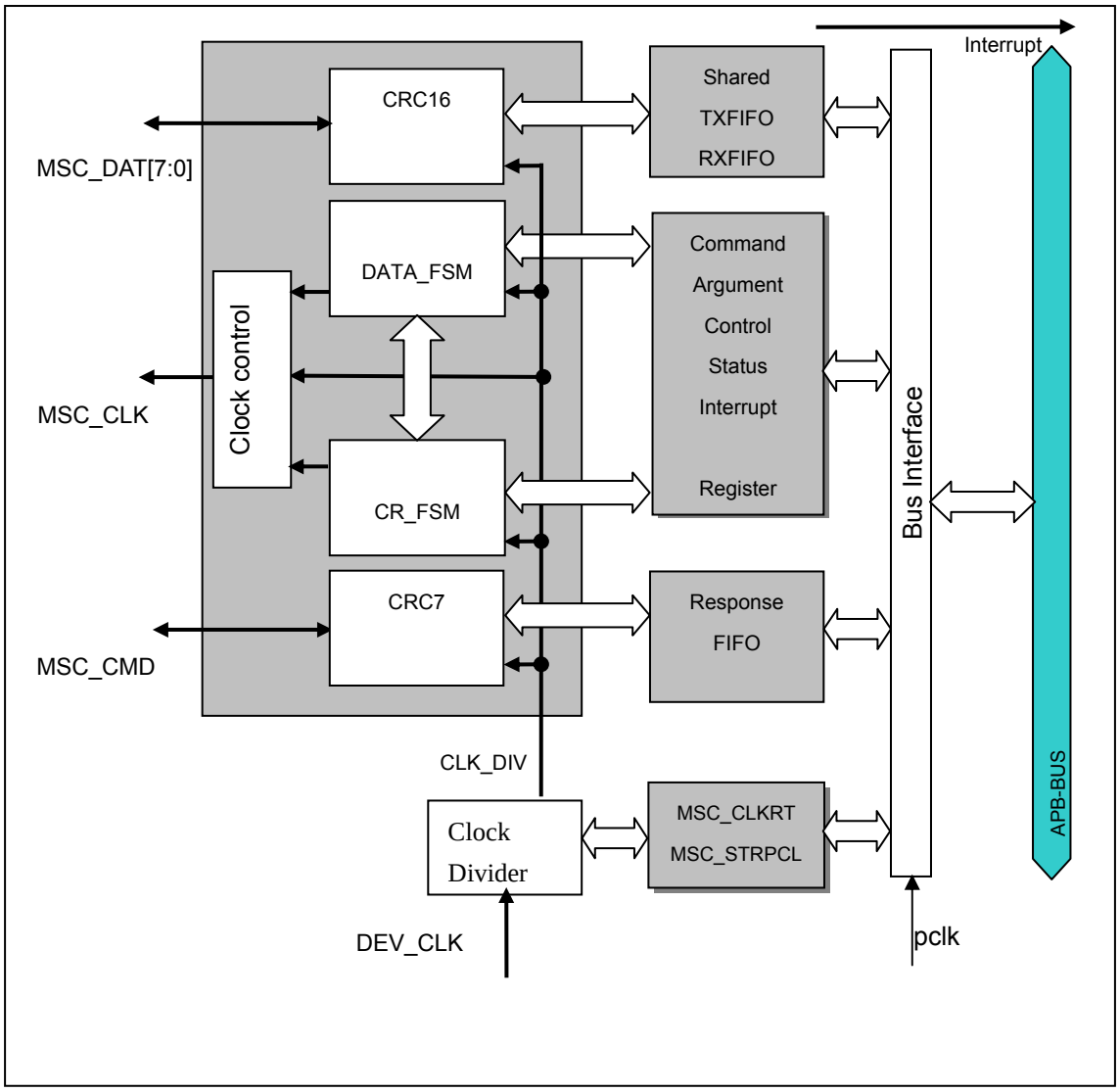


Figure 36-1 MMC/SD CE-ATA Controller Block Diagram

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36.3 MMC/SD Controller Signal I/O Description

MSC and the card communication over the CMD and DATA line is base on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

Command: a command is a token, which starts an operation. A command is sent from MSC either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line. Each command token is preceded by a start bit (‘0’) and succeeded by an end bit (‘1’). The total length is 48 bits and protected by CRC bits.

Table 36-1 Command Token Format

Bit position	**47**	**46**	**[45 : 40]**	**[39 : 8]**	**[7 : 1]**	**0**
Width (bits)	1	1	6	32	7	1
Value	0	1	X	X	x	1
Description	Start bit	Transmission bit	Command index	argument	CRC7	End bit

Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to MSC as an answer to a previously received command. A response is transferred serially on the CMD line. Response tokens have varies coding schemes depending on their content.

Data: data can be transferred from the card to MSC or vice versa. Data is transferred via the data line. Data transfers to/from the SD Memory Card are done in blocks. Data blocks always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the MSC to use single or multiple data lines.

Table 36-2 MMC/SD Data Token Format

Description	**Start bit**	**Data**	**CRC16**	**End bit**
Stream Data	0	X	no CRC	1
Block Data	0	X	X	1

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36.4 Register Description

The MMC-SD-CE_ATA controller is controlled by a set of registers that the application configures before every operation. The Table 36-3 lists all the MSC registers.

Table 36-3 MMC/SD Controller Registers Description

Name	RW	Reset Value	Address	Access Size
MSC_CTRL0	W	0x0000	0x10021000	16
MSC_STAT0	R	0x00000040	0x10021004	32
MSC_CLKRT0	RW	0x0000	0x10021008	16
MSC_CMDAT0	RW	0x00000000	0x1002100C	32
MSC_RESTO0	RW	0x40	0x10021010	16
MSC_RDTO0	RW	0xFFFF	0x10021014	32
MSC_BLKLEN0	RW	0x0000	0x10021018	16
MSC_NOB0	RW	0x0000	0x1002101C	16
MSC_SNOB0	R	0x????	0x10021020	16
MSC_IMASK0	RW	0x00FF	0x10021024	32
MSC_IREG0	RW	0x0000	0x10021028	16
MSC_CMD0	RW	0x00	0x1002102C	8
MSC_ARG0	RW	0x00000000	0x10021030	32
MSC_RES0	R	0x????	0x10021034	16
MSC_RXFIFO0	R	0x????????	0x10021038	32
MSC_TXFIFO0	W	0x????????	0x1002103C	32
MSC_LPM0	RW	0x00000000	0x10021040	32
MSC_CTRL1	W	0x0000	0x10022000	16
MSC_STAT1	R	0x00000040	0x10022004	32
MSC_CLKRT1	RW	0x0000	0x10022008	16
MSC_CMDAT1	RW	0x00000000	0x1002200C	32
MSC_RESTO1	RW	0x40	0x10022010	16
MSC_RDTO1	RW	0xFFFF	0x10022014	32
MSC_BLKLEN1	RW	0x0000	0x10022018	16
MSC_NOB1	RW	0x0000	0x1002201C	16
MSC_SNOB1	R	0x????	0x10022020	16
MSC_IMASK1	RW	0x00FF	0x10022024	32
MSC_IREG1	RW	0x0000	0x10022028	16
MSC_CMD1	RW	0x00	0x1002202C	8
MSC_ARG1	RW	0x00000000	0x10022030	32
MSC_RES1	R	0x????	0x10022034	16
MSC_RXFIFO1	R	0x????????	0x10022038	32
MSC_TXFIFO1	W	0x????????	0x1002203C	32
MSC_LPM1	RW	0x00000000	0x10022040	32

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36.4.1 MMC/SD Control Register (MSC_CTRL)

MSC_CTRL0 0x10021000

MSC_CTRL1 0x10022000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SEND_CCSD	SEND_AD_CCSD	Reserved						EXIT_MULTIPLE	EXIT_TRANSFER	START_READWAIT	STOP_READWAIT	RESET	START_OP	STRPCL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	SEND_CCSD	0: clear bit 1: Send Command Completion Signal Disable (CCSD) to CE_ATA device when set, host sends CCSD to CE_ATA device. Software set the bit only if current command is expecting CCS and interrupts are enabled in CE_ATA devices. Once the CCSD pattern is sent to device, host automatically clears the SEND_CCSD bit.	W
14	SEND_AS_CCSD	0: clear bit 1: send internally generated stop after sending CCSD to CE_ATA device When set, host automatically sends internally-generated STOP command(CMD12) to CE_ATA device. After sending CMD12, Auto Command Done (ACD) is set and generates interrupt to CPU. After sending the CCSD, controller automatically clears the SEND_AS_CCSD bit.	W
13:8	Reserved	Writing has no effect, read as zero.	R
7	EXIT_MULTIPLE	If CMD12 or CMD52 (I/O abort) is to be sent to terminate multiple block read/write in advance, set this bit to 1. 0: No effect; 1: Exit from multiple block read/write.	W
6	EXIT_TRANSFER	**Only used for SDIO suspend/resume and MMC stream read.** For SDIO, after suspend is accepted, set this bit with 1. For MMC, after the data of the expected number are received, set this bit with 1. 0: No effect 1: Exit from multiple block read/write after suspend is accepted, or exit from stream read	W
5	START_READWAIT	Only used for SDIO ReadWait. Start the ReadWait cycle. 0: No effect; 1: Start ReadWait	W

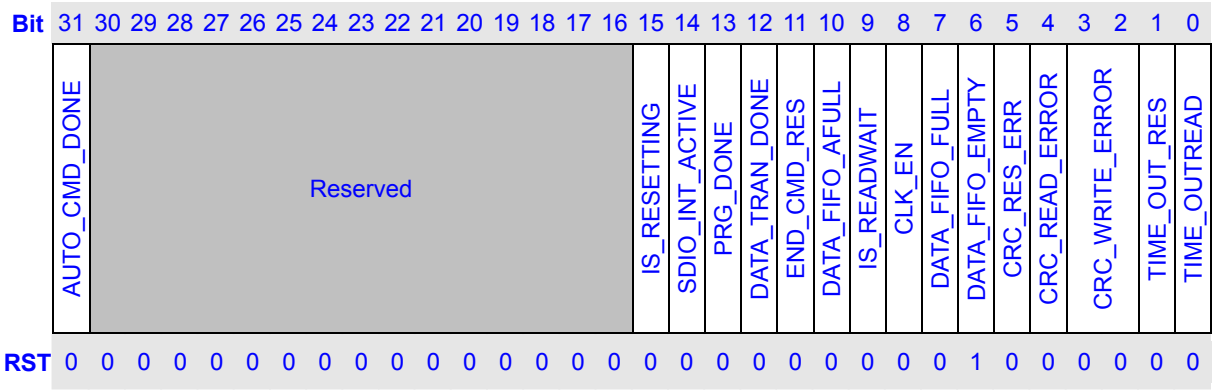
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4	STOP_READWAIT	Only used for SDIO ReadWait. Stop the ReadWait cycle. 0: No effect; 1: Start ReadWait.	W
3	RESET	Resets the MMC/SD controller. 0: No effect; 1: Reset the MMC/SD controller.	W
2	START_OP	This bit is used to start the new operation. When starting the clock, this bit can be 1. When stopping the clock, this bit can only be 0. 0: Do nothing; 1: Start the new operation.	W
1:0	CLOCK_CONTROL	These bits are used to start or stop clock. 00: Do nothing 01: Stop MMC/SD clock 10: Start MMC/SD clock 11: Reserved	W

36.4.2 MSC Status Register (MSC_STAT)

MSC_STAT0 **0x10021004**

MSC_STAT1 **0x10022004**



Bits	Name	Description	RW
31	AUTO_CMD_DONE	Indicate that the stop command (CMD12) that is internally generated by controller has finished.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15	IS_RESETTING	MSC is resetting after power up or MSC_STRPCL[RESET] is written with 1. 0: Reset has been finished; 1: Reset has not been finished.	R
14	SDIO_INT_ACTIVE	Indicates whether an interrupt is detected at the SD I/O card. A separate acknowledge command to the card is required to clear this interrupt. 0: No interrupt detected 1: The interrupt from SDIO is detected	R
13	PRG_DONE	Indicates whether card has finished programming.	R

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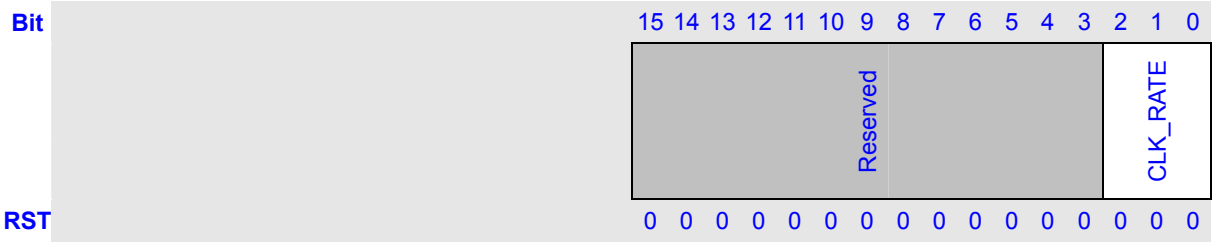
		0: Card has not finished programming and is busy 1: Card has finished programming and is not busy	
12	DATA_TRAN_DONE	Indicates whether data transmission to card has completed. 0: Data transmission to card has not completed 1: Data transmission to card has completed	R
11	END_CMD_RES	End command-response sequence or command sequence. 0: Command and response/no-response sequence has not completed 1: Command and response/no-response sequence has completed	R
10	DATA_FIFO_AFULL	Indicates whether data FIFO is almost full (The number of words >= 15). For reading data from card, use this bit. 0: Data FIFO is not full; 1: Data FIFO is full.	R
9	IS_READWAIT	Indicates whether SDIO card has entered ReadWait State. 0: Card has not entered ReadWait 1: Card has entered ReadWait	R
8	CLK_EN	Clock enabled. 0: Clock is off; 1: Clock is on.	R
7	DATA_FIFO_FULL	Indicates whether data FIFO is full. For reading data from card, do not use this bit, because it almost keeps to be 0. 0: Data FIFO is not full; 1: Data FIFO is full.	R
6	DATA_FIFO_EMPTY	Indicates whether data FIFO is empty. 0: Data FIFO is not empty; 1: Data FIFO is empty.	R
5	CRC_RES_ERR	Response CRC error. 0: No error on the response CRC 1: CRC error occurred on the response	R
4	CRC_READ_ERROR	CRC read error. 0: No error on received data 1: CRC error occurred on received data	R
3:2	CRC_WRITE_ERROR	CRC write error. 00: No error on transmission of data 01: Card observed erroneous transmission of data 10: No CRC status is sent back 11: Reserved	R
1	TIME_OUT_RES	Response time out. 0: Card response has not timed out 1: Card response has time out	R
0	TIME_OUT_READ	Read time out. 0: Card read data has not timed out 1: Card read data has timed out	R

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36.4.3 MSC Clock Rate Register (MSC_CLKRT)

The MSC_CLKRT register specifies the frequency division of the MMC/SD bus clock. The software is responsible for setting this register.

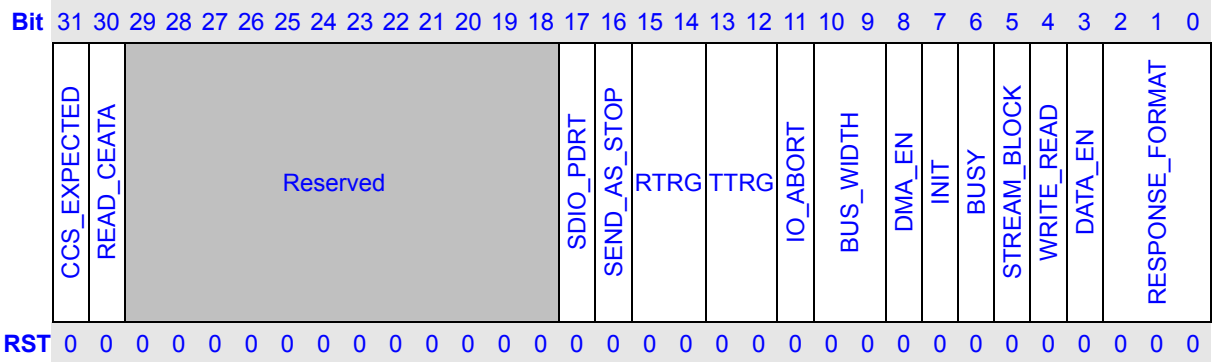
MSC_CLKRT0 **0x10021008**
MSC_CLKRT1 **0x10022008**



Bits	Name	Description	RW
15:3	Reserved	Writing has no effect, read as zero.	R
2:0	CLK_RATE	Clock rate. 000: CLK_DIV 001: 1/2 of CLK_DIV 010: 1/4 of CLK_DIV 011: 1/8 of CLK_DIV 100: 1/16 of CLK_DIV 101: 1/32 of CLK_DIV 110: 1/64 of CLK_DIV 111: 1/128 of CLK_DIV	WR

36.4.4 MMC/SD Command and Data Control Register (MSC_CMDAT)

MSC_CMDAT0 **0x1002100C**
MSC_CMDAT1 **0x1002200C**



Bits	Name	Description	RW
31	CCS_EXPECTED	0: interrupts are not enabled in CE-ATA device, or commands does not expect CCS from device	RW

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		1: interrupts are enabled in CE_ATA device, or RW_BLK command expects command completion signal from device If the command expects Command Completion Signal (CCS) from the device, the software should set the control bit. It is auto cleared 0 by hardware.	
30	READ_CEATA	0: host is not performing read access (RW_BLK or RW_REG) towards CE_ATA device 1: host id performing read access (RW_BLK or RW_REG) towards CE_ATA device Software should set the bit to indicate that CE_ATA device is being accessed for read transfer. The bit is used to disable read data timeout indication while performing CE_ATA read transfers. It is auto cleared 0 by hardware.	RW
29:18	Reserved	Writing has no effect, read as zero.	R
17	SDIO_PRDT	Determine whether SDIO interrupt is 2 cycle or extend more cycle when data block last is transferred. 0: more cycle (like single block) 1: exact 2 cycle	RW
16	SEND_AS_STOP	0: no stop command sent at end of data transfer 1: send stop command at end of data transfer when stop command has finished, it is auto cleared 0 by hardware.	RW
15:14	RTRG	These bits set the receive FIFO half-empty threshold value, when the number of transmit FIFO >= threshold value , RXFIFO_RD_REQ will be set to 1. 00 : more than or equal to 8 01: more than or equal to 16 10: more than or equal to 24 11: reserved	RW
13:12	TTRG	These bits set the transmit FIFO half-empty threshold value, when the number of transmit FIFO < threshold value , TXFIFO_WR_REQ will be set to 1. 00 : less than 8 01: less than 16 10: less than 24 11: reserved	RW
11	STOP_ABORT	Specifies the current command is used to abort data transfer. 0: Nothing 1: The current command is used to abort transfer it is auto cleared 0 by hardware.	WR
10:9	BUS_WIDTH	Specifies the width of the data bus.	WR

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		00: 1-bit 01: Reserved 10: 4-bit 11: 8bit	
8	DMA_EN	DMA mode enables. When DMA mode is used, this bit is also a mask on RXFIFO_RD_REQ and TXFIFO_WR_REQ interrupts. 0: Program I/O; 1: DMA mode.	WR
7	INIT	80 initialization clocks. 0: Do not precede command sequence with 80 clocks 1: Precede command sequence with 80 clocks	W
6	BUSY	Specifies whether a busy signal is expected after the current command. This bit is for no data command/response transactions only. 0: Not expect a busy signal 1: Expects a busy signal. If the response is R1b, then set it	WR
5	STREAM_BLOCK	Stream mode. 0: Data transfer of the current command sequence is not in stream mode 1: Data transfer of the current command sequence is in stream mode	WR
4	WRITE_READ	Specifies that the data transfer of the current command is a read or write operation. 0: Specifies that the data transfer of the current command is a read operation 1: Specifies that the data transfer of the current command is a write operation	WR
3	DATA_EN	Specifies whether the current command includes a data transfer. It is also used to reset RX_FIFO and TX_FIFO. 0: No data transfer with current command 1: Has data transfer with current command. It is also used to reset RX_FIFO and TX_FIFO	WR
2:0	RESPONSE_FORMAT	These bit specify the response format for the current command. 000: No response 001: Format R1 and R1b 010: Format R2 011: Format R3 100: Format R4 101: Format R5 110: Format R6 111: Format R7	WR

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36.4.5 MMC/SD Response Time Out Register (MSC_RESTO)

MSC_RESTO0 **0x10021010**

MSC_RESTO1 **0x10022010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								RES_TO							
RST	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	RES_TO	Specifies the number of MSC_CLK clock counts between the command and when the MMC/SD controller turns on the time-out error for the received response. The default value is 64.	WR

36.4.6 MMC/SD Read Time Out Register (MSC_RDTO)

MSC_RDTO0 **0x10021014**

MSC_RDTO1 **0x10022014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ_TO																															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	READ_TO	Specifies the number of clocks between the command and when the MMC/SD host controller turns on the time-out error for the received data. The unit is MSC_CLK.	WR

36.4.7 MMC/SD Block Length Register (MSC_BLKLEN)

MSC_BLKLEN0 **0x10021018**

MSC_BLKLEN1 **0x10022018**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLK_LEN															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:0	BLK_LEN	Specifies the number of bytes in a block, and is normally set to 0x200	WR

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		for MMC/SD data transactions. The value Specified in the cards CSD.	

36.4.8 MSC/SD Number of Block Register (MSC_NOB)

MSC_NOB0 **0x1002101C**
MSC_NOB1 **0x1002201C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NOB															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:0	NOB	Specifies the number of blocks in a data transfer. One block is a possibility.	WR

36.4.9 MMC/SD Number of Successfully-transferred Blocks Register (MSC_SNOB)

In block mode, the MSC_SNOB register records the number of successfully transferred blocks. If the last block has CRC error, this register also summaries it. It is used to query blocks for multiple block transfer.

MSC_SNOB0 **0x10021020**
MSC_SNOB1 **0x10022020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSC_SNOB															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15:0	MSC_SNOB	Specify the number of successfully transferred blocks for a multiple block transfer.	R

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36.4.10 MMC/SD Interrupt Mask Register (MSC_IMASK)

MSC_IMASK0 **0x10021024**

MSC_IMASK1 **0x10022024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																AUTO_CMD_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	AUTO_CMD_DONE	Mask the interrupt Auto Cmd Done (ACD). 0: Not masked; 1: Masked.	RW
14	DATA_FIFO_FULL	0: Not masked; 1: Masked.	RW
13	DATA_FIFO_EMP	0: Not masked; 1: Masked.	RW
12	CRC_RES_ERR	0: Not masked; 1: Masked.	RW
11	CRC_READ_ERR	0: Not masked; 1: Masked.	RW
10	CRC_WRITE_ERR	0: Not masked; 1: Masked.	RW
9	TIME_OUT_RES	0: Not masked; 1: Masked.	RW
8	TIME_OUT_READ	0: Not masked; 1: Masked.	RW
7	SDIO	Mask the interrupt from the SD I/O card. 0: Not masked; 1: Masked.	WR
6	TXFIFO_WR_REQ	Mask the Transmit FIFO write request interrupt. 0: Not masked; 1: Masked.	WR
5	RXFIFO_RD_REQ	Mask the Receive FIFO read request interrupt. 0: Not masked; 1: Masked.	WR
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Mask the End command response interrupt. 0: Not masked; 1: Masked.	WR
1	PRG_DONE	Mask the Programming done interrupt. 0: Not masked; 1: Masked.	WR
0	DATA_TRAN_DONE	Mask the Data transfer done interrupt. 0: Not masked; 1: Masked.	WR

36.4.11 MMC/SD Interrupt Register (MSC_IREG)

The MSC_IREG register shows the currently requested interrupt. The FIFO request interrupts, TXFIFO_WR_REQ, and RXFIFO_RD_REQ are masked off with the DMA_EN bit in the MSC_CMDAT

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register. The software is responsible for monitoring these bit in program I/O mode.

MSC_IREG0 **0x10021028**

MSC_IREG1 **0x10022028**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUTO_CMD_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	AUTO_CMD_DONE	indicate Auto Cmd Done (ACD) interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
14	DATA_FIFO_FULL	Indicate data FIFO is full interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
13	DATA_FIFO_EMP	Indicate data FIFO is empty interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
12	CRC_RES_ERR	Indicate response CRC error interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
11	CRC_READ_ERR	Indicate CRC read error interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
10	CRC_WRITE_ERR	Indicate CRC write error interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
9	TIME_OUT_RES	Indicate response time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
8	TIME_OUT_READ	Indicate read time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RW
7	SDIO	Indicates whether the interrupt from SDIO is detected. 0: The interrupt from SDIO is not detected 1: The interrupt from SDIO is detected	R
6	TXFIFO_WR_REQ	Transmit FIFO write request. Set if data FIFO becomes half	R

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		empty. (the number of words is < 8) 0: No Request for data Write to MSC_TXFIFO 1: Request for data write to MSC_TXFIFO	
5	RXFIFO_RD_REQ	Receive FIFO read request. Set if data FIFO becomes half full (the number of words is >= 8) or the entries in data FIFO are the last read data. 0: No Request for data read from MSC_RXFIFO 1: Request for data read from MSC_RXFIFO	R
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Indicates whether the command/response sequence has been finished. 0: The command/response sequence has not been finished 1: The command/response sequence has been finished Write 1 to clear.	WR
1	PRG_DONE	Indicates whether card has finished programming. 0: Card has not finished programming and is busy 1: Card has finished programming and is no longer busy Write 1 to clear.	WR
0	DATA_TRAN_DONE	Indicates whether data transfer is done. Note that for stream read/write, only when CMD12 (STOP_TRANS) has been sent, is this bit set. 0: Data transfer is not complete 1: Data transfer has completed or an error has occurred Write 1 to clear.	WR

36.4.12 MMC/SD Command Index Register (MSC_CMD)

MSC_CMD0 **0x1002102C**
MSC_CMD1 **0x1002202C**

Bit	7	6	5	4	3	2	1	0
	Reserved		CMD_INDEX					
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	CMD_INDEX	Specifies the command index to be executed.	WR

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36.4.13 MMC/SD Command Argument Register (MSC_ARG)

MSC_ARG0																														0x10021030	
MSC_ARG1																														0x10022030	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARG																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ARG	Specifies the argument for the current command.	WR

36.4.14 MMC/SD Response FIFO Register (MSC_RES)

The read-only MMC/SD Response FIFO register (RES_FIFO) holds the response sent back to the MMC/SD controller after every command. The size of this FIFO is 8 x 16-bit. The RES FIFO does not contain the 7-bit CRC for the response. The Status for CRC checking and response time-out status is in the status register, MSC_STAT.

The first halt-word read from the response FIFO is the most significant halt-word of the received response.

MSC_RES0															0x10021034	
MSC_RES1															0x10022034	
Bit								15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DATA															
RST								?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15:0	DATA	Contains the response to every command that is sent by the MMC/SD controller. The size of this FIFO register is 8 x 16-bit.	R

36.4.15 MMC/SD Receive Data FIFO Register (MSC_RXFIFO)

The MSC_RXFIFO is used to read the data from a card. It is read-only to the software, and is read on 32-bit boundary. The size of this FIFO is 16 x 32-bit.

MSC_RXFIFO0																														0x10021038	
MSC_RXFIFO1																														0x10022038	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
31:0	DATA	One word of read data. The size of this FIFO is 16 x 32-bit.	R

36.4.16 MMC/SD Transmit Data FIFO Register (MSC_TXFIFO)

The MSC_TXFIFO is used to write the data to a card. It is write-only to the software, and is written on 32-bit boundary. The size of this FIFO is 16 x 32-bit.

MSC_TXFIFO0 **0x1002103C**

MSC_TXFIFO1 **0x1002203C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	One word of write data. The size of this FIFO is 16 x 32-bit.	W

36.4.17 MMC/SD Low Power Mode Register (MSC_LPM)

The MSC_LPM is used to control whether MSC controller enters Low-Power Mode.

MSC_LPM0 **0x10021040**

MSC_LPM1 **0x10022040**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSPEED	Reserved																														LPM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	HSPEED	0: controller send CMD and data at clock falling 1: controller send CMD and data at clock rising	RW
30:1	Reserved	Writing has no effect, read as zero.	R
0	LPM	0 : Non –Low Power Mode 1: Low-Power Mode. Stop clock when card in idle (should be normally set to only MMC and SD cards. For SDIO cards, if interrupts must be detected, clock should not be stopped) When software sets the bit, MSC clock can auto be stopped. **NOTE:** when set the bit, the start_clock and stop clock can be not use.	RW

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36.5 MMC/SD Functional Description

All communication between system and cards is controlled by the MSC. The MSC sends commands of two type: broadcast and addressed (point-to-point) commands.

Broadcast commands are intended for all cards, command like “Go_Idle_State”, “Send_Op_Cond”, “All_send_CID” and “Set_relative_Addr” are using way of broadcasting. During Broadcast mode, all cards are in open-drain mode, to avoid bus contention.

After Broadcast commands “Set_relative_Addr” issue, cards are enter standby mode, and Addressed command will be used from now on, in this mode, CMD/DAT will return to push-pull mode, to have maximum driving for maximum operation frequency.

The MMC and the SD are similar product. Besides the 4x bandwidth and the built-in encryption, they are being programmed similarly.

The MMC/SD controller (MSC) is the interface between the software and the MMC/SD bus. It is responsible for the timing and protocol between the software and the MMC/SD bus. It consists of control and status registers, a 16-bit response FIFO that is 8 entries deep, and one 32-bit receive/transmit data FIFOs that are 16 entries deep. The registers and FIFOs are accessible by the software.

MSC also enable minimal data latency by buffering data and generating and checking CRCs.

36.5.1 MSC Reset

The MMC/SD controller (MSC) can be reset by a hardware reset or software reset. All registers and FIFO controls are set to their default values after any reset.

36.5.2 MSC Card Reset

The command Go_Idle_State, CMD0 is the software reset command for MMC and SD Memory Card, and sets each card into Idle State regardless of the current card state; while in SDIO card, CMD52 is used to write IO reset in CCCR. The cards are initialized with a default relative card address (RCA=0x0000) and with a default driver stage register setting (lowest speed, highest driving current capability).

36.5.3 Voltage Validation

All cards shall be able to establish communication with the host using any operation voltage in the maximal allowed voltage range specified in this standard. However, the support minimum and maximum values for Vdd are defined in Operation Conditions register (OCR) and many not cover the whole range. Cards that store the CID and CSD data in the payload memory would be able to communicate these information only under data transfer Vdd conditions. That means if host and card

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have non compatible Vdd ranges, the card will not be able to complete the identification cycle, nor to send CSD data.

Therefore, a special command Send_Op_cont (CMD1 for MMC), SD_Send_Op_Cont (CMD41 for SD Memory) and IO_Send_Op_Cont (CMD5 for SDIO) are designed to provide a mechanism to identify and reject cards which do not match the Vdd range desired by the host. This is accomplished by the host sending the required Vdd voltage window as the operand of this command. Cards which can not perform data transfer in the specified range must discard themselves from further bus operations and go into Inactive State. By omitting the voltage range in the command, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State. This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired.

36.5.4 Card Registry

Card registry on MCC and SD card are different.

For SD card, Identification process start at clock rate Fod, while CMD line output drives are push-pull drivers instead of open-drain. After the bus is activated the host will request the cards to send their valid operation conditions. The response to ACMD41 is the operation condition register of the card. The same command shall be send to all of the new cards in the system. Incompatible cards are sent into Inactive State. The host then issue the command All_Send_CID (CMD2) to each card and get its unique card identification (CID) number. Card that is unidentified, that is, which is in Ready State, send its CID number as the response. After the CID was sent by the card it goes into Identification State. Thereafter, the host issues Send_Relative_Addr (CMD3) asks the card to publish a new relative card address (RCA), which is shorter that CID and which will be used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the Stand-by State. At this point, if the host wants that the card will have another RCA number, it may ask the card to publish a new number by sending another Send_Relative_Addr command to the card. The last published RCA is the actual RCA of the card. The host repeats the identification process, that is, the cycles with CMD2 and CMD3 for each card in the system.

In MMC, the host starts the card identification process in open-drain mode with the identification clock rate Fod. The open drain driver stages on the CMD line allow parallel card operation during card identification. After the bus is active the host will request the cards to send their valid operation conditions (CMD1). The response to CMD1 is the ‘wired or’ operation on the condition restrictions of all cards in the system. Incompatible cards are sent into Inactive State. The host then issues the broadcast command All_Send_CID (CMD2), asking all cards for their unique card identification (CID) number. All unidentified cards, that is, those which are in Ready State, simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bitstream. Those cards, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods stop sending their CID immediately and must wait for the next identification cycle. Since CID is unique for each card, only one card can be successfully send its full CID to the host. This card then

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goes into Identification State. Thereafter, the host issues Set_Relative_Addr (CMD3) to assign to this card a relative card address (RCA). Once the RCA is received the card state changes to the Stand-by State, and the card does not react to further identification cycles, and its output switches from open-drain to push-pull. The host repeat the process, which is CM2 and CMD3, until the host receive time-out condition to recognize completion of the identification process.

36.5.5 Card Access

36.5.5.1 Block Access, Block Write and Block Read

During block write (CMD24-27) one or more blocks of data are transferred from the host to the card with a CRC appended to the end of each block by the host. A card supporting block write shall always be able to accept a block of data defined by WRITE_BL_LEN. If the CRC fails, the card shall indicate the failure on the DAT line; the transferred data will be discarded and not written, and all further transmitted blocks (in multiple block write mode) will be ignored.

Programming of the CID and CSD registers does not require a previous block length setting. The transferred data is also CRC protected. If a part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents. Some cards may require long and unpredictable times to write a block of data. After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the card with a SEND_STATUS command (CMD13) at any time, and the card will respond with its status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether the write process is still in progress). The host may deselect the card by issuing CMD7 (to select a different card) which will displace the card into the Disconnect State and release the DAT line without interrupting the write operation. When reselecting the card, it will reactivate busy indication by pulling DAT to low if programming is still in progress and the write buffer is unavailable.

Block read is similar to stream read, except the basic unit of data transfer is a block whose maximizes is defined in the CSD (READ_BL_LEN). If READ_BL_PARTIAL is set, smaller blocks whose starting and ending address are entirely contained within one physical block (as defined by READ_BL_LEN) may also be transmitted. Unlike stream read, a CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the Transfer state. CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a stop command is issued. If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed, the card shall detect a block misalignment at the beginning of the first mis-aligned block, set the ADDRESS_ERROR error bit in the status register, abort transmission and wait in the Data State for a stop command.

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36.5.5.2 Stream Access, Stream Write and Stream Read (MMC Only)

Stream write (CMD20) starts the data transfer from the host to the card beginning from the starting address until the host issues a stop command. Since the amount of data to be transferred is not determined in advance, CRC can not be used. If the end of the memory range is reached while sending data and no stop command has been sent by the host, all further transferred data is discarded.

There is a stream oriented data transfer controlled by READ_DAT_UNTIL_STOP (CMD11). This command instructs the card to send its payload, starting at a specified address, until the host sends a STOP_TRANSMISSION command (CMD12). The stop command has execution delay due to the serial command transmission. The data transfer stops after the end bit of the stop command. If the end of the memory range is reached while sending data and no stop command has been sent yet by the host, the contents of the further transferred payload is undefined.

36.5.5.3 Erase, Group Erase and Sector Erase (MMC Only)

It is desirable to erase many sectors simultaneously in order to enhance the data throughput. Identification of these sectors is accomplished with the TAG_* commands. Either an arbitrary set of sectors within a single erase group, or an arbitrary selection of erase groups may be erase at one time, but not both together. That is, the unit of measure for determining an erase is either a sector or an erase group. If a set of sectors must be erased, all selected sectors must lie within the same erase group. To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all sectors (or groups) within this range will be selected for erase.

36.5.5.4 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected / deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width. ACMD6 command is valid in ‘trans state’ only. That means the bus width may be changed only after a card was selected (CMD7).

36.5.6 Protection Management

Three write protect methods are supported in the host for Cards, Card internal write protect (Card’s responsibility), Mechanical write protect switch (Host responsibility only) and Password protection card lock operation.

36.5.6.1 Card Internal Write Protection

Card data may be protected against either erase or write. The entire card may be permanently write protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. For cards which support write protection of groups of sectors by setting the WP_GRP_SIZE sectors as specified in the CSD), and the write protection may be changed by the application. The SET_WRITE_PROT command sets the write protection of the addressed

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write-protect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.

The SEND_WRITE_PROT command is similar to a single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The card will ignore all LSB's below the group size.

36.5.6.2 Mechanical write protect switch

A mechanical sliding tablet on the side of the card will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the window is open that means the card is write protected. If the window is close the card is not write protected.

A proper, matched, switch on the socket side will indicated to the host that the card is write protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is un-known to the internal circuitry of the card.

36.5.6.3 Password Protect

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size is kept in an 128-bit PWD and 8-bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.

Locked cards respond to (and execute) all commands in the basic command class (class 0) and "lock card" command class. Thus the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0) will be locked automatically after power on. Similar to the existing CSD and CID register write commands the lock/unlock command is available in "trans_state" only. This means that it does not include an address argument and the card must be selected before using it. The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). The following table describes the structure of the command data block.

Table 36-4 Command Data Block Structure

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Rsv	Rsv	Rsv	Rsv	ERASE	LOCK_UNLOCK	CLR_PWD	SET_PWD
1	PWDS_LEN							
2	Password Data							
…								

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PWDS_LEN + 1	

ERASE – 1 Defines Forced Erase Operation (all other bits shall be 0) and only the command byte is sent.

LOCK/UNLOCK – 1=Locks the card. 0=Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).

CLR_PWD – 1=Clears PWD.

SET_PWD – 1=Set new password to PWD.

PWD_LEN – Defines the following password length (in bytes).

PWD – The password (new or currently used depending on the command).

The data block size shall be defined by the host before it send the card lock/unlock command. This will allow different password sizes.

The following paragraphs define the various lock/unlock command sequences:

Lock command sequences:

1 Setting the Password.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8bit card lock/unlock mode, the 8 bits password size (in bytes), and the number of bytes of the new password. In case that a password replacement is done, then the block size shall consider that both passwords, the old and the new one, are sent with the command.

c Send Card Lock/Unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWD_LEN) and the password itself. In case that a password replacement is done, then the length value (PWD_LEN) shall include both passwords, the old and the new one, and the PWD field shall include the old password (currently used) followed by the new password.

d In case that the sent old password is not correct (not equal in size and content) then LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In case that PWD matches the sent old password then the given new password and its size will be saved in the PWD and PWD_LEN fields, respectively.

NOTE:

the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0 there is no password set. If the value of PWD_LEN is not equal to zero the card will lock itself after power up. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending additional command for card lock.

2 Reset the password.

a Select a card (CMD7), if not previously selected already.

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b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWD_LEN) and the password (PWD) itself (LOCK/UNLOCK bit is don't care). If the PWD and PWD_LEN is set to 0. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

3 Locking a card.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be locked and the card-locked status bit will be set in the status register. If the password is not correct then LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

it is possible to set the password and to lock the card in the same sequence. In such case the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent. If the password was previously set (PWD_LEN is not 0), then the card will be locked automatically after power on reset. An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register.

Unlock command sequences:

1 Unlocking the card.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be unlocked and the card-locked status bit will be cleared in the status register. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

the unlocking is done only for the current power session. As long as the PWD is not

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cleared the card will be locked automatically on the next power up. The only way to unlock the card is by clearing the password. An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

2 Forcing Erase.

In case that the user forgot the password (the PWD content) it is possible to erase all the card data content along with the PWD content. This operation is called Forced Erase.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16) to 1 byte (8bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including 16-bit CRC. The data block shall indicate the mode ERASE (the ERASE bit shall be the only bit set).

If the ERASE bit is not the only bit in the data field then the LCOK_UNLOCK_FAILED error bit will be set in the status register and the erase request is rejected. If the command was accepted then ALL THE CARD CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked card will get unlocked.

An attempt to force erase on an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

36.5.7 Card Status

The response format R1 contains a 32-bit field named card status. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command.

Table below defines the different entries of the status. The type and clear condition fields in the table are abbreviate as follows:

Type:

E: Error bit.

S: Status bit..

R: Detected and set for the actual command response.

X: Detected and set during command execution. The host must poll the card by issuing the status command in order to read these bits.

Clear Condition:

A: According to the card current state.

B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).

C: Clear by read.

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Table 36-5 Card Status Description

Bits	Identifier	Type	Description	Clear Condition
31	OUT_OF_RAGE	E R	The command's argument was out of the allowed range for this card. 0: No Error 1: Error	C
30	ADDRESS_ERROR	E R X	A misaligned address which did not match the block length was used in the command. 0: No Error 1: Error	C
29	BLOCK_LEN_ERROR	E R	The transferred block length is not allowed for this, or the number of transferred bytes does not match the block length. 0: No Error 1: Error	C
28	ERASE_SEQ_ERROR	E R	An error in the sequence of erase commands occurred. 0: No Error 1: Error	C
27	ERASE_PARAM	E X	An invalid selection of sectors or groups for erase occurred. 0: No Error 1: Error	C
26	WP_VIOLATION	E R X	Attempt to program a write protected block. 0: No Protected 1: Protected	C
25	CARD_IS_LOCKED	S X	When set, signals that the card is locked by the host. 0: Card unlocked 1: Card locked	A
24	LOCK_UNLOCK_FAILED	E R X	Set when a sequence or password error has been detected in lock/unlock card command or if there was an attempt to access a locked card. 0: No Error 1: Error	C

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23	COM_CRC_ERROR	E R	The CRC check of the previous command failed. 0: No Error 1: Error	B
22	ILLEGAL_COMMAND	E R	Command not legal for the card state. 0: No Error 1: Error	B
21	CARD_ECC_FAILED	E X	Card internal ECC was applied but failed to correct the data. 0: normal 1: failure	C
20	CC_ERROR	E R X	Internal card controller error. 0: No Error 1: Error	C
19	ERROR	E R X	A general or an unknown error occurred during the operation. 0: No Error 1: Error	C
18	UNDERRUN	E X	The card could not sustain data transfer in stream read mode. 0: No Error 1: Error	C
17	OVERRUN	E X	The card could not sustain data programming in stream write mode. 0: No Error 1: Error	C
16	CID/CSD_OVERWRITE	E R X	Can be either one of the following errors. 0: No Error 1: Error	C
15	WP_ERASE_SKIP	S X	Only partial address space was erased due to existing write protected blocks. 0: No Protected 1 : Protected	C
14	CARD_ECC_DISABLED	S X	The command has been executed without using the internal ECC. 0: enabled 1: disabled	A

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13	ERASE_RESET	S R	An erase sequence was cleared before executing because an out of erase sequence command was received. 0: normal 1: set	C
12:9	CURRENT_STATE	S X	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as binary coded number between 0 and 15. 0: idle 1: ready 2: ident 3: stby 4: tran 5: data 6: rcv 7: prg 8 : dis (9 – 15) : rsv	B
8	READY_FOR_DATA	S X	Corresponds to buffer empty signaling on the bus. 0: No Ready 1: Ready	A
7:6	Reserved	-	-	-
5	APP_CMD	S R	The card will expect ACMD, or indication that the command has been interpreted as ACMD. 0: Disable 1: Enable	C
4:0	Reserved	-	-	-

36.5.8 SD Status

The SD status contains status bits that are related to the SD card proprietary features and may be used for future application specific usage. The size of the SD status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16-bit CRC. The SD status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran_state' (card is selected). SD status structure is described in below.

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The same abbreviation for *type* and *clear condition* were used as for the Card Status above.

Table 36-6 SD Status Structure

Bits	Identifier	Type	Description	Clear Condition
511:510	DAT_BUS_WIDTH	S R	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command. 00: 1 (default) 01: Reserved 10: 4 bit width 11: Reserved	A
509	SECURED_MODE	S R	Card is in Secured Mode of operation. 0: Not in the Mode 10: In the mode	A
508:496	Reserved.			
495:480	SD_CARD_TYPE	S R	All 0, is SD Memory cards.	A
479:448	SIZE_OF_PROTECTED_AREA	S R	Size of protected area.	A
447:312	Reserved.			
311:0	Reserved for manufacturer.			

36.5.9 SDIO

I/O access differs from memory in that the registers can be written and read individually and directly without a FAT file structure or the concept of blocks (although block access is supported). These registers allow access to the IO data, control of the IO function, and report on status or transfer I/O data to and from the host.

Each SDIO card may have from 1 to 7 functions plus one memory function built into it. A function is a self contained I/O device. I/O functions may be identical or completely different from each other. All I/O functions are organized as a collection of registers, and there is a maximum of 131,072 registers possible for each I/O function.

36.5.9.1 SDIO Interrupts

In order to allow the SDIO card to interrupt the host, and interrupt function is added to a pin on the SD interface. Pin number 8 which is used as DAT[1] when operating in the 4 bit SD mode is used to signal the card's interrupt to the host. The use of interrupt is optional for each card or function within a card. The SDIO interrupt is "level sensitive", that is, the interrupt line must be held active (low) until it is either recognized and acted upon by the host or de-asserted due to the end of the Interrupt Period.

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Once the host has serviced the interrupt, it is cleared via an IO write to the appropriate bit in the CCCR. The interrupt output of all SDIO cards is active low. This host controller provides pull-up resistors on all data lines DAT[3:0].

As Pin 8 of the card is shared between the IRQ and DAT[1] use in the 4 bit SD mode, and interrupt shall only be sent by the card and recognized by the host during a specific time. The time that a low on Pin 8 will be recognized as an interrupt is defined as the Interrupt Period.

The host here will only sample the level of Pin 8 (DAT[1]/IRQ) into the interrupt detector during the Interrupt Period. At all other times, the host will ignore the level on Pin 8. Note that the Interrupt Period is applicable for both memory and IO operations. The definition of the Interrupt Period is different for operations with single block and multiple block data transfer.

36.5.9.2 SDIO Suspend/Resume

Within a multi-function SDIO or a Combo (Mix IO and Memory) card, there are multiple devices (I/O and memory) that must share access to the SD bus. In order to allow the sharing of access to the host among multiple devices, SDIO and combo cards can implement the optional concept of suspend/resume. In a card supports suspend/resume, the host may temporarily halt a data transfer operation to one function or memory (suspend) in order to free the bus for a higher priority transfer to a different function of memory. Once this higher-priority transfer is complete, the original transfer is re-started where it left off (resume). The host controller here is supported by all IO functions except zero, and the memory of a combo card, and can suspend multiple transactions and resume them in any order desired. IO function zero does not support suspend/resume.

The procedure used to perform the Suspend/Resume operation on the SD bus is:

- The host determines which function currently used the DAT[] line(s).
- The host requests the lower priority or slower transaction to suspend.
- The host checks for the transaction suspension to complete.
- The host begins the higher priority transaction.
- The host waits for the completion of the higher priority transaction.
- The host restores the suspended transaction.

36.5.9.3 SDIO Read Wait

The optional Read Wait (RW) operation is defined only for the SD 1-bit and 4-bit modes. The read wait operation allows a host to signal a card that it is doing a read multiple (CMD53) operation to temporarily stall the data transfer while allowing the host to send commands to any function within the SDIO device. To determine if a card supports the Read Wait protocol, the host must test capability bits in CCCR. The timing for Read Wait is base on the Interrupt Period.

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36.5.10 Clock Control

The software should guarantee that the card identification process starts in open-drain mode with the clock rate fod (0 ~ 400khz). In addition, the software should also make the card into interrupt mode with fod (only for MMC). The commands that require fod are CMD0, CMD1, CMD2, CMD3, CMD5, CMD40 and ACMD41. In data transfer mode, the MSC controller can operate card with clock rate fpp (0 ~ 25Mhz).

36.5.11 Application Specified Command Handling

The MultiMediaCard/SD system is designed to provide a standard interface for a variety applications types. In this environment it is anticipate that there will be a need for specific customers/applications features. To enable a common way of implementing these features, two types of generic commands are defined in the standard: Application Specific Command, ACMD, and General Command, GEN_CMD.

GEN_CMD, this command, when received by the card, will cause the card to interpret the following command as an application specific command, ACMD. The ACMD has the same structure as of regular MultiMediaCard standard commands and it may have the same CMD number. The card will recognize it as ACMD by the fact that it appears after APP_CMD.

The only effect of the APP_CMD is that if the command index of the, immediately, following command has an ACMD overloading, the none standard version will used. If, as an example, a card has a definition for ACMD13 but not for ACMD7 then, if received immediately after APP_CMD command, Command 13 will be interpreted as the non standard ACMD13 but, command 7 as the standard CMD7.

In order to use one of the manufacturer specific ACMD's the host will:

1 Send APP_CMD. The response will have the APP_CMD bit (new status bit) set signaling to the host that ACMD is now expected.
2 Send the required ACMD. The response will have the APP_CMD bit set, indicating that the accepted command was interpreted as ACMD. If a non-ACMD is sent then it will be respected by the card as normal MultiMediaCard command and the APP_CMD bit in the Card Status stays clear.

If a non valid command is sent (neither ACMD nor CMD) then it will be handled as a standard MultiMediaCard illegal command error.
The bus transaction of the GEN_CMD is the same as the single block read or write commands (CMD24 or CMD17). The difference is that the argument denotes the direction of the data transfer (rather than the address) and the data block is not a memory payload data but has a vendor specific format and meaning.
The card shall be selected ('tran_state') before sending CMD56. The data block size is the BLOCK_LEN that was defined with CMD16. The response to CMD56 will be R1b (card status + busy indication).

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36.6 MMC/SD Controller Operation

36.6.1 Data FIFOs

The controller FIFOs for the response tokens, received data, and transmitted data are MSC_RES, MSC_RXFIFO, and MSC_TXFIFO, respectively. These FIFOs are accessible by the software and are described in the following paragraphs.

36.6.1.1 Response FIFO (MSC_RES)

The response FIFO, MSC_RES, contains the response received from an MMC/SD card after a command is sent from the controller. MSC_RES is a read-only, 16-bit, and 8-entry deep FIFO.

The FIFO will hold all possible response lengths. Responses that are only one byte long are located on the LSB of the 16-bit entry in the FIFO. The first half-word read from the response FIFO is the most significant half-word of the received response. For example, if the response format is R1, then the response read from RES_FIFO is bit [47:32], bit[31:16], bit[15:0] and in the third half-word only the low 8-bit is effective response [15:8] and the high 8-bit is ignored. If the response format is R2, then the response read from MSC_RES is bit [135:8] and needs reading 8 times.

The FIFO does not contain the response CRC. The status of the CRC check is in the status register, MSC_STAT.

36.6.1.2 Receive/Transmit Data FIFO (MSC_RXFIFO/MSC_TXFIFO)

The receive data FIFO and transmit data FIFO share one 16-entry x 32-bit FIFO, because at one time data are only received or are only transmitted. If it is used to receive data, it is called MSC_RXFIFO and read-only. If it is used to transmit data, it is called MSC_TXFIFO and write-only.

Data FIFO and its controls are cleared to a starting state after a system reset or at the beginning of the operations which include data transfer. (MSC_CMDAT[DATA_EN] == 1)

If at any time MSC_RXFIFO becomes full and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any overflows. When the clock is off, data transmission from the card stops until the clock is turned back on. After MSC_RXFIFO is not full, the controller turns the clock on to continue data transmission. The full status of the FIFO is registered in the MSC_STAT [DATA_FIFO_FULL] bit.

If at any time MSC_TXFIFO becomes empty and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any underrun. When the clock is off, data transmission to the card stops until the clock is turned back on. When MSC_TXFIFO is no longer empty, the controller automatically restarts the clock. The empty status of the FIFO is registered in the MSC_STAT [DATA_FIFO_EMPTY] bit.

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The FIFO is readable on word (32-bit) boundaries. The max read/written number is 16 words. The controller can correctly process big-endian and little-endian data.

Because at the beginning of the operation which include data transfer (MSC_CMDAT [DATA_EN] == 1), Data FIFO and its controls are cleared, software should guarantee data in FIFO have been read/written before beginning a new command.

36.6.2 DMA and Program I/O

Software may communicate to the MMC controller via the DMA or program I/O.

To access MSC_RXFIFO/MSC_TXFIFO with the DMA, the software must program the DMA to read or write the FIFO with source port width 32-bit, destination port width 32-bit, transfer data size 32-byte, transfer mode single. For example, to write 64 bytes of data to the MSC_TXFIFO, the software must program the DMA as follows:

```
DMA_DCTRn = 2                // Write 2 32-bytes (64 bytes)
DMA_DCCRn[SWDH] = 0          // source port width is 32-bit
DMA_DCCRn[DWDH] = 0          // destination port width is 32-bit
DMA_DCCRn[DS] = 4            // transfer data size is 32-byte
DMA_DCCRn[TM] = 4            // transfer mode is single
DMA_DCCRn[RDIL] = 0          // request detection interval length is 0
```

The number of 32-bytes should be calculated from the number of transferred bytes as follows:

The number of words = (The number of bytes + 31) / 32

If the number of transferred bytes is not the multiple of 4, the controller can correctly process endian.

The DMA trigger level is 8 words, that is to say, the DMA read trigger is when data words in MSC_RXFIFO is >= 8 and the DMA write trigger is when data words in MSC_TXFIFO is < 8. Software can also configure DMA registers based on requirements, but the above 32-byte transfer data size is most efficient.

With program I/O, the software waits for the MSC_IREG [RXFIFO_RD_REQ] or MSC_IREG [TXFIFO_WR_REQ] interrupts before reading or writing the respective FIFO.

NOTES:

1 The MSC_CMDAT [DMA_EN] bit must be set to a 1 to enable communication with the DMA and it must be set to a 0 to enable program I/O.

2 DMA can be enabled only after MSC_CMDAT is written, because MSC_CMDAT [DATA_EN] is used to reset TX/RXFIFO.

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36.6.3 Start and Stop clock

The software stops the clock as follows:

1 Write MSC_STRPCL with 0x01 to stop the MMC/SD bus clock.
2 Wait until MSC_STAT[CLK_EN] becomes zero.

To start the clock the software writes MSC_STRPCL with 0x02.

36.6.4 Software Reset

Reset includes the MSC reset and the card reset.

The MSC reset is through MSC_STRPCL [RESET] bit.

The card reset is to make the card into idle state. CMD0 (GO_IDLE_STATE) sets the MMC and SD memory cards into idle state. CMD52 (IO_RW_DIRECT, with argument 0x88000C08) reset the SD I/O card. The MMC/SD card are initialized with a default relative card address (RCA = 0x0001 for MMC and RCA = 0x0000 for SD) and with a default driver stage register setting (lowest speed, highest driving current capability).

The following registers must be set before the clock is started:

Step 1. Stop the clock.
Step 2. Set MSC_STRPCL register to 0x08 to reset MSC.
Step 3. Wait while MSC_STAT [IS_RESETTING] is 1.
Step 4. Set MSC_CMD with CMD0.
Step 5. Update the MSC_CMDAT register as follows:
  a Write 0x0000 to MSC_CMDAT [RESPONSE_FORMAT].
  b Clear the MSC_CMDAT [DATA_EN] bit.
  c Clear the MSC_CMDAT [BUSY] bit.
  d Clear the MSC_CMDAT [INIT] bit.
Step 6. Start the clock.
Step 7. Start the operation. (write MSC_STRPCL with 0x04)
Step 8. Wait for the END_CMD_RES interrupt.
Step 9. Set MSC_CMD with CMD52.
Step 10. Set MSC_ARG with 0x88000C08.
Step 11. Update the MSC_CMDAT register as follows:
  a Write 0x005 to MSC_CMDAT [RESPONSE_FORMAT].
  b Clear the MSC_CMDAT [DATA_EN] bit.
  c Clear the MSC_CMDAT [BUSY] bit.
  d Clear the MSC_CMDAT [INIT] bit.
Step 12. Start the operation.
Step 13. Wait for the END_CMD_RES interrupt.

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36.6.5 Voltage Validation and Card Registry

At most 10 MMC and 1 SD (either SDMEM or SDIO) can be inserted MMC/SD bus at the same time, and their voltage validation and card registry steps are different, so the software should be programmed as follows:

Step 1. Check whether SDIO card is inserted.
Step 2. Check whether SDMEM card is inserted.
Step 3. Check whether MMC cards are inserted.

36.6.5.1 Check SDIO

The commands are sent as follows:

Step 1. (Optional) Send CMD52 (IO_RW_DIRECT) with argument 0x88000C08 to reset SDIO card.
Step 2. Send CMD5 (IO_SEND_OP_CMD) to validate voltage.
Step 3. If the response is correct and the number of IO functions > 0, then continue, else go to check SDMEM.
Step 4. If C-bit in the response is ready (the initialization has finished), go to 6.
Step 5. Send CMD5 (IO_SEND_OP_CMD) to validate voltage, then go to 4.
Step 6. If memory-present-bit in the response is true, then it is a combo card (SDIO + Memory), else it is only a SDIO card.
Step 7. If it is a combo card, go to check SDMEM to initialize the memory part.
Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let the card publish a RCA. The RCA is returned from the response.
Step 9. If do not accept the new RCA, go to 8, else record the new RCA.
Step 10. Go to check MMC, because we can assure that there is no SDMEM card.

36.6.5.2 Check SDMEM

If there is no SDIO card or there is a combo card, continue to check SDMEM.

The commands are sent as follows:

Step 1. (Optional) Send CMD0 (GO_IDLE_STATE) to reset MMC and SDMEM card. This command has no response.
Step 2. Send CMD55. Here the default RCA 0x0000 is used for CMD55.
Step 3. If the response is correct (CMD55 has response), then continue, else go to check MMC.
Step 4. Send ACMD41 (SD_SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF8000).
Step 5. If the initialization has finished, go to 7. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)
Step 6. Send CMD55 and ACMD41 to validate voltage, and then go to 5.
Step 7. Send CMD2 (ALL_SEND_CID) to get the card CID.
Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let card publish a RCA. The RCA is returned

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from the response.

Step 9. If do not accept the new RCA, go to 8, else record the new RCA.

Step 10. Go to check MMC.

36.6.5.3 Check MMC

Because there may be several MMC card, so some steps (5 ~ 8) should be repeated several times.

The commands are sent as follows:

Step 1. Send CMD1 (SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF88000).

Step 2. If the response is correct, then continue, else goto 9.

Step 3. If the initialization has finished, go to 5. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)

Step 4. Send CMD1 (SEND_OP_CMD) to validate voltage, and then go to 3.

Step 5. Send CMD2 (ALL_SEND_CID) to get the card CID.

Step 6. If the response timeout occurs, goto 9.

Step 7. Send CMD3 (SET_RELATIVE_ADDR) to assign the card a RCA.

Step 8. If there are other MMC cards, then go to 5.

Step 9. Finish.

36.6.6 Single Data Block Write

In a single block write command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.

Step 2. Set MSC_BLKLEN to the number of bytes per block.

Step 3. Update the MSC_CMDAT register as follows:

a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].

b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.

c Set the MSC_CMDAT [DATA_EN] bit.

d Set the MSC_CMDAT [WRITE_READ] bit.

e Clear the MSC_CMDAT [STREAM_BLOCK] bit.

f Clear the MSC_CMDAT [BUSY] bit.

g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.

Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IREG [END_CMD_RES] interrupt.

Step 2. Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.

At the same time write data to the MSC_TXFIFO and continue until all of the data have been written to the FIFO.

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Step 3. Wait for MSC_IREG [PROG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.

Step 4. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

To address a different card, the software sends a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IREG [PROG_DONE] interrupt. This ensures that the card is not in the busy state.

In addition, CMD26 (PROGRAM_CID), CMD27 (PROGRAM_CSD), CMD42 (LOCK/UNLOCK), CMD56 (GEN_CMD: write) and CMD53 (single_block_write) operations are similar to single block write.

36.6.7 Single Block Read

In a single block read command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.

Step 2. Set MSC_BLKLEN register to the number of bytes per block.

Step 3. Update the following bits in the MSC_CMDAT register:

a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].

b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.

c Set the MSC_CMDAT [DATA_EN] bit.

d Clear the MSC_CMDAT [WRITE_READ] bit.

e Clear the MSC_CMDAT [STREAM_BLOCK] bit.

f Clear the MSC_CMDAT [BUSY] bit.

g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.

Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IREG [END_CMD_RES] interrupt.

Step 2. Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.

At the same time read data from the MSC_RXFIFO as data becomes available in the FIFO, and continue reading until all data is read from the FIFO.

Step 3. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

In addition, CMD30 (SEND_WRITE_PROT), ACMD13 (SD_STATUS), CMD56 (GEN_CMD-read), ACMD51 (SEND_SCR) and CMD53 (single_block_read) are similar to single block read.

36.6.8 Multiple Block Write

The multiple block write mode is similar to the single block write mode, except that multiple blocks of

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data are transferred. Each block is the same length. All the registers are set as they are for the single block write, except that the MSC_NOB register is set to the number of blocks to be written.

The multiple block write mode also requires a stop transmission command, CMD12, after the data is transferred to the card. After the MSC_IREG [DATA_TRAN_DONE] interrupt occurs, the software must program the controller register to send a stop data transmission command.

If multiple block write with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple_block_write) is also similar, but when IO abort (CMD52) is sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 36-7 How to stop multiple block write

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After write MSC_NOB blocks	1 Wait for DATA_TARN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort) 3 Wait for END_CMD_RES and PRG_DONE interrupt.
Open-ended or SDIO infinite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_STRPCL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.
Predefined block or SDIO finite	After writing MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_STRPCL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.

36.6.9 Multiple Block Read

The multiple blocks read mode is similar to the single block read mode, except that multiple blocks of data are transferred. Each block is the same length. All the registers are set as they are for the single block read, except that the MSC_NOB register is set to the number of blocks to be read.

The multiple blocks read mode requires a stop transmission command, CMD12, after the data from the card is received. After the MSC_IREG [DATA_TRAN_DONE] interrupt has occurred, the software must program the controller registers to send a stop data transmission command.

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If multiple block read with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple_block_read) is also similar, but when IO abort (CMD52) is sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 36-8 How to stop multiple block read

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort) 3 Wait for END_CMD_RES interrupt.
Open-ended or SDIO infinite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_STRPCL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.
Predefined block or SDIO finite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_STRPCL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.

36.6.10 Stream Write (MMC)

In a stream write command, the following registers must be set before the operation is started:

1 Update MSC_CMDAT register as follows:
   a Write 0x001 to the MSC_CMDAT [RESPONSE_FORMAT].
   b Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream write.
   c Set the MSC_CMDAT [DATA_EN] bit.
   d Set the MSC_CMDAT [WRITE_READ] bit.
   e Set the MSC_CMDAT [STREAM_BLOCK] bit.
   f Clear the MSC_CMDAT [BUSY] bit.
   g Clear the MSC_CMDAT [INIT] bit.
2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1 Wait for the MSC_IREG [END_CMD_RES] interrupt.
2 Write data to the MSC_TXFIFO and continue until all of the data is written to the Data FIFO.
3 Stop clock. Wait until MSC_STAT[CLK_EN] becomes 0. The clock must be stopped.
4 Set the command registers for a stop transaction command (CMD12) and other registers.
5 Start the clock and start the operation.

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6 Wait for the MSC_IREG [END_CMD_ERS] interrupt.
7 Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.
8 Wait for the MSC_IREG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.
9 Read the MSC_STAT register to verify the status of the transaction.

To address a different card, the software must send a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IREG [PRG_DONE] interrupt. This ensures that the card is not in the busy state.

If partial blocks are allowed (if CSD parameter WRITE_BL_PARTIAL is set) the data stream can start and stop at any address within the card address space, otherwise it shall start and stop only at block boundaries. If WRITE_BL_PARTIAL is not set, 16 more stuff bytes need to be written after the useful written data, otherwise only write the useful written data.

36.6.11 Stream Read (MMC)

In a stream read command, the following registers must be set before the operation is turned on:

1 Update the MSC_CMDAT register as follows:
  a Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].
  b Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream read.
  c Clear the MSC_CMDAT [WRITE_READ] bit.
  d Set the MSC_CMDAT [STREAM_BLOCK] bit.
  e Clear the MSC_CMDAT [BUSY] bit.
  f Clear the MSC_CMDAT [INIT] bit.
2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1 Wait for the MSC_IREG [END_CMD_RES] interrupt.
2 Read data from the MSC_RXFIFO and continue until all of the expected data has been read from the FIFO.
3 Write MSC_STRPCL [EXIT_TRANSER] with 1. If MSC_STAT[DATA_FIFO_FULL] is 1, then read MSC_RXFIFO to make it not full. Because if data FIFO is full, MSC_CLK is stopped. Here, the data FIFO contains useless data.
4 Set the command registers for a stop transaction command (CMD12) and send it. There is no need to stop the clock.
5 Wait for the MSC_IREG [END_CMD_RES].
6 Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.
7 Read the MSC_STAT register to verify the status of the transaction.

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36.6.12 Erase, Select/Deselect and Stop

For CMD7 (SELECT/DESELECT_CARD), CMD12 (STOP_TRANSMISSION) and CMD38 (ERASE), the following registers must be set before the operation is started:

1 Update the MSC_CMDAT register as follows:
   a Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].
   b Clear the MSC_CMDAT [DATA_EN] bit.
   c Clear the MSC_CMDAT [WRITE_READ] bit.
   d Clear the MSC_CMDAT [STREAM_BLOCK] bit.
   e Set the MSC_CMDAT [BUSY] bit.
   f Clear the MSC_CMDAT [INIT] bit.
2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1 Wait for the MSC_IREG [END_CMD_RES] interrupt.
2 Wait for the MSC_IREG [PRG_DONE] interrupt. If CMD12 is sent to terminate data read operation, then there is no need to wait for MSC_IREG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.

36.6.13 SDIO Suspend/Resume

The actual suspend/resume steps are as follows:

1 During data transfer, send CMD52 to require suspend. BR and RAW flag should be 1.
2 If BS flag in the response is 0, then suspend has been accepted and goto 4.
3 Send CMD52 to query card status. R flag should be 1. Go to 2.
4 Write MSC_STRPCL [EXIT_TRANSFER] with 1.
5 Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.
6 Read MSC_NOB, MSC_SNOB and etc, save them into variables.
7 Set registers for high priority transfer and start it.
8 Wait until high priority transfer is finished.
9 Restore registers from variables, but MSC_NOB should be (MSC_NOB – MSC_SNOB).
10 Send CMD52 to require resume. FSx should be resumed function number.

36.6.14 SDIO ReadWait

The actual ReadWait steps are as follows:

1 During multiple block read, read MSC_SNOB. If MSC_SNOB is nearby or equal to MSC_NOB, no need to use ReadWait.
2 Write MSC_STRPCL [START_READWAIT] with 1.
3 Wait until MSC_STAT [IS_READWAIT] becomes 1.
4 Send CMD52 to query card status.
5 Write MSC_STRPCL [STOP_READWAIT] with 1.

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36.6.15 Operation and Interrupt

The software can use polling-status method to operate the MMC/SD card, but this is not the proposed method, because its performance is very low. The proposed method is to use interrupt. Generally there are fixed necessary steps to finish each command. The steps are as follows:

1 (Optional) Stop clock. Poll CLK_EN.
2 Fill the registers (MSC_CMD, MSC_CMDAT, MSC_ARG, MSC_CLKRT, and etc).
3 (Optional) Start clock.
4 Start the operation. Wait for the MSC_IREG [END_CMD_RES] interrupt.
5 Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.
6 Send STOP_TRANS (CMD12) or I/O abort (CMD52). Wait for the MSC_IREG [END_CMD_ERS] interrupt.
7 Wait for the MSC_IREG [DATA_TRAN_DONE] interrupt.
8 Wait for the MSC_IREG [PRG_DONE] interrupt.

Table 36-9 The mapping between Commands and Steps

Index	Abbreviation	1	2	3	4	5	6	7	8	Comments
CMD0	GO_IDLE_STATE	Y	Y	Y	Y					
CMD1	SEND_OP_COND	Y	Y	Y	Y					
CMD2	ALL_SEND_CID	Y	Y	Y	Y					
CMD3	SET_RELATIVE_ADDR	Y	Y	Y	Y					
CMD4	SET_DSR	Y	Y	Y	Y					
CMD7	SELECT/DSELECT_CARD	Y	Y	Y	Y				Y	
CMD9	SEND_CID	Y	Y	Y	Y					
CMD10	SEND_CSD	Y	Y	Y	Y					
CMD11	READ_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y		
CMD12	STOP_TRANSMISSION	Y	Y	Y	Y				Y	
CMD13	SEND_STATUS	Y	Y	Y	Y					
CMD15	GO_INACTIVE_STATE	Y	Y	Y	Y					
CMD16	SET_BLOCKLEN	Y	Y	Y	Y					
CMD17	READ_SINGLE_BLOCK	Y	Y	Y	Y	Y				
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y			Open-ended
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y				Predefine blocks
CMD20	WRITE_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y	Y	
CMD23	SET_BLOCK_COUNT	Y	Y	Y	Y					
CMD24	WRITE_SINGLE_BLOCK	Y	Y	Y	Y	Y			Y	
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y		Y	Open-ended
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y			Y	Predefine blocks
CMD26	PROGRAM_CID	Y	Y	Y	Y	Y			Y	
CMD27	PROGRAM_CSD	Y	Y	Y	Y	Y			Y	

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CMD28	SET_WRITE_PROT	Y	Y	Y	Y				Y	
CMD29	CLR_WRITE_PROT	Y	Y	Y	Y				Y	
CMD30	SEND_WRITE_PROT	Y	Y	Y	Y	Y				
CMD32	ERASE_WR_BLOCK_START	Y	Y	Y	Y					
CMD33	ERASE_WR_BLOCK_END	Y	Y	Y	Y					
CMD35	ERASE_GROUP_START	Y	Y	Y	Y					
CMD36	ERASE_GROUP_END	Y	Y	Y	Y					
CMD38	ERASE	Y	Y	Y	Y				Y	
CMD39	FAST_IO	Y	Y	Y	Y					
CMD40	GO_IRQ_STATE	Y	Y	Y	Y					
CMD42	LOCK/UNLOCK	Y	Y	Y	Y	Y			Y	
CMD55	APP_CMD	Y	Y	Y	Y					
CMD56	GEN_CMD	Y	Y	Y	Y	Y				Read
CMD56	GEN_CMD	Y	Y	Y	Y	Y			Y	Write
ACMD6	SET_BUS_WIDTH	Y	Y	Y	Y					
ACMD13	SD_STATUS	Y	Y	Y	Y	Y				
ACMD22	SEND_NUM_WR_BLOCKS	Y	Y	Y	Y					
ACMD23	SET_WR_BLOCK_COUNT	Y	Y	Y	Y					
ACMD41	SD_SEND_OP_COND	Y	Y	Y	Y					
ACMD42	SET_CLR_CARD_DETECT	Y	Y	Y	Y					
ACMD51	SEND_SCR	Y	Y	Y	Y	Y				

NOTE: For stream read/write, STOP_CMD is sent after finishing data transfer. For write, STOP_CMD is with the last six bytes. For read, STOP_CMD is sent after receiving data and card sends some data which MSC ignores.

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37 UART Interface

37.1 Overview

This chapter describes the universal asynchronous receiver/transmitter (UART) serial ports. There are three UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550-industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

37.1.1 Features

- Full-duplex operation
- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 32x8 bit transmit FIFO and 32x11bit receive FIFO
- Independently controlled transmit, receive (data ready or timeout), line status interrupts
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

37.1.2 Pin Description

Table 37-1 UART Pins Description

Name	Type	Description
RxD	Input	Receive data input
TxD	Output	Transmit data output
CTS_	Input	Clear to Send — Modem Transmission enabled
RTS_	Output	Request to Send — UART Transmission request

NOTE: UART2, UART0 support RxD, TxD, RTS_, CTS_, UART1 supports only RxD, TxD.

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37.2 Register Descriptions

All UART register 32-bit access address is physical address. When ULCR.DLAB is 0, URBR, UTHR and UIER can be accessed; When ULCR.DLAB is 1, UDLLR and UDLHR can be accessed.

Table 37-2 UART Registers Description

Name	Description	RW	Reset Value	Address	Access Size
URBR0	UART Receive Buffer Register 0	R	0x??	0x10030000	8
UTHR0	UART Transmit Hold Register 0	W	0x??	0x10030000	8
UDLLR0	UART Divisor Latch Low Register 0	RW	0x00	0x10030000	8
UDLHR0	UART Divisor Latch High Register 0	RW	0x00	0x10030004	8
UIER0	UART Interrupt Enable Register 0	RW	0x00	0x10030004	8
UIIR0	UART Interrupt Identification Register 0	R	0x01	0x10030008	8
UFCR0	UART FIFO Control Register 0	W	0x00	0x10030008	8
ULCR0	UART Line Control Register 0	RW	0x00	0x1003000C	8
UMCR0	UART Modem Control Register 0	RW	0x00	0x10030010	8
ULSR0	UART Line Status Register 0	R	0x00	0x10030014	8
UMSR0	UART Modem Status Register 0	R	0x00	0x10030018	8
USPR0	UART Scratchpad Register 0	RW	0x00	0x1003001C	8
ISR0	Infrared Selection Register 0	RW	0x00	0x10030020	8
UMR0	UART M Register 0	RW	0x00	0x10030024	8
UACR0	UART Add Cycle Register 0	RW	0x00	0x10030028	16
URBR1	UART Receive Buffer Register 1	R	0x??	0x10031000	8
UTHR1	UART Transmit Hold Register 1	W	0x??	0x10031000	8
UDLLR1	UART Divisor Latch Low Register 1	RW	0x00	0x10031000	8
UDLHR1	UART Divisor Latch High Register 1	RW	0x00	0x10031004	8
UIER1	UART Interrupt Enable Register 1	RW	0x00	0x10031004	8
UIIR1	UART Interrupt Identification Register 1	R	0x01	0x10031008	8
UFCR1	UART FIFO Control Register 1	W	0x00	0x10031008	8
ULCR1	UART Line Control Register 1	RW	0x00	0x1003100C	8
UMCR1	UART Modem Control Register 1	RW	0x00	0x10031010	8
ULSR1	UART Line Status Register 1	R	0x00	0x10031014	8
UMSR1	UART Modem Status Register 1	R	0x00	0x10031018	8
USPR1	UART Scratchpad Register 1	RW	0x00	0x1003101C	8
ISR1	Infrared Selection Register 1	RW	0x00	0x10031020	8
UMR1	UART M Register 1	RW	0x00	0x10031024	8
UACR1	UART Add Cycle Register 1	RW	0x00	0x10031028	16
URBR2	UART Receive Buffer Register 2	R	0x??	0x10032000	8
UTHR2	UART Transmit Hold Register 2	W	0x??	0x10032000	8
UDLLR2	UART Divisor Latch Low Register 2	RW	0x00	0x10032000	8
UDLHR2	UART Divisor Latch High Register 2	RW	0x00	0x10032004	8

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UIER2	UART Interrupt Enable Register 2	RW	0x00	0x10032004	8
UIIR2	UART Interrupt Identification Register 2	R	0x01	0x10032008	8
UFCR2	UART FIFO Control Register 2	W	0x00	0x10032008	8
ULCR2	UART Line Control Register 2	RW	0x00	0x1003200C	8
UMCR2	UART Modem Control Register 2	RW	0x00	0x10032010	8
ULSR2	UART Line Status Register 2	R	0x00	0x10032014	8
UMSR2	UART Modem Status Register 2	R	0x00	0x10032018	8
USPR2	UART Scratchpad Register 2	RW	0x00	0x1003201C	8
ISR2	Infrared Selection Register 2	RW	0x00	0x10032020	8
UMR2	UART M Register 2	RW	0x00	0x10032024	8
UACR2	UART Add Cycle Register 2	RW	0x00	0x10032028	16

37.2.1 UART Receive Buffer Register (URBR)

The read-only URBR is corresponded to one level 11bit buffer in non-FIFO mode and a 32x11bit FIFO that holds the character(s) received by the UART. Bits in URBR are right justified when being configured to use fewer than eight bits, and the rest of most significant data bits are zeroed and the most significant three bits of each buffer are the status for the character in the buffer. If ULSR.DRY is 0, don't read URBR, otherwise wrong operation may occur.

URBR0, URBR1, URBR2 — **0x10030000, 0x10031000, 0x10032000 (DLAB = 0)**

Bit	7	6	5	4	3	2	1	0
	URBR							
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7:0	URBR	8-bit UART receive read data.	R

37.2.2 UART Transmit Hold Register (UTHR)

The write-only UTHR is corresponded to one leve 8 bit buffer in non-FIFO mode and a 32x8bit FIFO in FIFO mode that holds the data byte(s) to be transmitted next.

UTHR0, UTHR1, UTHR2 — **0x10030000, 0x10031000, 0x10032000 (DLAB = 0)**

Bit	7	6	5	4	3	2	1	0
	UTHR							
RST	?	?	?	?	?	?	?	?

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Bits	Name	Description	RW
7:0	UTHR	8-bit UART transmit write hold data.	W

37.2.3 UART Divisor Latch Low/High Register (UDLLR / UDLHR)

UART Divisor Latch registers, UDLLR/UDLHR together compose the divisor for the programmable baud rate generator that can take the UART device clock and divide it by 1 to (2^{16} – 1).

The UART device source clock is EXCLK or EXCLK/2 that is determined by CPCCR.ECS. UDLHR/UDLLR stores the high/low 8-bit of the divisor respectively. Load these divisor latches during initialization to ensure that the baud rate generator operates properly. If both Divisor Latch registers are 0, the 16X clock stops.

If you don't set UMR and UACR, UART will work at normal mode with the specified frequency. The relationship between baud rate and the value of Divisor is shown by the formula when UMR and UACR are not set:

Baud Rate = (UART device clock) / (16 * **Divisor**)

UDLLR0, UDLLR1, UDLLR2 — **0x10030000, 0x10031000, 0x10032000 (DLAB = 1)**

Bit	7	6	5	4	3	2	1	0
	Divisor Latch Low 8-bit							
RST	0	0	0	0	0	0	0	0

UDLHR0, UDLHR1, UDLHR2 — **0x10030004, 0x10031004, 0x10032004 (DLAB = 1)**

Bit	7	6	5	4	3	2	1	0
	Divisor Latch High 8-bit							
RST	0	0	0	0	0	0	0	0

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37.2.4 UART Interrupt Enable Register (UIER)

The UART Interrupt Enable Register (UIER) contains the interrupt enable bits for the five types of interrupts (receive data ready, timeout, line status, and transmit data request, and modem status) that set a value in UIIR.

UIER0, UIER1, UIER2 — **0x10030004, 0x100301004, 0x10032004 (DLAB = 0)**

Bit	7	6	5	4	3	2	1	0
	Reserved			RTOIE	MSIE	RLSIE	TDRIE	RDRIE
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	RTOIE	**Receive Timeout Interrupt Enable.** 0: Disable the receive timeout interrupt 1: Enable the receive timeout interrupt Timeout means the URDR (FIFO mode) is not empty but no character has received for a period of time T: T (bits) = 4 X Word length + 12.	RW
3	MSIE	**Modem Status Interrupt Enable.** 0: Disable the modem status interrupt 1: Enable the modem status interrupt	RW
2	RLSIE	**Receive Line Status Interrupt Enable.** 0: Disable receive line status interrupt 1: Enable receive line status interrupt	RW
1	TDRIE	**Transmit Data Request Interrupt Enable.** 0: Disable the transmit data request interrupt 1: Enable the transmit data request interrupt	RW
0	RDRIE	**Receive Data Ready Interrupt Enable.** 0: Disable the receive data ready interrupt 1: Enable the receive data ready interrupt	RW

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37.2.5 UART Interrupt Identification Register (UIIR)

The read-only UART Interrupt Identification Register (UIIR) records the prioritized pending interrupt source information. Its initial value after power-on reset is 0x01.

UIIR0, UIIR1, UIIR2 **0x10030008, 0x10031008, 0x10032008**

Bit	7	6	5	4	3	2	1	0
	FFMSEL		Reserved		INID			INPEND
RST	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
7:6	FFMSEL	**FIFO Mode Select.** 0b00: Non-FIFO mode 0b01: Reserved 0b10: Reserved 0b11: FIFO mode	R
5:4	Reserved	Writing has no effect, read as zero.	R
3:1	INID	**Interrupt Identifier.** These bits identify the current highest priority pending interrupt. INID: Description 0b000: Modem Status 0b001: Transmit Data Request 0b010: Receive Data Ready 0b011: Receive Line Status 0b100: Reserved 0b101: Reserved 0b110: Receive Time Out 0b111: Reserved See Table 37-3 for details.	R
0	INPEND	**Interrupt Pending.** 0: interrupt is pending 1: No interrupt pending	R

Table 37-3 UART Interrupt Identification Register Description

UIIR.INID	Interrupt Set/Clear Cause			
	Priority	Type	Source	Clear Condition
0b0001	—	None	No pending interrupt	—

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0b0110	1st Highest	Receive Line Status	Overrun, Parity, Frame Error, Break Interrupt, and FIFO Error (DMA mode only)	Reading ULSR or empty all the error characters in DMA mode
0b0100	2nd Highest	Receive Data Ready	FIFO mode: Trigger threshold was reached Non-FIFO mode: URBR full	FIFO mode: Reading URBR till below trigger threshold. Non-FIFO mode: Empty URBR
0b1100	2nd Highest	Receive Timeout	FIFO mode only: URBR not empty but no data read in for a period of time	Reset receive buffer by setting UFCR.RFRT to 1 or Reading URBR
0b0010	3rd Highest	Transmit Data Request	FIFO mode: Empty location in UTHR equal to half or more than half Non-FIFO mode: UTHR empty	FIFO mode: Data number in UTHR more than half Non-FIFO mode: Writing UTHR
0b0000	4th Highest	Modem Status	Modem CTS_ pin status change	Reading UMSR

37.2.6 UART FIFO Control Register (UFCR)

The write-only register UFCR contains the control bits for receive and transmit FIFO.

UFCR0, UFCR1, UFCR2 **0x10030008, 0x10031008, 0x10032008**

Bit	7	6	5	4	3	2	1	0
	RDTR		Reserved	UME	DME	TFRT	RFRT	FME
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:6	RDTR	**Receive Buffer Data Number Trigger.** These bits are used to select the trigger level for the receive data ready interrupt in FIFO mode. 0b00: 1 0b01: 8 0b10: 16 0b11: 24	W
5	Reserved	Writing has no effect, read as zero.	R
4	UME	**UART Module Enable.** 0: Disable UART 1: Enable UART	W

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3	DME	**DMA Mode Enable.** 0: Disable DMA mode 1: Enable DMA mode	W
2	TFRT	**Transmit Holding Register Reset.** 0: Not reset 1: Reset transmit FIFO	W
1	RFRT	**Receive Buffer Reset.** 0: Not reset 1: Reset receive FIFO	W
0	FME	**FIFO Mode Enable.** Set this bit before the trigger levels. 0: non-FIFO mode 1: FIFO mode	W

37.2.7 UART Line Control Register (ULCR)

The ULCR defines the format for UART data transmission.

ULCR0. ULCR1, ULCR2, ULCR3 **0x1003000C, 0x1003100C, 0x1003200C**

Bit	7	6	5	4	3	2	1	0
	DLAB	SBK	STPAR	PARM	PARE	SBLS	WLS	
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	DLAB	**Divisor Latch Access Bit.** 0: Enable to access URBR, UTHR or UIER 1: Enable to access UDLLR or UDLHR	W
6	SBK	**Set Break.** Causes a break condition (at least one 0x00 data) to be transmitted to the receiving UART. Acts only on the TXD pin and has no effect on the transmit logic. 0: No effect on TXD output 1: Forces TXD output to 0	W
5	STPAR	**Sticky Parity.** Setting this bit forces parity location to be opposite of PARM bit when PARE is 1 (it is ignored when PARE is 0). 0: Disable Sticky parity 1: Enable Sticky parity (opposite o f PARM bit)	W
4	PARM	**Parity Odd/Even Mode Select.** If PARE = 0, PARM is ignored. 0: Odd parity; 1: Even parity.	W

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3	PARE	**Parity Enable.** Enables a parity bit to be generated on transmission or checked on reception. 0: No parity; 1: Parity.	W
2	SBLS	**Stop Bit Length Select.** Specifies the number of stop bits transmitted and received in each character. When receiving, the receiver checks only the first stop bit. 0: 1 stop bit 1: 2 stop bits, except for 5-bit character then 1-1/2 bits	W
1:0	WLS	**Word Length Select.** 0b00: 5-bit character 0b01: 6-bit character 0b10: 7-bit character 0b11: 8-bit character	W

37.2.8 UART Line Status Register (ULSR)

The read-only ULSR indicates status information during the data transfer. Receive error information in ULSR[4:1] remains set until software reads ULSR and it must be read before the error character is read.

ULSR0, ULSR1, ULSR2 **0x10030014, 0x10031014, 0x10032014**

Bit	7	6	5	4	3	2	1	0
	FIFOE	TEMP	TDRQ	BI	FMER	PARER	OVER	DRY
RST	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
7	FIFOE	**FIFO Error Status. (FIFO mode only)** FIFOE is set when there is at least one kind of receive error (parity, frame, overrun, break) for any of the characters in receive buffer. FIFOE is reset when all error characters are read out of the buffer. During DMA transfer, the error interrupt generates when FIFOE is 1, and no receive DMA request generates even when data in receive buffer reaches the trigger threshold until all the error characters are read out. In non-DMA mode, FIFOE set does not generate error interrupt. 0: No error data in receive buffer or non-FIFO mode 1: One or more error character in receive buffer	R
6	TEMP	**Transmit Holding Register Empty.** Set when both UTHR and shift register are empty. It is cleared when	R

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		either the UTHR or the shift register contains a data character. 0: There is data in the transmit shifter and UTHR 1: All the data in the transmit shifter and UTHR has been shifted out	
5	TDRQ	**Transmit Data Request.** Set when UTHR has half or more empty location (FIFO mode) or empty (non-FIFO mode). When both UIER.TDRIE and TDRQ are 1, transmit data request interrupt generates or during DMA transfer, DMA request to the DMA controller generates when UIER.TDRIE is 0 and TDRQ is 1. 0: There is one (non-FIFO mode) or more than half data (FIFO mode) in UTHR 1: None data (non-FIFO mode) or half or less than half data (FIFO mode) in UTHR	R
4	BI	**Break Interrupt.** BI is set when the received data input is held low for longer than a full-word transmission time (the total time of start bit + data bits + parity bit + stop bits). BI is cleared when the processor reads the ULSR. In FIFO mode, only one character equal to 0x00 is loaded into the FIFO regardless of the length of the break condition. BI shows the break condition for the character at the front of the FIFO, not the most recently received character. 0: No break signal has been received 1: Break signal received	R
3	FMER	**Framing Error.** Set when the bit following the last data bit or parity bit is detected to be 0. If the ULCR had been set for two or one and half stop bits, the other stop bits are not checked except the first one. In FIFO mode, FMER shows a framing error for the character at the front of the receive buffer, not for the most recently received character. Cleared when the processor reads the ULSR. 0: No framing error 1: Invalid stop bit has been detected	R
2	PARER	**Parity Error.** Indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. PARER is set upon detection if a parity error and is cleared when the processor reads the ULSR. In FIFO mode, PARER shows a parity error for the character at the front of the FIFO, not the most recently received character. 0: No parity error 1: Parity error has occurred	R
1	OVER	**Overrun Error.**	R

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		Set when both receive buffer and shifter are full and new data is received which will be lost. Cleared when the processor reads the ULSR. 0: No data has been lost 1: Receive data has been lost	
0	DRY	**Data Ready.** Set when a complete incoming character has been received into the Receive Buffer registers. DRY is cleared when the receive buffer is read (non-FIFO mode) or when the buffer is empty or when the buffer is reset by setting UFCR.RFRT to 1. 0: No data has been received 1: Data is available in URBR	R

37.2.9 UART Modem Control Register (UMCR)

The UMCR uses the modem control pins RTS_ and CTS_ to control the interface with a modem or data set. UMCR also controls the loopback mode. Loopback mode must be enabled before the UART is enabled.

UMCR0, UMCR1, UMCR2 **0x10030010, 0x10031010, 0x10032010**

Bit	7	6	5	4	3	2	1	0
	MDCE	FCM	Reserved	LOOP	Reserved		RTS	Reserved
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	MDCE	**Modem Control Enable.** 0: Modem function is disabled; 1: Modem function is enabled.	W
6	FCM	**Flow Control Mode.** 0: Flow control by software; 1: Flow control by hardware.	
5	Reserved	Writing has no effect, read as zero.	R
4	LOOP	**Loop Back.** This bit is used for diagnostic testing of the UART. When LOOP is 1, TXD output pin is set to a logic 1 state, RXD is disconnected from the pin, and the output of the transmitter shifter register is looped back into the receiver shift register input internally, similar to CTS_ and RTS_ pins and the RTS bit of the UMCR is connected to CTS bit of UMSR respectively. Loopback mode must be selected before the UART is enabled. 0: Normal operation mode; 1: Loopback-mode UART operation.	W
3:2	Reserved	Writing has no effect, read as zero.	R

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1	RTS	**Request To Send.** This bit can control the RTS_ output state. 0: RTS_ force to high; 1: RTS_ force to low.	W
0	Reserved	Writing has no effect, read as zero.	R

37.2.10 UART Modem Status Register (UMSR)

The read-only UMSR provides the current state of the control lines from the modem to the processor. They are cleared when the processor reads UMSR.

UMSR0, UMSR1, UMSR2 **0x10030018, 0x10031018, 0x10032018**

Bit	7	6	5	4	3	2	1	0
	Reserved			CTS	Reserved			CCTS
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	CTS	**Status of Clear To Send.** When MDCE bit is 1, this bit is the complement of CTS_ input. If Loop bit of UMCR is 1, this bit is equivalent to RTS bit of UMCR. 0: CTS_ pin is 1 1: CTS_ pin is 0	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	CCTS	**Change status of CTS_.** When MDCE bit is 1, this bit indicates the state change on CTS_ pin. 0: No state change on CTS_ pin since last read of UMSR 1: A change occurs on the state of CTS_ pin	R

37.2.11 UART Scratchpad Register

This Scratchpad register is used as a scratch register for the programmer and has no effect on the UART.

USPR **0x1003001C**

Bit	7	6	5	4	3	2	1	0
	Scratch Data							
RST	?	?	?	?	?	?	?	?

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37.2.12 Infrared Selection Register (ISR)

The ISR is used to configure the slow-infrared (SIR) interface that is provided in each UART to support two-way wireless communication using infrared transmission that conforms to the IrDA serial infrared specification 1.1. The maximum frequency is up to 115.2kbps.

ISR 0x10030020

Bit	7	6	5	4	3	2	1	0
	Reserved			RDPL	TDPL	XMODE	RCVEIR	XMITIR
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	RDPL	**Receive Data Polarity.** 0: Slow-infrared (SIR) interface decoder takes positive pulses as zeros 1: SIR decoder takes negative pulses as zeros	W
3	TDPL	**Transmit Data Polarity.** 0: SIR encoder generates a positive pulse for a data bit of zero 1: SIR encoder generates a negative pulse for a data bit of zero	W
2	XMODE	**Transmit Pulse Width Mode.** Set when the transmit encoder needs to generate 1.6us pulses (that are 3/16 of a bit-time at 115.2 kbps). Cleared when the transmit encoder needs to generate 3/16 of a bit-time wide according to current baud rate. 0: Transmit pulse width is 3/16 of a bit-time wide 1: Transmit pulse width is 1.6 us	W
1	RCVEIR	**Receiver SIR Enable.** This bit is used to select the signal from the RXD pin is processed by the IrDA decoder before it is fed to the UART (RCVEIR = 1) or bypass IrDA decoder and is fed directly to the UART (RCVEIR = 0). 0: Receiver is in UART mode 1: Receiver is in SIR mode	W
0	XMITIR	**Transmitter SIR Enable.** This bit is used to select TXD output pin is processed by the IrDA encoder before it is fed to the device pin (XMITIR = 1) or bypass IrDA encoder and is fed directly to the device pin (XMITIR = 0). **NOTE:** disable infrared LED before XMITIR is set, otherwise a false start bit may occur. 0: Transmitter is in UART mode 1: Transmitter is in SIR mode	W

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37.2.13 UART M Register (UMR)

UMSR0, UMSR1, UMSR2									0x10030024, 0x10031024, 0x10032024
Bit	7	6	5	4	3	2	1	0	
	Reserved			M					
RST	0	0	0	0	0	0	0	0	

M is the value of UMR register.
It will take UART at least M cycles to transmit one bit and receiver to receive one bit.
It will take UART at most M+1 cycles for transmitter to transmit one bit and receiver to receive one bit.

37.2.14 UART Add Cycle Register (UACR)

UACR0, UACR1, UACR2													0x10030028, 0x10031028, 0x10032028
Bit	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved				AC								
RST	0	0	0	0	0	0	0	0	0	0	0	0	

If nth bit of the register is 1, it will take UART M+1 cycles to transmit or receive the bit of date for transmit or receive.
If the register is 12'h0, UART will receive or transmit a bit by M cycle.
If the register is 12'hfff, UART will receive or transmit a bit by M+1 cycle.
For the detail to see For any frequency clock to use the Uart.

37.3 Operation

The following sections describe the UART operations that include flow of configuration, data transmission, data reception, and Infrared mode.

37.3.1 UART Configuration

Before UART starts to transfer data or changing transfer format, configuration must be done to define the transfer format. The sample flow is as the following:

In FIFO mode, set FME bit of UFCR to 1, reset receive and transmit FIFO, then initialize the UART as described below:

1 Clear UFCR.UME to 0.

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2 Set value in UDLL/UDHR to generate the baud rate clock.
3 Set data format in ULCR.
4 If it is in FIFO MODE, set FME bit and other FIFO control in UFCR, reset receive and transmit FIFO, otherwise skip item 4.
5 Set each interrupt enable bit in UIER in interrupt-based transfer or set UFCR.DME in DMA-based transfer (DMA transfer is FIFO mode only), then set UFCR.UME.

37.3.2 Data Transmission

After configuration, UART is ready for data transfer. For data transmission, refer to the following procedure:

1 Read ULSR.TDRQ (interrupt disable) or wait for transmit data request interrupt (interrupt enable), if TDRQ = 1 or transmit data request interrupt generates, that means there is enough empty location in UTHR for new data.
2 If ULSR.TDRQ is 1 or get the transmit data request interrupt, write transmit data to UTHR to start transmission.
3 Do item 1 and item 2 if there are more data waiting for transmit.
4 After all necessary data are written to UTHR, wait ULSR.TEMP = 1, that means all data completely transmitted.
5 If it is necessary to send break, set ULCR.SBK and at least wait for 1-bit interval time to send a valid break, then clear ULCR.SBK.
6 Clear UME bit to finish UART transmission.

37.3.3 Data Reception

After configuration, UART is ready for data transfer. For data reception, refer to the following sample procedure:

1 Read ULSR.DRY (interrupt disable) or wait for receive data request interrupt (interrupt enable), if ULSR.DRY =1 or receive data request interrupt generates, that means URBR has one data (non-FIFO mode) or data in URBR reaches the trigger value. (FIFO mode)
2 If ULSR.DRY = 1 or receive data request interrupt generates, then read ULSR.FIFOE or see if there is error interrupt, if FIFOE = 1, it means received data has receive error, then go to error handler, other wise go to item 3.
3 Read one received data in URBR (non-FIFO mode) or data equal to trigger value in URBR. (FIFO mode)
4 Check whether all data received: check whether ULSR.DRY = 0, in FIFO mode and interrupt is enabled, timeout interrupt may generate, when timeout interrupt generates, read URBR till ULSR.DRY = 0.
5 Clear UFCR.UME to end data reception when all data are received and ULSR.DRY = 0.

37.3.4 Receive Error Handling

A sample error handling flow is as the following:

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1 If ULSR.FIFOE = 1, it means there is receive error in received data, then check what error it is.
2 If ULSR.OVER = 1, go to OVER error handling.
3 If ULSR.BI = 1, go to Break handling.
4 If ULSR.FMER = 1, go to Frame error handling.
5 If PARER = 1, go to PARER error handling.

37.3.5 Modem Transfer

When UMCR.MDCE = 1, modem control is enabled. Transfer flow can be stopped and restarted by software through RTS_ and CTS_ pin. When UART transmitter detects low level on CTS_ pin, it stops transmission and TxD pin goes to mark state after finishing transmitting the current character until it detects CTS_ pin goes back to high level. RTS_ pin is output to receiving UART and its state can be controlled by setting UMCR.RTS bit, that is, setting UMCR.RTS to 1, RTS_ pin is low level output that means UART is ready to receive data, on the contrary, it means UART currently can't receive more data.

37.3.6 DMA Transfer

UART can operate in DMA-based (UFCR.DME = 1, FIFO mode only), that is, dma request initiated by UART takes the place of interrupt request and transmission/reception is carried out using DMA instead of CPU. Be sure that software guarantee to disable transmit and receive interrupt except timeout and error interrupts.

During DMA transfer, if an interrupt occurs, software must first read the ULSR to see if an error interrupt exists, then check the UIIR for the source of the interrupt and if DMA channel is already halt because of the error indicator from UART, then disable DMA channel and read out all the error data from receive FIFO. Software re-set and re-enable DMA and data transfer by DMA will re-start.

37.3.7 Slow IrDA Asynchronous Interface

Each UART supports slow infra-red (SIR) transmission and reception by setting ISR.XMITIR and ISR.RCVEIR to 1 (make sure the two bits are not set to 1 at the same time because SIR can't operate full-duplex). According to the IrDA 1.1, data rate is limited at a maximum value of 115.2Kbps.

In SIR transmit mode, the transmit pulse comes out at a rate of 3/16 (when the transmit data bit is zero); in SIR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (an active high or low pulse is demodulation to 0, and no pulse is demodulation to 1).

Compared to normal UART, there are some limitations to SIR, that is, each character is fixed to 8-bit data width, no parity and 1 stop bit and modem function is ignored. The IrDA 1.1 specifies a minimum 10ms latency after an optical node ceases transmitting before its receiver recovers its receiving function and software must guarantee this delay.

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In the IrDA 1.1 specification, communication must start up at the rate of 9600bps, but then allows the link to negotiate higher (or lower) data rates if supported by both ends. However, the communication rate will not automatically change. Change, if necessary, is performed by software.

37.3.8 For any frequency clock to use the UART

NOTE: if you don't set M register and UACR the UART work at normal mode with the specified frequencies. To use other frequency you should to set M register and UACR to right value.

1 The Improving

Following changes are made:

a One bit is composed by M CLK_{BR} cycles, which can be 4~1024.

b Some extra CLK_{BR} cycles can be inserted in some bits in one frame, so that like M has fraction.

For instance:

$CLK_{BR} = CLK_{DEV} / N$ N = 1, 2, …

$CLK_{BR} = CLK_{DEV}$ = 4MHz

Band rate = 460800

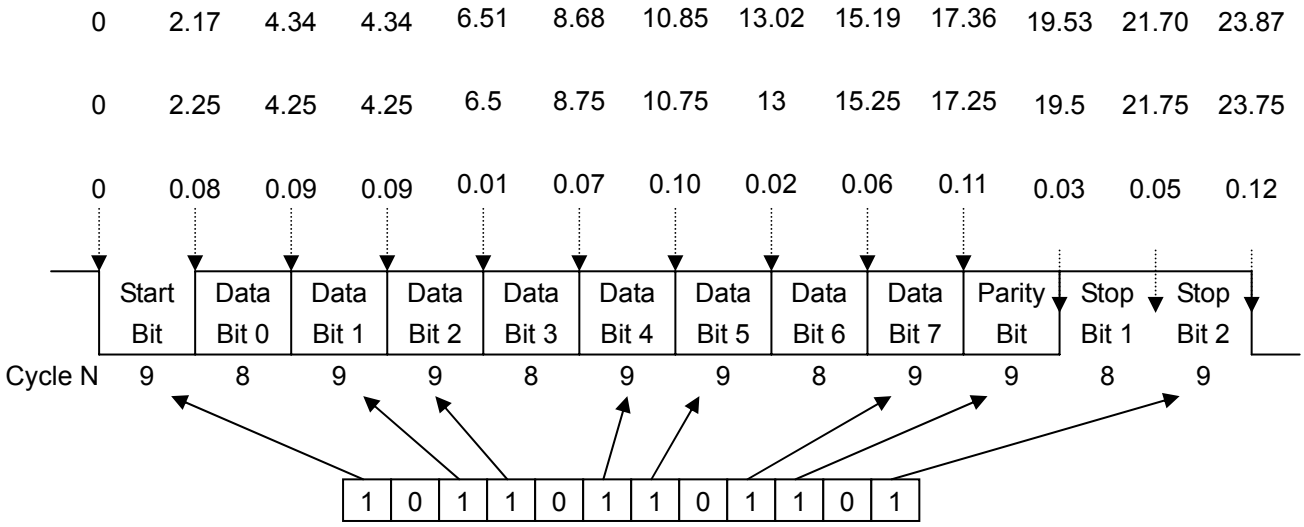
In accurate

M_a = 8.681

We take

M = 8, with 8 extra cycles in every frame

A 12-bit register is used to indicate where to insert the extra cycles.



For transmission, in theory, the biggest error is half of CLK_{BR} cycle, which is 0.125us here.

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2 To set UMR register

$CLK_{BR} = CLK_{DEV} / N$

$M_a = CLK_{BR}$/band rate

M is modem of M_a.

Write M to Mregister.

Considering the power and the robust quality, for M form 6 to 32 is you better select by set the UDLR.

The max error

$$\frac{0.5 / CLK_{BR}}{M_a / CLK_{BR}} = 0.5/M_a < 0.5/M$$

M	4	8	16	32	64
error/W_{bit}	12.5%	6.25%	3.125%	1.56%	0.78%

3 To set UACR value

For each bit of it means:

0: means not to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M cycles to transmit or receive the bit

1: means to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M+1 cycles to transmit or receive the bit

To set UACR value you must ensure that the max error of each bit should be less than $0.5P_{BR}$.

For example：M_a-M =0.15; M+1-M_a=0.85;

Write UMR 8

Write UMR 408

cycle/bit	：	M，	M，	M，	M+1，	M，	M，	M，	M，	M，	M，	M+1，	M
UACR	：	0	0	0	1	0	0	0	0	0	0	1	0

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38 Smart Card Controller

38.1 Overview

Smart Card Controller (SCC) interface is a primary device and communications interface for kinds of IC cards. The SCC interface supports communication with smart cards as specified in standard ISO7816-3. There are two SCC interfaces integrated in this SOC. And they perform the same functions. The SCC interface supports T=0 and T=1 protocol defined in ISO7816-3.

Software controls the session between the SCC interface and the card by SCC registers. Choosing protocol type and parameters, receiving and sending a byte to/from the card, activating/deactivating the card, and similar operations are accomplished with read/write operations to SCC registers. Transforming byte convention (inverse to direct and vice-versa, according to the session convention) is performed within SCC. Hence, software does not have to perform format inversion before character receipt. The SCC interface provides functionality to support the above standards, but it is the responsibility of software to ensure the standards are met.

Features:

- Supports normal card and UIM card
- 8-bit, 16-level receive-/transmit- FIFO
- Supports asynchronous character (T=0) communication modes
- Supports asynchronous block (T=1) communication modes
- Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.)
- Supports extra guard time waiting
- Auto-error detection in T=0 receive mode
- Auto-character repeat in T=0 transmit mode
- Transforms inverted format to regular format and vice versa
- Support stop clock function in some power consuming sensitive applications

38.2 Pin Description

Table 38-1 Smart Card Controller Pins Description

Name	I/O	Description
SCC_CLK	Output	Serial clock connects SCC and the card
SCC_DAT	Input/Output	Data communication pin

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38.3 Register Description

Table 38-2 Smart Card Controller Registers Description

Name	RW	Reset Value	Address	Access Size
SCCDR	RW	0x??	0x10041000	8
SCCFDR	R	0x00	0x10041004	8
SCCCR	RW	0x00000000	0x10041008	32
SCCSR	RW	0x8000	0x1004100C	16
SCCTFR	RW	0x0173	0x10041010	16
SCCEGTR	RW	0x00	0x10041014	8
SCCECR	RW	0x00000000	0x10041018	32
SCCRTOR	RW	0x00	0x1004101C	8

38.3.1 Transmit/Receive FIFO Data Register (SCCDR)

SCCDR 0x10041000

Bit	7	6	5	4	3	2	1	0
	DR							
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7:0	DR	Data port of HW FIFO.	RW

38.3.2 FIFO Data Count Register (SCCFDR)

SCCFDR 0x10041004

Bit	7	6	5	4	3	2	1	0
	Reserved			R				
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4:0	R	Characters resisted in FIFO.	R

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38.3.3 Control Register (SCCCR)

SCCCR 0x10041008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCCE	TRS	T2R	Reserved			FDIV		FLUSH	Reserved					TRIG		TP	CONV	TXIE	RXIE	TENDIE	RTOIE	ECIE	EPIE	RETIE	EOIE	Reserved		TSEND	PX		CLKSTP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SCCE	Enables or disables SCC. When disable it, the SCC_CLK will be stopped.	RW
30	TRS	Transmit or Receive Select. 0: Reception mode; 1: Transmission mode.	RW
29	T2R	Auto-T2R support. T2R means Transmit turn to Reception. 0: controlled by SW; 1: controlled by HW.	RW
28:26	Reserved	Writing has no effect, read as zero.	R
25:24	FDIV	Frequency Divider Select. 00: Same as device clk 01: Half of device clk 10: ¼ of device clk 11: Reserved	RW
23	FLUSH	Flush FIFO. 0: Does not empty the Rx/Tx FIFO; 1: Empty the Rx/Tx FIFO.	RW
22:18	Reserved	Writing has no effect, read as zero.	R
17:16	TRIG	Receive/Transmit FIFO trigger. 00: 1 01: 4 10: 8 11: 14	RW
15	TP	Communicate protocol. 0: (T=0); 1: (T=1).	RW
14	CONV	Card data transfer convention. 0: LSB first; 1: MSB first and inverted.	RW
13	TXIE	Tx FIFO counter meets the trigger value interrupt enable bit.	RW
12	RXIE	Rx FIFO counter meets the trigger value interrupt enable bit.	RW
11	TENDIE	Transmission finished interrupt enable bit. (Both FIFO and transmitter are empty)	RW
10	RTOIE	Reception timeout interrupt enable bit.	RW
9	ECIE	ETU counter overflow interrupt enable bit.	RW
8	EPIE	Parity error interrupt enable bit.	RW
7	RETIE	Re-transmitting 3 times interrupt enable bit.	RW
6	EOIE	Receive overrun error interrupt enable bit.	RW
5:4	Reserved	Writing has no effect, read as zero.	R

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3	TSEND	Receive TS character stage finished bit. 0: TS character has not been received; 1: TS character has been received.	RW
2:1	PX	Parameter X. SCC stop clock mode selection. 00 – Does not support SCC clock stop 01 – SCC_CLK stops at state low 10 – SCC_CLK stops at state high 11 – Reserved	RW
0	CLKSTP	SCC clock stop. 0:SCC has left or is leaving clock stop mode; 1: SCC has entered or is entering clock stop mode.	RW

38.3.4 Status Register (SCCSR)

SCCSR 0x1004100C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRANS	Reserved		ORER	RTO	PER	TFTG	RFTG	TEND	Reserved		RETR_3	Reserved			ECNTO
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	TRANS	Transfer status. Specifies whether the transfer is stopped or not.	R
14:13	Reserved	Writing has no effect, read as zero.	R
12	ORER	Receive overrun error.	RW
11	RTO	Reception timeout.	R
10	PER	Parity error.	RW
9	TFTG	Hit Tx FIFO trigger.	R
8	RFTG	Hit Rx FIFO trigger.	R
7	TEND	Transmission end. Both Tx FIFO and transmitter are empty.	RW
6:5	Reserved	Writing has no effect, read as zero.	R
4	RETR_3	Re-transmit exceed 3 times.	RW
3:1	Reserved	Writing has no effect, read as zero.	R
0	ECNTO	ETU counter overflow.	RW

38.3.5 Transmission Factor Register (SCCTFR)

SCCTFR 0x10041010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							FD								
RST	0	0	0	0	0	0	0	1	0	1	1	1	0	0	1	1

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Bits	Name	Description	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	FD	Value of F/D. The initial value is 0x173(371).	RW

38.3.6 Extra Guard Timer Register (SCCEGTR)

SCCEGTR 0x10041014

Bit	7	6	5	4	3	2	1	0
	EGTR							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	EGTR	The register is corresponding with N value of ISO7816-3. Which indicates the extra-guard time of a transmission?	RW

38.3.7 ETU Counter Value Register (SCCECR)

SCCECR 0x10041018

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												EC																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	EC	ETU counter. Write operation will clear the internal counter automatically.	RW

38.3.8 Reception Timeout Register (SCCRTOR)

SCCRTOS 0x1004101C

Bit	7	6	5	4	3	2	1	0
	RTO							
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	RTO	Retry times when parity error detected.	RW

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39 TS Slave Interface (TSSI)

39.1 Overview

The TS Slave Interface (TSSI) in JZ4770 is used to connect DTV Demodulator. It supports MPEG-2 Transport Stream (TS) as its input.

Features:

- Support both parallel mode and serial mode for TS data transfer
- TSDI0 or TSDI7 can be used to transfer data in serial mode
- The order of data in one byte supports LSB at first or MSB at first
- The order of data in one word supports LSB at first or MSB at first
- Input control signals and data can be either active high or active low
- Support using either positive or negative edge of TSCLK
- Support PID filtering function
- Up to 33 PID filters can be used when PID filtering function is enabled
- Support adding data 0 before or after transport stream
- Support master DMA transmission

39.2 Pin Description

Table 39-1 TSSI Pin Description

Name	I/O	Description
TSDI0~7	I	TS data bus
TSFAIL	I	TS packet uncorrectable
TSCLK	I	TS clock
TSFRM	I	TS data valid
TSSTR	I	TS packet start

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39.3 Register Description

In this section, we will describe the registers in TSSI. Following table lists all the register definitions. All registers' 32bit addresses are physical addresses. And detailed function of each register will be described below.

Table 39-2 TSSI Register Description

Name	Description	RW	Reset Value	Address	Access Size
TSENA	TSSI Enable Register	RW	0x08	0x134E0000	8
TSCFG	TSSI Configure Register	RW	0x04FF	0x134E0004	16
TSCTRL	TSSI Control Register	RW	0x03	0x134E0008	8
TSSTAT	TSSI State Register	RW	0x00	0x134E000C	8
TSFIFO	TSSI FIFO Register	R	0x????????	0x134E0010	32
TSPEN	TSSI PID Enable Register	RW	0x00000000	0x134E0014	32
TSNUM	TSSI Data Number Register	RW	0x00	0x134E0018	8
TSDTR	TSSI Data Trigger Register	RW	0x7F	0x134E001C	8
TSPID0	TSSI PID Filter Register 0	RW	0x00000000	0x134E0020	32
TSPID1	TSSI PID Filter Register 1	RW	0x00000000	0x134E0024	32
TSPID2	TSSI PID Filter Register 2	RW	0x00000000	0x134E0028	32
TSPID3	TSSI PID Filter Register 3	RW	0x00000000	0x134E002C	32
TSPID4	TSSI PID Filter Register 4	RW	0x00000000	0x134E0030	32
TSPID5	TSSI PID Filter Register 5	RW	0x00000000	0x134E0034	32
TSPID6	TSSI PID Filter Register 6	RW	0x00000000	0x134E0038	32
TSPID7	TSSI PID Filter Register 7	RW	0x00000000	0x134E003C	32
TSPID8	TSSI PID Filter Register 8	RW	0x00000000	0x134E0040	32
TSPID9	TSSI PID Filter Register 9	RW	0x00000000	0x134E0044	32
TSPID10	TSSI PID Filter Register 10	RW	0x00000000	0x134E0048	32
TSPID11	TSSI PID Filter Register 11	RW	0x00000000	0x134E004C	32
TSPID12	TSSI PID Filter Register 12	RW	0x00000000	0x134E0050	32
TSPID13	TSSI PID Filter Register 13	RW	0x00000000	0x134E0054	32
TSPID14	TSSI PID Filter Register 14	RW	0x00000000	0x134E0058	32
TSPID15	TSSI PID Filter Register 15	RW	0x00000000	0x134E005C	32
TSDDA	TSSI DMA Descriptor Address	RW	0x00000000	0x134E0060	32
TSDTA	TSSI DMA Target Address	R	0x00000000	0x134E0064	32
TSDID	TSSI DMA Identifier	R	0x00000000	0x134E0068	32
TSDCMD	TSSI DMA Command	R	0x00000000	0x134E006C	32
TSDST	TSSI DMA Status	RW	0x00000000	0x134E0070	32
TSTC	TSSI Transfer Control Register	RW	0x00000000	0x134E0074	32

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39.3.1 TSSI Enable Register (TSENA)

The register TSENA is used to trigger TSSI to work.

TSENA **0x134E0000**

Bit	7	6	5	4	3	2	1	0
	SFT_RST	Reserved		FAIL	PEN_0	PID_EN	DMA_EN	ENA
RST	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
7	SFT_RST	TSSI FIFO software-reset. Set it to 1 and later it will be cleared by hardware auto. 0: Stop reset 1: Start reset	RW
6:5	Reserved	Writing has no effect, read as zero.	R
4	FAIL	0:FAIL signal is decided by TSSI Demodulator 1:FAIL signal is equal to 1	
3	PEN_0	Choose PID filter enable for PID=0. 0: not enable 1: enable	RW
2	PID_EN	Enable / disenable the PID filtering function. 0: PID filtering function is not enabled 1: PID filtering function is enabled	RW
1	DMA_EN	Enable / disenable the DMA mode. 0: DMA mode is not enabled (CPU only) 1: DMA mode is enabled	RW
0	ENA	Enable / disenable the TSSI module. 0: TSSI is not enabled 1: TSSI is enabled	RW

39.3.2 TSSI Configure Register (TSCFG)

The register TSCFG is used to configure the TSSI.

TSCFG **0x134E0004**

Bit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	F_TRIGV			Reserved		TRANS_MD		EDN_WD	EDN_BT	TSDI_H	USE_0	TSCLK_CH	PARAL	TSCLK_P	TSFRM_H	TSSTR_H	TSFAIL_H
RST	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0

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<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>16:14</td><td>F_TRIGV</td><td>Specify the trigger value of FIFO.
<table>
<tr><th>F_TRIGV</th><th>Description</th></tr>
<tr><td>0</td><td>Trigger Value is 4</td></tr>
<tr><td>1</td><td>Trigger Value is 8</td></tr>
<tr><td>2</td><td>Trigger Value is 16</td></tr>
<tr><td>3</td><td>Trigger Value is 32</td></tr>
<tr><td>4</td><td>Trigger Value is 48</td></tr>
<tr><td>5</td><td>Trigger Value is 64</td></tr>
<tr><td>6</td><td>Trigger Value is 80</td></tr>
<tr><td>7</td><td>Trigger Value is 96</td></tr>
</table>
Trigger value should be greater than Expected Transfer Size.</td><td>RW</td></tr>
<tr><td>13:12</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>11:10</td><td>TRANS_MD</td><td>Choose the mode of adding data 0.
<table>
<tr><th>TRANS_MD</th><th>Description</th></tr>
<tr><td>0</td><td>Add data 0 before transport stream</td></tr>
<tr><td>1</td><td>Add data 0 after transport stream</td></tr>
<tr><td>2</td><td>Do not add data 0</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>9</td><td>EDN_WD*1</td><td>The order of data in word.</td><td>RW</td></tr>
<tr><td>8</td><td>EDN_BT*1</td><td>The order of data in byte.</td><td>RW</td></tr>
<tr><td>7</td><td>TSDI_H</td><td>Choose the polarity of TSDI0~7.
0: TSDI0~7 is active low
1: TSDI0~7 is active high</td><td>RW</td></tr>
<tr><td>6</td><td>USE_0</td><td>USE_0 is only used in SERIAL mode (TSCFG.PARAL=0).
0: Use TSDI7 to transfer data
1: Use TSDI0 to transfer data</td><td>RW</td></tr>
<tr><td>5</td><td>TSCLK_CH</td><td>Choose how to use TSCLK.
0: When $f_{pclk} > 3f_{TSCLK}$
1: When $f_{pclk} > 2f_{TSCLK}$</td><td>RW</td></tr>
<tr><td>4</td><td>PARAL</td><td>Choose the working mode of TSSI.
0: Serial Mode
1: Parallel Mode</td><td>RW</td></tr>
<tr><td>3</td><td>TSCLK_P</td><td>This bit is used to determine which edge of TSCLK is used when TSSI is sampling data.
0: Use the negative edge of TSCLK
1: Use the positive edge of TSCLK</td><td>RW</td></tr>
<tr><td>2</td><td>TSFRM_H</td><td>Choose the polarity of TSFRM.
0: TSFRM is active low
1: TSFRM is active high</td><td>RW</td></tr>
<tr><td>1</td><td>TSSTR_H</td><td>Choose the polarity of TSSTR.</td><td>RW</td></tr>
</table>

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		0: TSSTR is active low 1: TSSTR is active high	
0	TSFAIL_H	Choose the polarity of TSFAIL. 0: TSFAIL is active low 1: TSFAIL is active high	RW

NOTE:

*1: END_BT and END_WD in register TSCFG.

	Byte0 Bit0-7	Byte1 Bit0-7	Byte2 Bit0-7	Byte3 Bit0-7	Byte4 Bit0-7	Byte5 Bit0-7	Byte6 Bit0-7	Byte7 Bit0-7
END_WD=0	Byte0	Byte1	Byte2	Byte3				
	Byte4	Byte5	Byte6	Byte7				
END_WD=1	Byte3	Byte2	Byte1	Byte0				
	Byte7	Byte6	Byte5	Byte4				
END_BT=0	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
END_BT=1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

39.3.3 TSSI Control Register (TSCTRL)

The register TSCTRL is used to control TSSI to work.

TSCTRL **0x134E0008**

Bit	7	6	5	4	3	2	1	0
	Reserved					F_DTRM	F_OVRNM	F_TRIGM
RST	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	F_DTRM	FIFO data trigger interrupt mask. 0: enabled 1: masked	RW
1	F_OVRNM	FIFO overrun interrupt mask.	RW

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		0: enabled 1: masked	
0	F_TRIGM	FIFO trigger interrupt mask. 0: enabled 1: masked	RW

39.3.4 TSSI State Register (TSSTAT)

The register TSSTAT is used to keep the state of TSSI.

TSSTAT **0x134E000C**

Bit	7	6	5	4	3	2	1	0
	Reserved					F_DTR	F_OVRN	F_TRIG
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	F_DTR	FIFO data trigger interrupt flag. 1: active 0: not active	RW
1	F_OVRN	FIFO overrun interrupt flag. 1: active 0: not active	RW
0	F_TRIG	FIFO trigger interrupt flag. 1: active 0: not active	RW

39.3.5 TSSI FIFO Register (TSFIFO)

The register TSFIFO is corresponded to TSSI FIFO.

TSFIFO **0x134E0010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

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39.3.6 TSSI PID Enable Register (TSPEN)

The register TSPEN is used to control the PID filtering.

TSPEN **0x134E0014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN_151	EN_141	EN_131	EN_121	EN_111	EN_101	EN_91	EN_81	EN_71	EN_61	EN_51	EN_41	EN_31	EN_21	EN_11	EN_01	EN_150	EN_140	EN_130	EN_120	EN_110	EN_100	EN_90	EN_80	EN_70	EN_60	EN_50	EN_40	EN_30	EN_20	EN_10	EN_00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	EN_x1 (x=15~0)	PID filter enable for TSPIDx.PID1. 0: not enable; 1: enable.	RW
15:0	EN_x0 (x=15~0)	PID filter enable for TSPIDx.PID0. 0: not enable; 1: enable.	RW

39.3.7 TSSI Data Number Register (TSNUM)

The register TSNUM is used to show the current number of the data in FIFO.

TSNUM **0x134E0018**

Bit	7	6	5	4	3	2	1	0
	Reserved	DNUM						
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	DNUM	The current number of data in FIFO. The range of the data number is from 0 to 127.	RW

39.3.8 TSSI Data Trigger Register (TSDTR)

The register TSDTR is used to trigger the FIFO level interrupt when the current data number in the FIFO is more than the value in TSDTR.

TSDTR **0x134E001C**

Bit	7	6	5	4	3	2	1	0
	Reserved	DTR						
RST	0	1	1	1	1	1	1	1

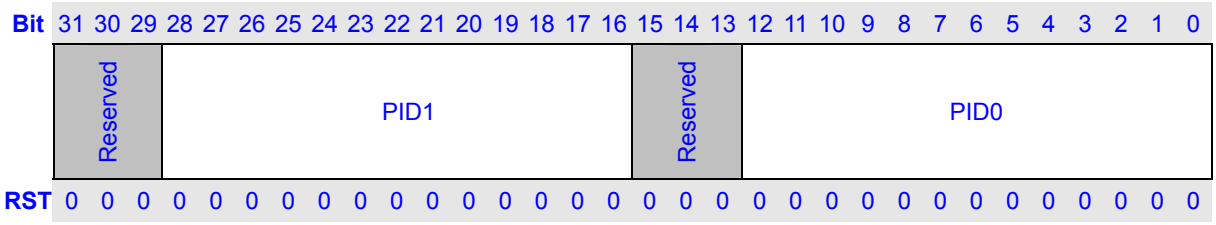
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Bits	Name	Description	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	DTRG	The trigger number of FIFO. The range of the data number is from 0 to 127.	RW

39.3.9 TSSI PID Filter Registers (TSPID0~15)

The registers TSPID0~15 are used to store PID values that need to be filtered from MPEG-2 TS.

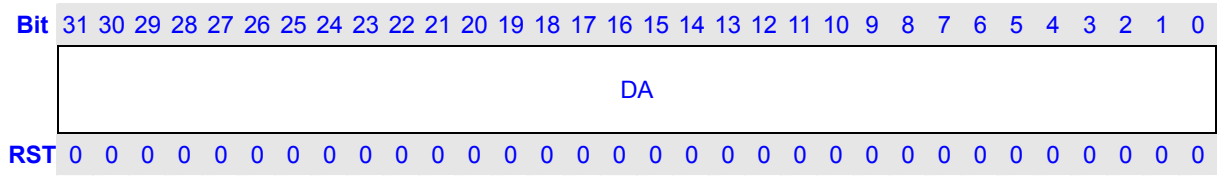
TSPID0~15 **0x134E0020~0x134E005C**



Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:16	PID1	Set the PID value that needs to be filtered.	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	PID0	Set the PID value that needs to be filtered.	RW

39.3.10 TSSI DMA Descriptor Address (TSDDA)

TDDA **0x134E0060**



Bits	Name	Description	RW
[31:0]	DA	Descriptor Address. It must be aligned to 4-word. It can be written by software and coped from the descriptor. Software should write the descriptor address before enable the DMA, and only the first DA needed if LINK enabled.	RW

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39.3.11 TSSI DMA Target Address (TSDTA)

TDTA 0x134E0064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R
31:0	TA	Target Address. It should be aligned to 32-word. It will be coped from the descriptor.	R

39.3.12 TSSI DMA Identifier (TSDID)

TDID 0x134E0068

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DID															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DID	Descriptor Identifier. It will be coped from the descriptor. It will be copied to TDST.DID.	R

39.3.13 TSSI DMA Command (TSDCMD)

TDCMD 0x134E006C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TLEN																								Reserved			TEFE	TSZ		TEIE	LINK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	R
31:8	TLEN	Transfer Length. Unit is word. When DMA transfer end, the TLEN will be counted down to 0. This field will be coped from the descriptor.	R
7:5	Reserved	Writing has no effect, read as zero.	R
4	TEFE	Transfer End Flag Enable. 0: disable TSDST.TEND 1: enable TSDST.TEND This field will be coped from the descriptor.	R
3:2	TSZ	Expected Transfer Size. 0: 4 word 1: 8 word 2: 16 word 3: 32 word This field will be coped from the descriptor.	R
1	TEIE	Transfer End Interrupt Enable. 0, disable interrupt 1, enable interrupt This field will be coped from the descriptor.	R
0	LINK	Descriptor Link Enable. 0, disable 1, enable This field will be coped from the descriptor.	R

39.3.14 TSST DMA Status (TSDST)

TDST 0x134E0070

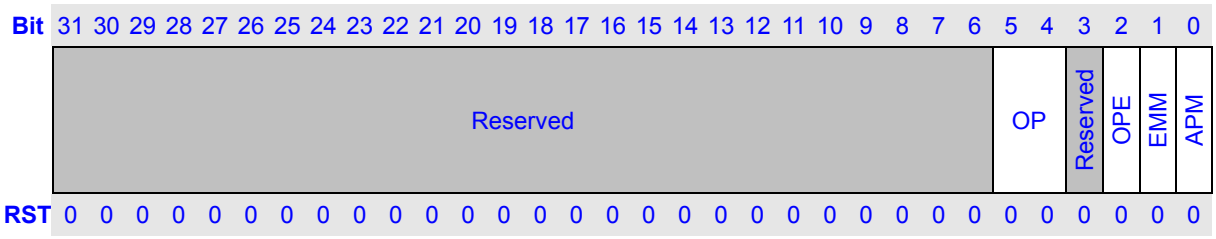
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DID																Reserved															TEND
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	DID	Copied from Descriptor Identifier when DMA interrupt occurred. Write 0 will clear this field.	RW
15:1	Reserved	Write has no effect, read as zero.	R
0	TEND	Transfer End Flag. 0: Transfer is not finished 1: Transfer is finished Write 0 will clear this field.	RW

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39.3.15 TSSI Transfer Control Register (TSTC)

TSTC **0x134E0074**



Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
5:4	OP	Optional Priority Configuration. Only used when OPE is set to 1. OP / TSSI AHB Priority / Number of Data in FIFO 2'b00 / 0 / n <= 16 1 / 16 < n <= 32 2 / 32 < n <= 64 3 / 64 < n 2'b01 / 0 / n <= 16 1 / 16 < n <= 48 2 / 48 < n <= 80 3 / 80 < n 2'b10 / 0 / n <= 32 1 / 32 < n <= 64 2 / 64 < n <= 96 3 / 96 < n 2'b11 / 0 / n <= 48 1 / 48 < n <= 80 2 / 80 < n <= 112 3 / 112 < n It is suggested to use 2'b10.	
3	Reserved	Writing has no effect, read as zero.	R
2	OPE	Optional Priority Mode Enable Control. Only used when APM is 1. 0: TSSI calculates the priority according to the fifo status 1: TSSI calculates the priority according to OP which is configured by software	RW
1	EME	Emergency Mode Enable Control. 0: Emergency Mode Disable; 1: Emergency Mode Enable	RW
0	APM	Auto Priority Mode Enable Control. 0: Auto priority mode disables. TSSI uses the priority set by arbiter 1: Auto priority mode enables. TSSI can use the priority according the FIFO status	RW

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39.4 TSSI Timing

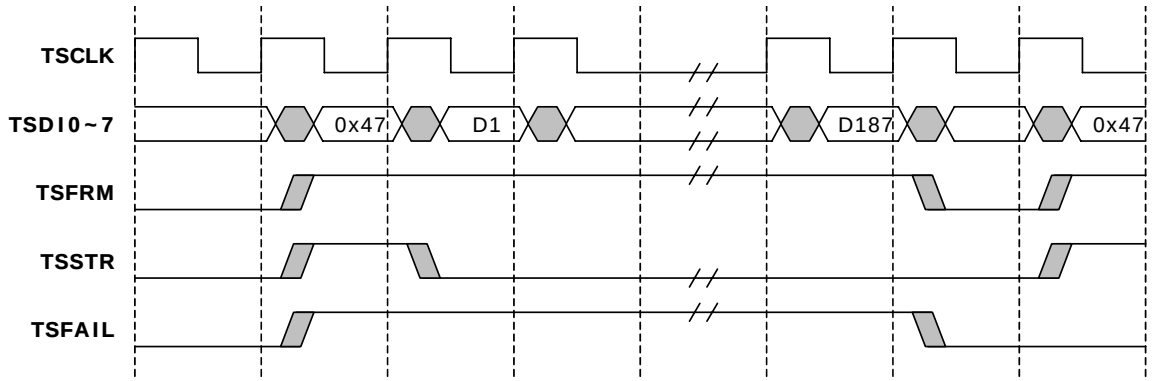


Figure 39-1 Timing waveform in parallel mode

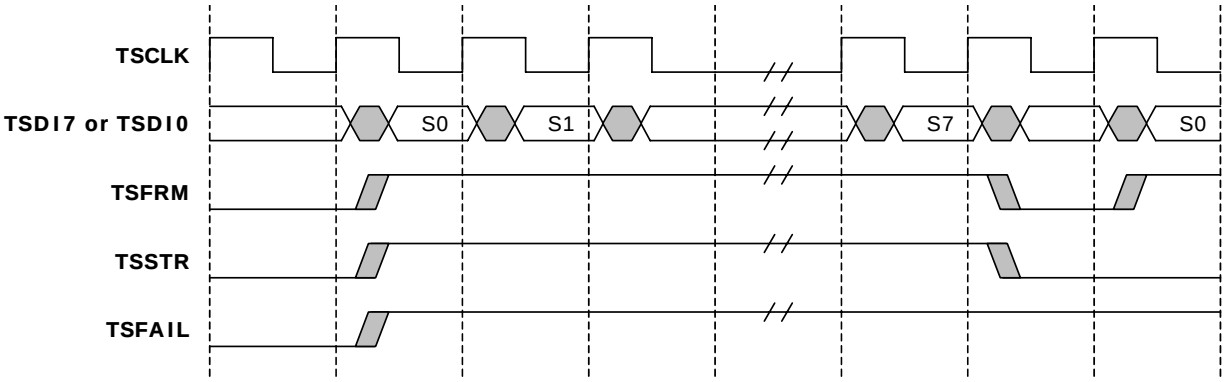


Figure 39-2 Timing waveform in serial mode

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39.5 TSSI Guide

39.5.1 TSSI Operation without PID Filtering Function

1 Set TSCTRL to 0x03 to mask all interrupts.
2 Set TSCFG to choose the working mode of TSSI and the trigger value of FIFO.
3 Set TSENA.PID_EN to 0 to turn off the PID filtering function.
4 set the DMA descriptor first if using the master DMA.
5 Set TSENA.DMA_EN to 1 or 0 to decide whether to use the DMA mode or not.
6 Write 0x00 to TSSTAT clear all interrupt flag.
7 Set TSCTRL to 0x00 to enable all interrupts.
8 Set TSENA.ENA to 1 to turn on TSSI module.

39.5.2 TSSI Operation with PID Filtering Function

1 Set TSCTRL to 0x03 to mask all interrupts.
2 Set TSCFG to choose the working mode of TSSI and the trigger value of FIFO.
3 Set TSENA.PID_EN to 1 to turn on the PID filtering function.
4 set the DMA descriptor first if using the master DMA.
5 Set TSENA.DMA_EN to 1 or 0 to decide whether to use the DMA mode or not.
6 Write 0x00 to TSSTAT clear all interrupt flag.
7 Set TSCTRL to 0x00 to enable all interrupts.
8 Set TSENA.ENA to 1 to turn on TSSI module.
9 Change TSPID registers and then set TSPID to enable the PID filter.
10 When PID in TS package is equal to the valve in TSPID register, the TS package will be getting.

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40 Ethernet MAC Controller

40.1 Overview

The processor contains one Ethernet media access controller (MAC), each capable of supporting 10/100Mbps Ethernet. The MAC provides the interface between the host application and the PHY layer through the media independent interface (MII) or the Reduced-MII (RMII). The PHY layer device is external to the processor.

The MAC supports the protocol requirements to meet the Ethernet/IEEE 802.3 specification. The MAC operates in both half and full duplex modes. In half-duplex mode, the controller supports the IEEE802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. In full-duplex mode, it supports the IEEE802.3 MAC Control Layer, including the pause operation for flow control.

A dedicated DMA engine is implemented to support the MAC so that the general purpose DMA is not required.

The MAC features are:

- IEEE 802.3, 802.3u specification compliance
- 10/100 Mbps data transfer rates
- IEEE 802.3 compliant MII interface to talk to an external PHY
- The Reduced-MII interface to an external PHY
- Full and half duplex
- CSMA/CD in half duplex
- Flow control support for full duplex
- Collision detection and auto retransmit on collisions in half duplex
- Automatic 32-bit CRC generation and checking
- Optional to insert PAD/CRC32 on transmit packets
- Optional automatic Pad stripping on the receive packets
- External and internal loopback support on the MII
- Filtering modes supported on the Ethernet side
  - One 48 bit Perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast addresses
  - Promiscuous Mode
  - Pass all incoming packets with a status report
  - Toss bad packets
- Dedicated DMA engine using burst mode
- DMA linked list Descriptor Chaining support
- Descriptor architecture allows large blocks of data transfer with minimum CPU intervention

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40.2 VLAN support Ethernet Signals

The following table shows the signals associated with the Ethernet MAC MII interfaces.

Table 40-1 Ethernet MII Signals

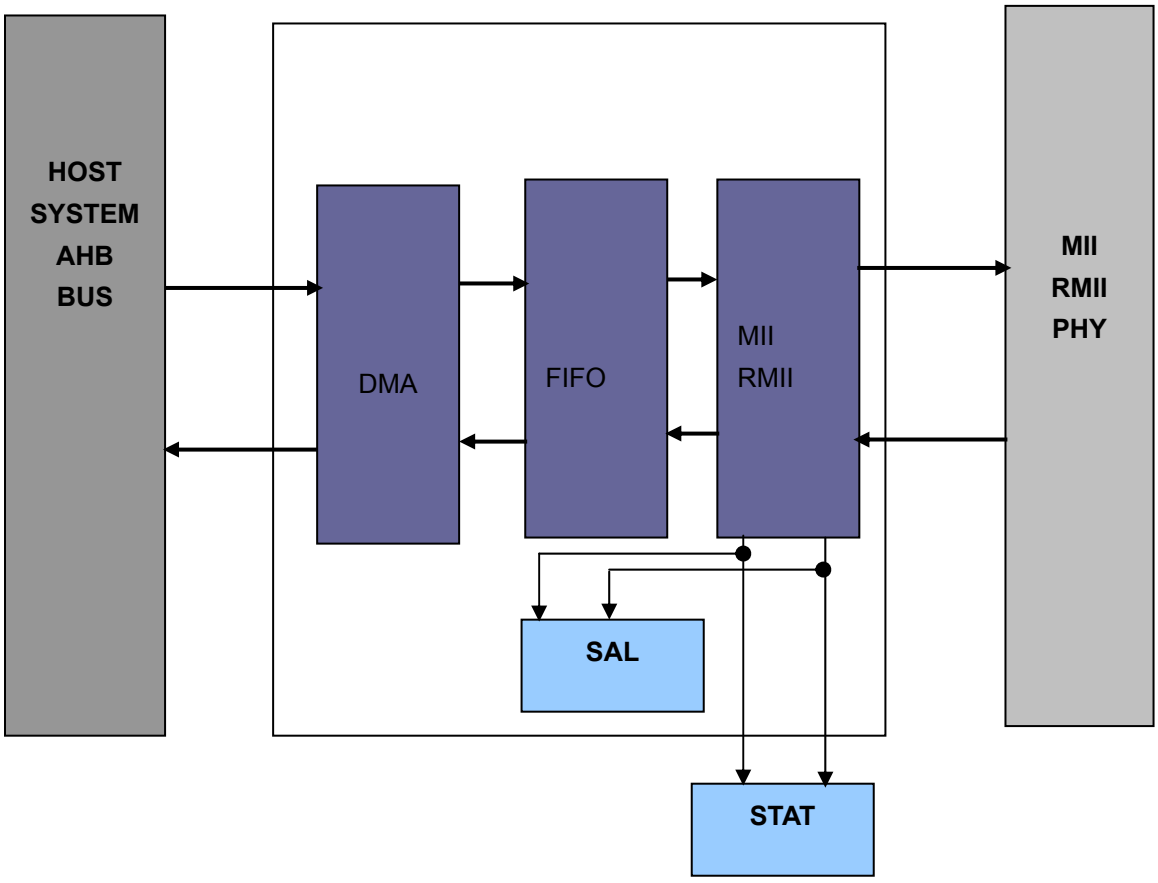
Signal	I/O	Description
RX_CLK	Input	Continuous clock that provides the timing reference for the datatransfer from the PHY to the MAC. RX_CLK is sourced by the PHY.RX_CLK must have a frequency equal to 25% of the data rate of the received signal data stream (typically 25 MHz at 100-Mbps and 2.5MHz at 10-Mbps).
RX_DV	Input	RX_DV is driven by the external Ethernet PHY and indicates that a receive frame is in process and that the data on RXD[3:0] is valid.
RX_ER	Input	RX_ER is driven by the Ethernet PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the MAC that an error was detected some where in the frame presently being transferred from the PHY to the MAC.
RXD [3:0]	Input	RXD[3:0] is a 4-bit wide data bus driven by the PHY to the MAC synchronous with RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD[3:0] transfers four bits of recovered data from the PHY to the MAC. While RX_DV is negated, RXD[3:0] has no effect on the MAC.
TX_CLK(REF_CLK)	Input	Continuous clock input for synchronization of transmit data. 25 MHz when operating at 100-Mbps and 2.5 MHz when operating at 10-Mbps. When in RMII mode, REF_CLK 50MZ whenever at 100-Mbps or at 10-Mbps.
TX_EN	Output	Indicates that the data on TXD[3:0] is valid.
TXD [3:0]	Output	4-bit wide data bus synchronous to TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] presents valid data to the PHY. While TX_EN is negated the data presented on TXD[3:0] is not valid.
CRS	Input	The PHY asserts CRS when either transmit or receive medium is non idle. The PHY negates CRS when both the transmit and receive medium are idle. CRS is an asynchronous input.
COL	Input	The PHY asserts COL upon detection of a collision on the medium and continues to assert COL while the collision condition persists. COL is an asynchronous input. The COL signal is ignored by the MAC when operating in full duplex mode.
MDC	Output	MDC is sourced by the MAC to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The MDC frequency is fixed at system bus clock divided by 160.
MDIO	I/O	MDIO is the bidirectional data signal between the MAC and the PHY that is clocked by MDC.

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Table 40-2 Pin Map of MII and RMII Mode

Normal MII Mode	Reduced MII Mode
TXD[1:0]	TXD[1:0]
TXD[3:2]	NC
TXEN	TXEN
TXCLK	REF_CLK
RXD[1:0]	RXD[1:0]
RXD[3:2]	NC
RXDV	CRS DV
RXCLK	NC
COL	NC
CRS	NC
MDC	MDC
MDIO	MDIO

40.3 Block Diagram



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40.4 DMA Module

40.4.1 Overview

The DMA module provides a DMA bridge between a host system that uses an AMBA AHB™ bus and the Ethernet MAC.

The DMA module interfaces to the host system through 32-bit AHB Master and Slave ports. On the MAC side of the module, it has a high-performance synchronous interface for DMA data transfer to/from the FIFO and a semi-synchronous interface for configuring the MAC and the FIFO through their HST interfaces.

For ease of handling by software, transfers are handled using linked lists of transfer descriptors which together define one buffer in host memory for Tx operations and another for Rx operations. These buffers will typically be configured as ring buffers but this is up to the user to implement.

Registers within the DMA provide Control and Status information concerning these transfers. These registers are accessed through the AHB Slave port, alongside accesses to the HST interfaces on the MAC and the FIFO.

40.4.2 Features

- AMBA AHB 2.0 compliant Master port for payload data transfer
- AMBA AHB 2.0 compliant Slave port for DMA bridge, FIFO and MAC configuration
- RAM-free synchronous single-clock domain design
- 32-bit architecture
- Linked-List Transfer Descriptors for minimal software overhead

40.4.3 Register Map

Name	RW	Reset Value	Address	Access Size
DMATxCtrl	RW	0x00000000	0x134B0180	32
DMATxDesc	RW	0x?0000000	0x134B0184	32
DMATxStatus	RW	0x????????	0x134B0188	32
DMARxCtrl	RW	0x00000000	0x134B018C	32
DMARxDesc	RW	0x?0000000	0x134B0190	32
DMARxStatus	RW	0x????????	0x134B0194	32
DMAIntrMask	RW	0x?0000000	0x134B0198	32
DMAInterrupt	RW	0x?0000000	0x134B019C	32

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40.4.4 Register Description

40.4.4.1 DMATxCtrl

DMATxCtrl **0x134B0180**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															TXEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	TXEN	Setting this bit enables DMA transmit packet transfers. The bit is cleared by the built-in DMA controller whenever it encounters a Tx Underrun or Bus Error state. Default is '0'.	RW

40.4.4.2 DMATxDesc

DMATxDesc **0x134B0184**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMATxDesc																															Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	DMATxDesc	When TxEnable is set by the host, the built-in DMA controller reads this register to discover the location in host memory of the first transmit packet descriptor.	R
0	Reserved	Writing has no effect, read as zero.	R

40.4.4.3 DMATxStatus

DMATxStatus **0x134B0188**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TxPktCount								Reserved														TxUdrun	TxPktSent
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	TxPktCount	8-bit transmit packet counter that is incremented whenever the built-in DMA controller successfully transfers a packet, and decremented whenever the host writes a '1' to bit 0 of this register.	RW
15:2	Reserved	Writing has no effect, read as zero.	R
1	TxUdrun	Set whenever the DMA controller reads a set ('1') Empty Flag in the descriptor it is processing.	RW
0	TxPktSent	When set, indicates that one or more packets have been successfully transferred. Writing a '1' to this bit reduces the TxPktCount value by one. The bit is cleared whenever TxPktCount is zero.	RW

40.4.4.4 DMARxCtrl

DMARxCtrl **0x134B018C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RXEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RXEN	Setting this bit enables DMA receive packet transfers. When set, the built-in DMA controller will start to receive a new packet whenever the FIFO indicates that a new packet is available (FRSOF asserted). The bit is cleared by the built-in DMA controller whenever it encounters an Rx Overflow or Bus Error state.	RW

40.4.4.5 DMARxDescriptor

DMARxDescriptor **0x134B0190**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DESCP_ADDR																															0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

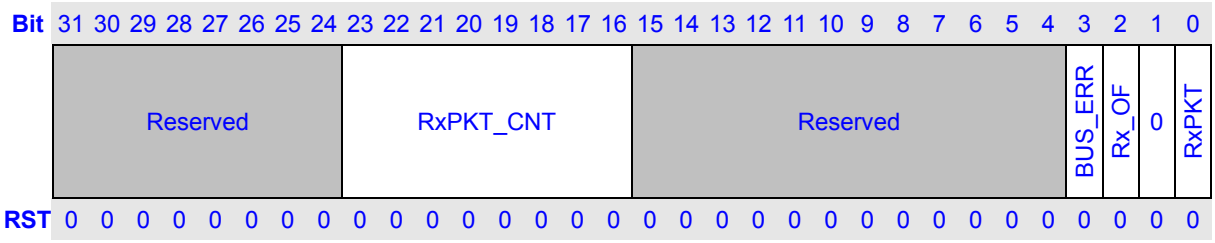
Bits	Name	Description	RW
31:2	DESCP_ ADDR	When RxEnable is set by the host, the built-in DMA controller reads this register to discover the location in host memory of the first receive packet Descriptor.	RW

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1:0	0	Ignored by the DMA controller, since it is a requirement of the system that all descriptors are 32-bit aligned in host memory.	RW

40.4.4.6 DMARxStatus

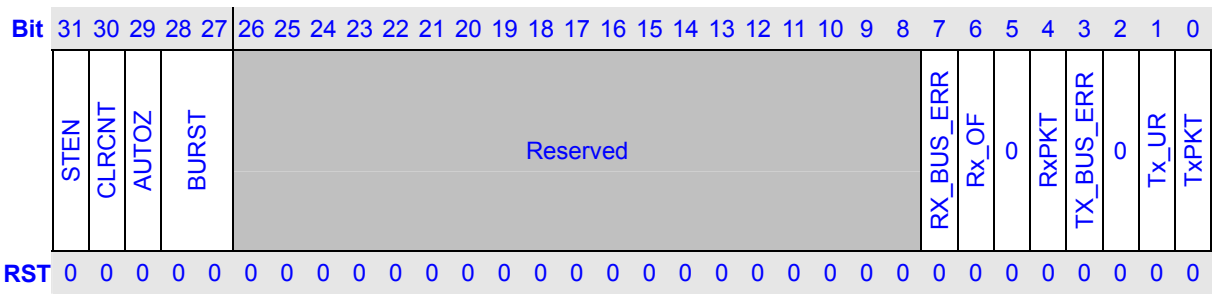
DMARxStatus **0x134B0194**



Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	RxPKT_CNT	8-bit receive packet counter that is incremented whenever the built-in DMA controller successfully transfers a packet, and is decremented whenever the host writes a '1' to bit zero of this register.	RWC
15:4	Reserved	Writing has no effect, read as zero.	R
3	BUS_ERR	When set, indicates that a host slave split, retry or error response was received by the DMA controller.	RWC
2	Rx_OF	Set whenever the DMA controller reads a zero Empty Flag in the descriptor it is processing.	RWC
1	0	0.	R
0	RxPKT	When set, indicates that one or more packets have been successfully transferred. Writing a '1' to this bit reduces the RxPktCount value by one. The bit is cleared whenever RxPktCount is zero.	RW

40.4.4.7 DMAIntrMask

DMAIntrMask **0x134B0198**



Bits	Name	Description	RW
31	STEN	Enable counting STAT.	RW

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30	CLRCNT	Zero all counters and carries immediately.	RW
27	AUTOZ	Auto zero addressed.	RW
28:27	BURST	00: BURST4 01: BURST4 10: BURST8 11: BURST16	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7	RX_BUS_ERR	Setting this bit to '1' enables the BusError bit in the DMARxStatus register as an interrupt source.	RW
6	Rx_OF	Setting this bit to '1' enables the RxOverflow bit in the DMARxStatus register as an interrupt source.	RW
5	0	0.	R
4	RxPKT	Setting this bit to '1' enables the RxPktReceived bit in the DMARxStatus register as an interrupt source.	RW
3	TX_BUS_ERR	Setting this bit to '1' enables the BusError bit in the DMATxStatus register as an interrupt source.	RW
2	0	0.	R
1	Tx_UR	Setting this bit to '1' enables the TxUnderrun bit in the DMATxStatus register as an interrupt source.	RW
0	TxPKT	Setting this bit to '1' enables the TxPktSent bit in the DMATxStatus register as an interrupt source.	RW

40.4.4.8 DMAInterrupt

DMAIntrrupt **0x134B019c**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RX_BUS_ERR	Rx_OF	0	RxPKT	TX_BUS_ERR	0	Tx_UR	TxPKT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	RX_BUS_ERR	Set to '1' to record a Receive Bus Error interrupt when the BusError bit in the DMARxStatus register and bit 7 of the DMAIntrMask register are both set.	R
6	Rx_OF	Set to '1' to record an Rx Overflow interrupt when the RxOverflow bit in the DMARxStatus register and bit 6 of the DMAIntrMask register are both set.	R

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5	0	0.	R
4	RxPKT	Set to '1' to record a RxPkt Received interrupt when the RxPktReceived bit in the DMARxStatus register and bit 4 of the DMAIntrMask register are both set.	R
3	TX_BUS_ERR	Set to '1' to record a Transmit Bus Error interrupt when the BusError bit in the DMATxStatus register and bit 3 of the DMAIntrMask register are both set.	R
2	0	0.	R
1	Tx_UR	Set to '1' to record a Tx Underrun interrupt when the TxUnderrun bit in the DMATxStatus register and bit 1 of the DMAIntrMask register are both set.	R
0	TxPKT	Set to '1' to record a Tx Pkt Sent interrupt when the TxPktSent bit in the DMATxStatus register and bit 0 of the DMAIntrMask register are both set.	R

40.5 FIFO Module

40.5.1 Overview

The FIFO module consists of the following seven major RTL modules:

- 10/100 Mb/s FIFO Fabric Transmit Interface Module
- 10/100 Mb/s FIFO System Transmit Interface Module
- 10/100 Mb/s FIFO Fabric Receive Interface Module
- 10/100 Mb/s FIFO System Receive Interface Module
- 10/100 Mb/s FIFO System Watermark Module
- 10/100 Mb/s FIFO Host Interface Module
- 10/100 Mb/s FIFO Clock and Reset Module

40.5.2 Features

- Data queuing for increased system-level throughput
- Synthesis-definable buffer sizes from 64K bytes to 256 bytes
- Clock frequency-independent I/O ports
- Single- or multiple-word I/O data transfers
- Programmable high and low receive storage-level indicators
- CPU frame insertion and inspection capabilities
- Automatic pause frame handshaking circuitry
- Programmable pause frame handshaking reassertion interval
- Programmable high transmit storage-level indicator
- Graceful receive memory full frame drop
- Graceful enable and disable
- Programmable frame mode or word cut-through threshold
- Transmit storage underrun indication

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- Transmit storage frame rewind capabilities
- Full memory utilization
- Optional per transmit frame MAC configuration data
- Synchronous dual-port memory utilization
- Low gate count
- Easy synthesis

40.5.3 Register Map

Name	RW	Reset Value	Address	Access Size
CFG_R0	RW	0x0000001F	0x134B003C	32
CFG_R1	rw	0x0FFFFFFF	0x134b004C	32
CFG_R2	RW	0x1FFF1FFF	0x134B0050	32
CFG_R3	RW	0x0FFF0FFF	0x134B0054	32
CFG_R4	RW	0x00000000	0x134B0058	32
CFG_R5	RW	0x0000FFFF	0x134B005C	32
RAM_ACC_R0	RW	0x00000000	0x134B0060	32
RAM_ACC_R1	RW	0x00000000	0x134B0064	32
RAM_ACC_R2	RW	0x00000000	0x134B0068	32
RAM_ACC_R3	R	0x00000000	0x134B006C	32
RAM_ACC_R4	RW	0x00000000	0x134B0070	32
RAM_ACC_R5	RW	0x00000000	0x134B0074	32
RAM_ACC_R6	RW	0x00000000	0x134B0078	32
RAM_ACC_R7	R	0x00000000	0x134B007C	32

40.5.4 Register Description

40.5.4.1 CFG_R0

CFG_R **0x134B003C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											FTFENRPLY	STFENRPLY	FRFENRPLY	SRFENRPLY	WTMENRPLY	Reserved			FTFENREQ	STFENREQ	FRFENREQ	SRFENREQ	WTMENREQ	Reserved			HSTRSTFT	HSTRSTST	HSTRSTFR	HSTRSTSR	HSTRSTWT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:21	Reserved	Writing has no effect, read as zero.	R
20	FTFENRPLY	When asserted, the mmiitfif_fab module is enabled. When negated,	R

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		the mmiitfif_fab module is disabled. The bit should be polled until it reaches the expected value.	
19	STFENRPLY	When asserted, the mmiitfif_sys module is enabled. When negated, the mmiitfif_sys module is disabled. The bit should be polled until it reaches the expected value.	R
18	FRFENRPLY	When asserted, the mmiirfif_fab module is enabled. When negated, the mmiirfif_fab module is disabled. The bit should be polled until it reaches the expected value.	R
17	SRFENRPLY	When asserted, the mmiirfif_sys module is enabled. When negated, the mmiirfif_sys module is disabled. The bit should be polled until it reaches the expected value.	R
16	WTMENRPLY	When asserted, the mmiitfif_wtm module is enabled. When negated, the mmiitfif_wtm module is disabled. The bit should be polled until it reaches the expected value.	R
15:13	Reserved	Writing has no effect, read as zero.	R
12	FTFENREQ	When asserted, requests enabling of the mmiitfif_fab module. When negated, requests disabling of the mmiitfif_fab module.	RW
11	STFENREQ	When asserted, requests enabling of the mmiitfif_sys module. When negated, requests disabling of the mmiitfif_sys module.	RW
10	FRFENREQ	When asserted, requests enabling of the mmiirfif_fab module. When negated, requests disabling of the mmiirfif_fab module.	RW
9	SRFENREQ	When asserted, requests enabling of the mmiirfif_sys module. When negated, requests disabling of the mmiirfif_sys module.	RW
8	WTMENREQ	When asserted, requests enabling of the mmiitfif_wtm module. When negated, requests disabling of the mmiitfif_wtm module.	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	HSTRSTFT	When asserted, this bit will place the mmiitfif_fab module in reset.	RW
3	HSTRSTST	When asserted, this bit will place the mmiitfif_sys module in reset.	RW
2	HSTRSTFR	When asserted, this bit will place the mmiirfif_fab module in reset.	RW
1	HSTRSTSR	When asserted, this bit will place the mmiirfif_sys module in reset.	RW
0	HSTRSTWT	When asserted, this bit will place the mmiitfif_wtm module in reset.	RW

40.5.4.2 CFG_R1

CFG_R1 **0x134B004C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				CFGFRTH												CFGXOFFRTX																
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	CFGFRTH	This hex value represents the minimum number of 4-byte locations that will be simultaneously stored in the receive RAM, relative to the beginning of the frame being input, before **frrdy** may be asserted. Note that **frrdy** will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on **fracpt** assertion. When set to maximum value, **frrdy** may be asserted only after the completion of the input frame. The value of this register must be greater than 18d when **hstdrplt64** is asserted; the additional two bits allow for overhead. The register length shown is for a receive RAM with 12 address bits (16K Bytes). The register length will vary with the addressable RAM size used.	RW
15:0	CFGXOFFRTX	This hex value represents the number of pause quanta (64 bit times) that occur after an XOFF pause frame has been acknowledged (**psack**), while the M-MIIFIF receive storage level has remained higher than the low watermark, until the M-MIIFIF will reassert **tpcf**.	RW

40.5.4.3 CFG_R2

CFG_R2 **0x134B0050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			CFGHWM													Reserved			CFGLWM													
RST	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:16	CFGHWM	This hex value represents the maximum number of 4-byte words that will be simultaneously stored in the receive RAM before **tpcf** and **psval** will facilitate an XOFF pause control frame. The register length shown is for a receive RAM with 12 address bits (16K Bytes). The register length will vary with the addressable RAM size used.	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	CFGLWM	This hex value represents the minimum number of 4-byte words that will be simultaneously stored in the receive RAM before **tpcf** and **psval** will facilitate an XON pause control frame in response to a previously transmitted XOFF pause control frame. The register length shown is for a receive RAM with 12 address bits (16K Bytes). The register length will vary with the addressable RAM size used.	RW

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40.5.4.4 CFG_R3

CFG_R3 0x134B0054

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				CFGHWMFT												Reserved				CFGFTTH											
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	CFGHWMFT	This hex value represents the maximum number of 4-byte locations that will be simultaneously stored in the transmit RAM before **fthwm** will be asserted. Note that **fthwm** has two **ftclk** clock periods of latency before assertion or negation. This should be considered when calculating any headroom required for maximum size packets. The register length shown is for a transmit RAM with 11 address bits (8K Bytes). The register length will vary with the addressable RAM size used.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	CFGFTTH	This hex value represents the minimum number of 4-byte locations that will be simultaneously stored in the transmit RAM, relative to the beginning of the frame being input, before **tpsf** will be asserted. Note that **tpsf** will be latent a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing. When set to maximum value, **tpsf** will be asserted only after the completion of the input frame. The register length shown is for a transmit RAM with 11 address bits (8K Bytes). The register length will vary with the addressable RAM size used.	RW

40.5.4.5 CFG_R4

CFG_R4 0x134B0058

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HSTFLTRFRM															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	HSTFLTRFRM	These configuration bits are used to signal the drop frame conditions internal to the M-MIIFIF. The bits correspond to the Receive Statistics Vector on a one-to-one basis. For example bit 0 corresponds to	RW

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		RSV[16], and bit 1 corresponds to RSV[17]. When these bits compare and the don't care is not asserted, the frame will be dropped. This is true for all **hstfltrm** bits with the exception of **hstfltrfrm[15]**, which is used to compare with the unicast address match input port of the M-MIIFIF. The setting of these bits, along with their don't care values in the **hstfltrfrmdc** configuration registers, create the filter that will assert the **srdrpfrm** output if the receive frame does not pass the acceptable conditions and should be dropped by the system. For example, if you want to drop a frame that contains a FCS Error, bit 4 would be set, and all receive frames that have RSV[20] asserted would be dropped.	

40.5.4.6 CFG_R5

CFG_R5 **0x134B005C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									CFGHDPLX	SRFULL	HSTSRFULLCLR	CLKENMODE	HSTDRPLT64	Reserved		HSTFLTRFRMDC															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:23	Reserved	Writing has no effect, read as zero.	R
22	CFGHDPLX	Assertion of this bit configures the M-MIIFIF to enable half-duplex backpressure as a flow control mechanism. Deassertion of this bit configures the M-MIIFIF to enable pause frames as a flow control mechanism.	RW
21	SRFULL	Assertion of this read-only bit indicates that the maximum capacity of the receive FIFO storage has been met or exceeded. If the **cfgfrth** bits are not all set, exceeding the FIFO storage capacity may result in data frame truncation as opposed to full frame deletion. Frame truncation is not recommended as an operation of the M-MIIFIF. The bit should be polled until it reaches the expected value.	RW
20	HSTSRFULLCLR	This bit should be written asserted when it is desired to clear the **srfull** indicator bit. After **hstfullclr** assertion, **srfull** should be read until it becomes deasserted. **hstfullclr** should then be	RW

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		written deasserted for the indicator to become operational again.	
19	CLKENMODE	This bit should be asserted when TXCENI is being toggled. This is done when the PE-MACMII is integrated with the PE-RMII.	RW
18	HSTDRPLT64	Setting this bit will cause the frame to be dropped if a receive frame is less than 64 bytes in length. This bit should not be asserted if **cfgfrth** is less than 12h.	RW
17:16	Reserved	Writing has no effect, read as zero.	R
15:0	HSTFLTRFRMDC	These configuration bits indicate which Receive Statistics Vectors are don't cares for M-MIIFIF frame drop circuitry. The bits correspond to the Receive Statistics Vector on a one per one basis. For example, bit 0 corresponds to RSV[16], and bit 1 corresponds to RSV[17]. Setting of a **hstfltrfrmdc** bit will indicate a don't care for that RSV bit. Clearing the bit will look for a matching level on the corresponding **hstfltrfrm** bit. If a match is made, then the frame is dropped. All bits should be set when **cfgfrth** bits are not all set.	RW

40.5.4.7 RAM_ACC_R0

RAM_ACC_R0 **0x134B0060**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTTRAMWREQ	HSTTRAMWACK	Reserved						HSTTRAMWDAT								Reserved			HSTTRAMWADX												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HSTTRAMWREQ	Host transmit RAM write request. Requests the handshake of **hsttramwdat** and **hsttramwadx** values to the transmit FIFO RAM. Should only be asserted while **hsttramwack** is negated and while the transmit data path is disabled from receiving data and in a steady state. It should only be negated after receiving an asserted **hsttramwack**.	RW
30	HSTTRAMWACK	Host transmit RAM write acknowledge. Signifies the acceptance of **hsttramwdat** and **hsttramwadx** values to the transmit FIFO RAM or mmiitfif_fab module. Will only be asserted or negated following assertion or negation of **hsttramwreq.**	R
29:24	Reserved	Writing has no effect, read as zero.	R

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23:16	HSTTRAMWDAT	Host transmit RAM write data. This is the upper byte of transmit FIFO RAM data that will be written at the address of **hsttramwadx[10:0]** if **hsttramwadx[12]** is negated and **hsttramwreq** is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows: hsttramwdat[39] = ftcfrm hsttramwdat[38:37] = ftpppadmode[1:0] hsttramwdat[36] = ftppen hsttramwdat[35] = ftppgenfcs hsttramwdat[34] = fteof hsttramwdat[33:32] = ftdatnvld[1:0]	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	HSTTRAMWADX	Host transmit RAM write address. This field has different functionality based on the value of **hsttramwadx[12]** and whether the M-MIIFIF FIFO RAM access register 0 is being written to or read from. When read from, **hsttramwadx[11:0]** field contains the actual write pointer value of the mmiitfif_fab module. When written to, the **hsttramwadx** register will be loaded. If **hsttramwadx[12]** is low, **hsttramwadx[10:0]** will be the transmit RAM address to which **hsttramwdat** is written. If **hsttramwadx[12]** is high, **hsttramwadx[11:0]** contains the pointer value that will be written to the mmiitfif_fab module. The register definition for **hsttramwadx[10:0]** is for a transmit RAM with 11 address bits (8K Bytes). The register length will vary with the addressable RAM size used. The definition of **hsttramwadx[12:11]** will shift to remain left-justified in the register.	RW

40.5.4.8 RAM_ACC_R1

RAM_ACC_R1 **0x134B0064**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTTRAMWDAT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	HSTTRAMWDAT	Host transmit RAM write data. This is the lower 4 bytes of transmit FIFO RAM data that will be written at the address of **hsttramwadx[10:0]** if **hsttramwadx[12]** is negated and **hsttramwreq** is asserted.	RW

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40.5.4.9 RAM_ACC_R2

RAM_ACC_R2 **0x134B0068**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTTRAMRREQ	HSTTRAMRACK	Reserved						HSTTRAMRDAT								Reserved			HSTTRAMRADX												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HSTTRAMRREQ	Host transmit RAM read request. Requests the handshake of **hsttramradx** values to the transmit FIFO RAM and **hsttramrdat** values from the transmit FIFO RAM. Should only be asserted while **hsttramrack** is negated and while the transmit data path is disabled from receiving data and in a steady state. It should only be negated after receiving an asserted **hsttramrack**.	RW
30	HSTTRAMRACK	Host transmit RAM read acknowledge. Signifies the acceptance of **hsttramradx** values to the transmit FIFO RAM and reception of **hsttramrdat** from the transmit FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of **hsttramrreq**.	R
29:24	Reserved	Writing has no effect, read as zero.	R
23:16	HSTTRAMRDAT	Host transmit RAM read data. This is the upper byte of transmit FIFO RAM data that was read at the address of **hsttramradx[10:0]** if **hsttramradx[12]** is negated and **hsttramrreq** is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows: hsttramrdat[39] = ftcfrm hsttramrdat[38:37] = ftpppadmode[1:0] hsttramrdat[36] = ftppen hsttramrdat[35] = ftppgenfcs hsttramrdat[34] = fteof hsttramrdat[33:32] = ftdatnvld[1:0]	R
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	HSTTRAMRADX	Host transmit RAM read address. If **hsttramradx[12]** is written low, **hsttramradx[10:0]** is the transmit FIFO RAM address that **hsttramrdat** is read from. If **hsttramradx[12]** is written high, **hsttramradx[11:0]** contains the pointer value read from the mmiitfif_sys module. The register definition for **hsttramradx[10:0]** is for a transmit RAM	RW

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		with 11 address bits (8K Bytes). The register length will vary with the addressable RAM size used. The definition of **hsttramradx[12:11]** will shift to remain left-justified in the register.	

40.5.4.10 RAM_ACC_R3

RAM_ACC_R3 **0x134B006C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTTRAMRDAT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	HSTTRAMRDAT	Host transmit RAM read data. This is the lower 4 bytes of transmit FIFO RAM data that is read at the address of **hsttramradx[10:0]** if **hsttramradx[12]** is negated and **hsttramrreq** is asserted.	R

40.5.4.11 RAM_ACC_R4

RAM_ACC_R4 **0x134B0070**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTRRAMWREQ	HSTRRAMWACK	Reserved						HSTRRAMWDAT								Reserved				HSTRRAMWADX											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HSTRRAMWREQ	Host receive RAM write request. Requests the handshake of **hstrramwdat** and **hstrramwadx** values to the receive FIFO RAM. Should only be asserted while **hstrramwack** is negated and while the receive data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted **hstrramwack**.	RW
30	HSTRRAMWACK	Host receive RAM write acknowledge. Signifies the acceptance of **hstrramwdat** and **hstrramwadx** values to the receive FIFO RAM or mmiirfif_sys module. Will only be asserted or negated following assertion or negation of **hstrramwreq**.	R
29:24	Reserved	Writing has no effect, read as zero.	R

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23:16	HSTRRAMWDAT	Host receive RAM write data. This is the upper byte of receive FIFO RAM data that will be written at the address of **hstrramwadx[11:0]** if **hstrramwadx[13]** is negated and **hstrramwreq** is asserted. This part of the receive FIFO RAM contains control information for the frame as follows: hstrramwdat[35] = frsof hstrramwdat[34] = freof hstrramwdat[33:32] = frdatnvld[1:0]	RW
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	HSTRRAMWADX	Host receive RAM write address. This field has different functionality based on the value of **hstrramwadx[13]** and whether the M-MIIFIF FIFO RAM access register 4 is being written to or read from. When read from, **hstrramwadx[12:0]** field contains the actual write pointer value of the mmiirfif_sys module. When written to, the **hstrramwadx** register will be loaded. If **hstrramwadx[13]** is low, **hstrramwadx[11:0]** will be the receive FIFO RAM address to which **hstrramwdat** is written. If **hstrramwadx[13]** is high, **hstrramwadx[12:0]** contains the pointer value that will be written to the mmiirfif_sys module. The register definition for **hstrramwadx[12:0]** is for a receive RAM with 12 address bits (16K bytes). The register length will vary with the addressable RAM size used. The definition of **hstrramwadx[13]** will shift to remain left-justified in the register.	RW

40.5.4.12 RAM_ACC_R5

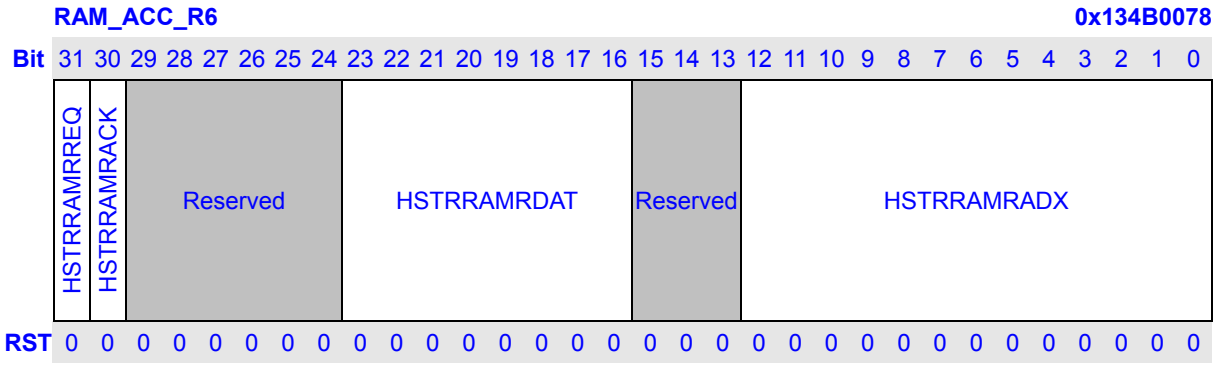
RAM_ACC_R5 **0x134B0074**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTRRAMWDAT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:0	HSTRRAMWDAT	Host receive RAM write data. This is the lower 4 bytes of receive FIFO RAM data that will be written at the address of **hstrramwadx[11:0]** if **hsttramwadx[13]** is negated and **hstrramwreq** is asserted.	RW

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40.5.4.13 RAM_ACC_R6



Bits	Name	Description	RW
31	HSTRRAMRREQ	Host receive RAM read request. Requests the handshake of **hstrramradx** values to the receive FIFO RAM and **hstrramrdat** values from the receive FIFO RAM. Should only be asserted while **hstrramrack** is negated and while the receive data path is disabled from receiving data and in a steady state. It should only be negated after receiving an asserted **hstrramrack**.	RW
30	HSTRRAMRACK	Host receive RAM read acknowledge. Signifies the acceptance of **hstrramradx** values to the receive FIFO RAM and reception of **hstrramrdat** from the receive FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of **hstrramrreq**.	R
29:24	Reserved	Writing has no effect, read as zero.	R
23:16	HSTRRAMRDAT	Host receive RAM read data. This is the upper byte of receive FIFO RAM data that was read at the address of **hstrramradx[10:0]** if **hstrramradx[13]** is negated and **hstrramrreq** is asserted. This part of the receive FIFO RAM contains control information for the frame as follows: hstrramrdat[35] = frsof hstrramrdat[34] = freof hstrramrdat[33:32] = frdatnvld[1:0]	R
15:13	Reserved	Writing has no effect, read as zero.	R
12:0	HSTRRAMRADX	Host receive RAM read address. If **hstrramradx[13]** is written low, **hstrramradx[11:0]** is the receive FIFO RAM address that **hstrramrdat** is read from. If **hstrramradx[13]** is written high, **hstrramradx[12:0]** contains the pointer value read from the mmiirfif_fab module. The register definition for **hstrramradx[12:0]** is for a receive RAM with 12 address bits (16K bytes). The register length will vary with the addressable RAM size used. The definition of **hstrramradx[13]** will shift to remain left-justified in the register.	RW

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40.5.4.14 RAM_ACC_R7

RAM_ACC_R7 0x134B007C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTRRAMRDAT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	HSTRRAMRDAT	Host receive RAM read data. This is the lower 4 bytes of receive FIFO RAM data that is read at the address of **hstrramradx[11:0]** if **hstrramradx[13]** is negated and **hstrramrreq** is asserted.	R

40.6 MII Module

40.6.1 Overview

The MII module is a full function 10 / 100 Mbps Media Access Controller modules with Media Independent Interface and optional interface modules.

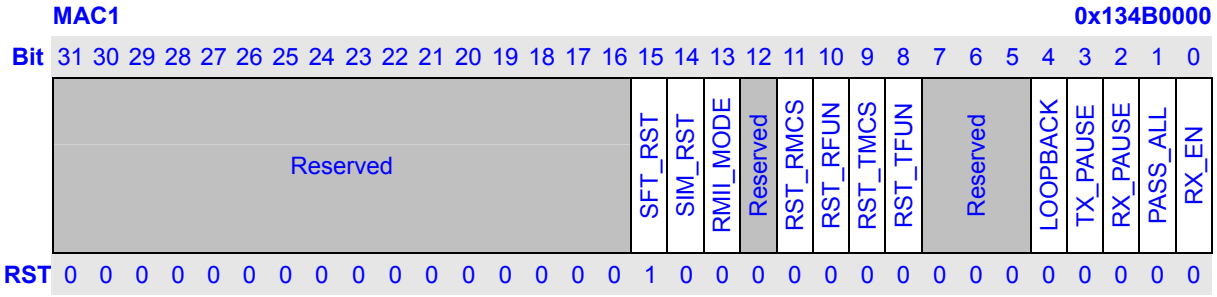
40.6.2 Register Map

Name	RW	Reset Value	Address	Access Size
MAC1	RW	0x00008000	0x134B0000	32
MAC2	RW	0x00000000	0x134B0004	32
IPGT	RW	0x00000000	0x134B0008	32
IPGR	RW	0x00000000	0x134B000C	32
CLRT	RW	0x0000370f	0x134B0010	32
MAXF	RW	0x00000600	0x134B0014	32
SUPP	RW	0x00001000	0x134B0018	32
TEST	RW	0x00000000	0x134B001C	32
MCFG	RW	0x00000000	0x134B0020	32
MCMD	RW	0x00000000	0x134B0024	32
MADR	RW	0x00000000	0x134B0028	32
MWTD	RW	0x00000000	0x134B002C	32
MRDD	RW	0x00000000	0x134B0030	32
MIND	RW	0x00000000	0x134B0034	32
SA0	RW	0x00000000	0x134B0040	32
SA1	RW	0x00000000	0x134B0044	32
SA2	RW	0x00000000	0x134B0048	32

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40.6.3 Register Description

40.6.3.1 MAC1



Bits	Name	Description	RW
15	SFT_RST	Setting this bit will put all modules within the PE-MACMII in reset except the Host Interface. The Host Interface is reset via HRST.	RW
14	SIM_RST	Setting this bit will cause a reset to the random number generator within the Transmit Function.	RW
13	RMII_MODE	RMII_MODE.	RW
12:11	Reserved	Writing has no effect, read as zero.	R
11	RST_RMCS	Setting this bit will put the MAC Control Sublayer / Receive domain logic in reset.	RW
10	RST_RFUN	Setting this bit will put the Receive Function logic in reset.	RW
9	RST_TMCS	Setting this bit will put the MAC Control Sublayer / Tx domain logic in reset.	RW
8	RST_TFUN	Setting this bit will put the Transmit Function logic in reset.	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	LOOPBACK	Setting this bit will cause the MAC Transmit interface to be loop backed to the MAC Receive interface. Clearing this bit results in normal operation.	RW
3	TX_PAUSE	When enabled, PAUSE Flow Control frames are allowed to be transmitted. When disabled, Flow Control frames are blocked.	RW
2	RX_PAUSE	When enabled, the MAC acts upon received PAUSE Flow Control frames. When disabled, received PAUSE Flow Control frames are ignored.	RW
1	PASS_ALL	When enabled, the MAC will indicate PASS CURRENT RECEIVE FRAME for all frames regardless of type (normal vs. Control). When disabled, the MAC de-asserts PASS CURRENT RECEIVE FRAME for valid Control frames.	RW
0	RX_EN	Set this to allow receive frames to be received. Internally the MAC synchronizes this control bit to the incoming receive stream and outputs SYNCHRONIZED RECEIVE ENABLE, to be used by host system to qualify receive frames.	RW

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40.6.3.2 MAC2

MAC2 0x134B0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	EXC_DEFER	BP_NB	NO_BACKOFF	Reserved		LONG_PRE	PURE_PRE	AUTO_PAD	VLAN_PAD	PAD_EN	CRC_EN	DLY_CRC	HUGE_FRM	LEN_CK	FULL_DPX
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
14	EXC_DEFER	When enabled the MAC will defer to carrier indefinitely as per the Standard. When disabled, the MAC will abort when the excessive deferral limit is reached and provide feedback to the host system.	RW
13	BP_NB	When enabled, the MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent.	RW
12	NO_BACKOFF	When enabled, the MAC will immediately retransmit following a collision rather than using the Binary Exponential Backoff algorithm as specified in the Standard.	RW
11:10	Reserved	Writing has no effect, read as zero.	R
9	LONG_PRE	When enabled, the MAC only allows receive packets, which contain preamble fields less than 12 bytes in length. When disabled, the MAC allows any length preamble as per the Standard.	RW
8	PURE_PRE	When enable, the MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errored preamble is discarded. When disabled, no preamble checking is performed.	RW
7	AUTO_PAD	Set this bit to cause the MAC to automatically detect the type of frame, either tagged or un-tagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly.	RW
6	VLAN_PAD	Set this bit to cause the MAC to pad all short frames to 64 bytes and append a valid CRC.	RW
5	PAD_EN	Set this bit to have the MAC pad all short frames. Clear this bit if frames presented to the MAC have a valid length. This bit is used in conjunction with *AUTO PAD ENABLE* and *VLAN PAD ENABLE*.	RW
4	CRC_EN	Set this bit to append a CRC to every frame whether padding was required or not. Must be set if PAD/CRC ENABLE is set. Clear this bit if frames presented to the MAC contain a CRC.	RW
3	DLY_CRC	This bit determines the number of bytes, if any, of proprietary header	RW

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		information that exists on the front of IEEE 802.3 frames.	
2	HUGE_FRM	When enabled frames of any length are transmitted and received.	RW
1	LEN_CK	When enabled, both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the Transmit/Receive Statistics Vector.	RW
0	FULL_DPX	When enabled, MAC operates in Full-Duplex mode. Disable for Half-Duplex operation.	RW

40.6.3.3 IPGT

IPGT **0x134B0008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									B2B_IPG						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
6:0	B2B_IPG	This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 µs (in 100 Mb/s) or 9.6 µs (in 10 Mb/s). In Half-Duplex the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 µs (in 100 Mb/s) or 9.6 µs (in 10 Mb/s).	RW

40.6.3.4 IPGR

IPGR **0x134B000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NB2B_IPG_P1							Reserved	NB2B_IPG_P2						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14:8	NB2B_IPG_P1	This is a programmable field representing the optional carrierSense window referenced in IEEE 802.3/4.2.3.2.1 'Carrier Deference'. If carrier is detected during the timing of IPGR1, the MAC defers to carrier. If, however, carrier becomes active after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to medium. Its range of values is 0x0 to IPGR2. The recommended value is 0xC (12d).	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	NB2B_IPG_P2	This is a programmable field representing the Non-Back-to-Back Inter-Packet-Gap. The recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 µs (in 100 Mb/s) or 9.6 µs (in 10 Mb/s).	RW

40.6.3.5 CLRT

CLRT **0x134B0010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		CW						Reserved				RT_MAX			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	1	1	1	1

Bits	Name	Description	RW
31:14	Reserved	Writing has no effect, read as zero.	R
13:8	CW	This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.	RW
7:4	Reserved	Writing has no effect, read as zero.	R
3:0	RT_MAX	This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the attemptLimit to be 0xF (15d). Its default is '0xF'.	RW

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40.6.3.6 MAXF

MAXF																														0x134B0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																MAXF															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

40.6.3.7 RAM_ACC_R7

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	MAXF	This field resets to 0x0600, which represents a maximum receive frame of 1536 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter maximum length restriction is desired, program this 16-bit field.	RW

40.6.3.8 SUPP

SUPP																														0x134B0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RST_INT	Reserved		PHY_MODE	RST_RMII	Reserved		SPEED	RST_100X	FQ	NC	LF	RST_10T	Reserved	EN_JAB	BM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	RST_INT	Setting this bit resets the attached Interface module. Clearing this bit allows for normal operation. This bit can be used in place of bits 11, 7, and 3 when connecting only 1 interface module.	RW
14:13	Reserved	Writing has no effect, read as zero.	R
12	PHY_MODE	This bit configures the Serial MII logic with the connecting SMII device type. Set this bit when connecting to a SMII PHY. Clear this bit when connecting to a SMII MAC. When MAC is selected, the SMII will operate at 100 Mb/s, Full Duplex.	RW
11	RST_RMII	This bit resets the Reduced MII logic.	RW
10:9	Reserved	Writing has no effect, read as zero.	R

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8	SPEED	This bit configures the Reduced MII logic for the current operating speed. When set, 100 Mb/s mode is selected. When cleared, 10 Mb/s mode is selected.	RW
7	RST_100X	This bit resets the PE100X module, which contains the 4B/5B symbol encipher/decipher logic. Effects PE100X module only.	RW
6	FQ	When enabled, transmit data is quieted which allows the contents of the cipher to be output. When cleared, normal operation is enabled. Effects PE100X module only.	RW
5	NC	When enabled, the raw transmit 5B symbols are transmitted without ciphering. When disabled, normal ciphering occurs. Effects PE100X module only.	RW
4	LF	When enabled, the 330ms Link Fail timer is disabled allowing for shorter simulations. Removes the 330 µS link-up time before reception of streams is allowed. When cleared, normal operation occurs. Effects PE100X module only.	RW
3	RST_10T	This bit resets the PE10T module which converts MII nibble streams to the serial bit stream of 10T transceivers. Effects PE10T module only.	RW
2	Reserved	Writing has no effect, read as zero.	R
1	EN_JAB	This bit enables the Jabber Protection logic within the PE10T in ENDEC mode. Jabber is the condition where a transmitter is stuck on for longer than 50ms preventing other stations from transmitting. Effects PE10T module only.	RW
0	BM	When '1' - MAC is in 10BASE-T ENDEC mode which changes decodes (such as Excess Defer) to be based on the bit clock rather than the nibble clock.	RW

40.6.3.9 TEST

TEST **0x134B001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													TB	TP	SQ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	TB	Setting this bit will cause the MAC to assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.	RW
1	TP	This bit causes the MAC Control sublayer to inhibit transmissions,	RW

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		just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received.	
0	SQ	This bit reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time.	RW

40.6.3.10 MCFG

MCFG **0x134B0020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RM	Reserved										CS			NP	SI	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	RM	This bit resets the MII Management module.	RW
14:5	Reserved	Writing has no effect, read as zero.	R
4:2	CS	This field is used by the clock divide logic in creating the MII Management Clock (MDC) which IEEE 802.3u defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz, however.	RW
1	NP	Set this bit to cause the MII Management module to perform read/write cycles without the 32-bit preamble field. Clear this bit to cause normal cycles to be performed. Some PHYs support suppressed preamble.	RW
0	SI	Set this bit to cause the MII Management module to perform read cycles across a range of PHYs. When set, the MII Management module will perform read cycles from address 1 through the value set in PHY ADDRESS[4:0]. Clear this bit to allow continuous reads of the same PHY.	RW

Clock Select	4	3	2
Host Clock divided by 4	0	0	x
Host Clock divided by 6	0	1	0
Host Clock divided by 8	0	1	1
Host Clock divided by 10	1	0	0
Host Clock divided by 14	1	0	1
Host Clock divided by 20	1	1	0
Host Clock divided by 28	1	1	1

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40.6.3.11 MCMD

MCMD 0x134B0024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														SCAN	READ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	SCAN	This bit causes the MII Management module to perform Read cycles continuously. This is useful for monitoring Link Fail for example.	RW
0	READ	This bit causes the MII Management module to perform a single Read cycle. The Read data is returned in Register 0xC (MII Mgmt Read Data).	RW

40.6.3.12 MADR

MADR 0x134B0028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					PHY_ADR					Reserved				REG_ADR	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Writing has no effect, read as zero.	R
12:8	PHY_ADR	This field represents the 5-bit PHY Address field of Mgmt cycles. Up to 31 PHYs can be addressed (0 is reserved).	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4:0	REG_ADR	This field represents the 5-bit Register Address field of Mgmt cycles. Up to 32 registers can be accessed.	RW

40.6.3.13 MWTD

MWTD 0x134B002C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	WDATA	When written, a MII Mgmt write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from Register (0x0A).	W

40.6.3.14 MRDD

MRDD **0x134B0030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	RDATA	Following a MII Mgmt Read Cycle, the 16-bit data can be read from this location.	R

40.6.3.15 MIND

MIND **0x134B0034**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												LF	NVLD	SCAN	BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	LF	When ‘1’ is returned - indicates MII Mgmt link fail has occurred.	R
2	NVLD	When ‘1’ is returned - indicates MII Mgmt Read cycle has not completed and the Read Data is not yet valid.	R
1	SCAN	When ‘1’ is returned - indicates a scan operation (continuous MII Mgmt Read cycles) is in progress.	R
0	BUSY	When ‘1’ is returned - indicates MII Mgmt module is currently performing an MII Mgmt Read or Write cycle.	R

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40.6.3.16 SA0

SA0 0x134B0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SADD1								SADD2							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	SADD1	This field holds the first octet of the station address.	RW
7:0	SADD2	This field holds the second octet of the station address.	RW

40.6.3.17 SA1

SA1 0x134B0044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SADD3								SADD4							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	SADD3	This field holds the third octet of the station address.	RW
7:0	SADD4	This field holds the fourth octet of the station address.	RW

40.6.3.18 SA2

SA2 0x134B0048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SADD5								SADD6							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	SADD5	This field holds the fifth octet of the station address.	RW
7:0	SADD6	This field holds the sixth octet of the station address.	RW

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40.7 RMII Module

40.7.1 Overview

The Reduced-MII was designed to convey the complete 16-bit MII information between a 10/100 Mb/s MAC and an RMII PHY with 7 pins per port.
The RMII module converts the Media Independent Interface to the new and improved Reduced Media Independent Interface for use with new lower pin count PHYs. The RMII adheres to the Reduced-MII Specification version 1.2, dated March 20, 1998.

40.7.2 Feature

- Provides reduced pin-count interface for Ethernet physical layer devices
- Supports Preliminary Draft Version 1.2 of the RMII Specification
- Supports Full and Half duplex operation
- Supports 10 and 100 Mb/s operation

40.8 SAL Module

40.8.1 Overview

The SAL module, Station Address Logic module, accepts the destination address field of incoming packets and all the related control signals and performs an address comparison.

Two types of valid destination addresses exist; a single physical address and a multicast address. When a single physical destination address is received, the PE-SAL module performs a direct comparison between the destination address and the address stored in the 48-bit Station Address Register. The 48-bit Station Address Register is loaded by the host when the module is first configured.

When a multicast destination address is received, a hash algorithm is applied to the address after it goes through a 32-bit CRC checker. The upper 6 bits of the 32-bit result from the CRC checker is decoded and used to select a bit in a 64-bit hash table which is pre-configured by the host. If the address compares correctly, the signal ACCEPT is set high to reflect a successful address comparison and the packet will be flagged as accepted. Otherwise, REJECT will be set high to reject the packet. The PE-SAL module can also be programmed to accept all incoming packets (promiscuous mode), all packets with multicast address or all packets with broadcast address.

In addition to the above functionality, the PE-SAL module facilitates insertion of its internal 48-bit Station Address Register into the system transmit data stream through byte multiplexed enabled output.

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40.8.2 Register Map

Name	RW	Reset Value	Address	Access Size
AFR	RW	0x00000000	0x134B01A0	32
HT1	RW	0x00000000	0x134B01A4	32
HT2	RW	0x00000000	0x134B01A8	32

40.8.3 Register Description

40.8.3.1 AFR

AFR **0x134B01A0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												PRO	PRM	AMC	ABC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	PRO	Promiscuous Mode.	RW
2	PRM	Accept Multicast.	RW
1	AMC	Accept Multicast (qualified).	RW
0	ABC	Accept Broadcast.	RW

40.8.3.2 HT1

HT1 **0x134B01A4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HT1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	HT1	Hash Table [64:32].	RW

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40.8.3.3 HT2

HT2																															0x134B01A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HT2																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	HT2	Hash Table [31:0].	RW

40.9 STAT Module

40.9.1 Overview

The STAT module is a low gate count, register based, statistics gathering module. It has 37 separate counters, which simply count or accumulate conditions that occur as packets are transmitted and received. These counters will support RMON MIB group 1, RMON MIB group 2 if table counters, RMON MIB group 3, RMON MIB group 9, RMON MIB 2, and the dot 3 Ethernet MIB.

On the transmit side, the STAT module looks at bits from the Transmit Statistics Vector (TSV[51:0]) whenever Transmit Statistics Vector Pulse (TSVP) is asserted. A particular MACs Transmit Function sub-module generates the Transmit Statistics Vector.

During receive packets, the Receive Statistics Vector (RSV[30:0]) is examined whenever the Receive Statistics Vector Pulse (RSVP) is asserted. A particular MACs Receive Function sub-module generates the Receive Statistics Vector.

One or more non-zero elements in either of these statistics vectors trigger the STAT module to update its statistics counters. These counters are stored in internal data registers. The host can access the internal data registers at any time. The STAT is capable of maintaining worst-case throughput conditions of one RSV and/or one TSV per four STAT internal clocks.

The ECU may be interrupted upon any one counter's rollover condition via a carry interrupt output from the STAT. Each counters rollover condition can be discreetly masked from causing an interrupt by internal masking registers. In addition, each individual counter value may be reset on read access, or all counters may be simultaneously reset by assertion of an external module input pin.

40.9.2 Register Map

Name	RW	Reset Value	Address	Access Size
TR64	RW		0x134B0080	32

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TR127	RW		0x134B0084	32
TR255	RW		0x134B0088	32
TR511	RW		0x134B008C	32
TR1K	RW		0x134B0090	32
TRMAX	RW		0x134B0094	32
TRMGV	RW		0x134B0098	32
RBYT	RW		0x134B009C	32
RPKT	RW		0x134B00A0	32
RFCS	RW		0x134B00A4	32
RMCA	RW		0x134B00A8	32
RBCA	RW		0x134B00AC	32
RXCF	RW		0x134B00B0	32
RXPF	RW		0x134B00B4	32
RXUO	RW		0x134B00B8	32
RALN	RW		0x134B00BC	32
RFLR	RW		0x134B00C0	32
RCDE	RW		0x134B00C4	32
RCSE	RW		0x134B00C8	32
RUND	RW		0x134B00CC	32
ROVR	RW		0x134B00D0	32
RFRG	RW		0x134B00D4	32
RJBR	RW		0x134B00D8	32
RDRP	RW		0x134B00DC	32
TBYT	RW		0x134B00E0	32
TPKT	RW		0x134B00E4	32
TMCA	RW		0x134B00E8	32
TBCA	RW		0x134B00EC	32
TXPF	RW		0x134B00F0	32
TDFR	RW		0x134B00F4	32
TEDF	RW		0x134B00F8	32
TSCL	RW		0x134B00FC	32
TMCL	RW		0x134B0100	32
TLCL	RW		0x134B0104	32
TXCL	RW		0x134B0108	32
TNCL	RW		0x134B010C	32
TPFH	RW		0x134B0110	32
TDRP	RW		0x134B0114	32
TJBR	RW		0x134B0118	32
TFCS	RW		0x134B011C	32
TXCF	RW		0x134B0120	32
TOVR	RW		0x134B0124	32

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TUND	RW		0x134B0128	32
TFRG	RW		0x134B012C	32
CAR1	R		0x134B0130	32
CAR2	R		0x134B0134	32
CAM1	RW		0x134B0138	32
CAM2	RW		0x134B013C	32

40.9.3 Register Description

40.9.3.1 TR64

TR64 **0x134B0080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TR64																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TR64	Transmit and Receive 64 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

40.9.3.2 TR127

TR127 **0x134B0084**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TR127																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TR127	Transmit and Receive 65 to 127 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

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40.9.3.3 TR255

TR255 **0x134B0088**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TR255																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TR255	Transmit and Receive 128 to 255 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

40.9.3.4 TR511

TR511 **0x134B008C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TR511																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TR511	Transmit and Receive 256 to 511 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

40.9.3.5 TR1K

TR1K **0x134B0090**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TR1K																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TR1K	Transmit and Receive 512 to 1023 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 512 to	RW

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		1023 bytes in length inclusive (excluding framing bits but including FCS bytes).	

40.9.3.6 TRMAX

TRMAX **0x134B0094**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TRMAX																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TRMAX	Transmit and Receive 1024 to 1518 Byte Frame Counter: Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

40.9.3.7 TRMGV

TRMGV **0x134B0098**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TRMGV																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TRMGV	Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter: Incremented for each good VLAN frame transmitted and received which is 1519 to 1522 bytes in length inclusive (excluding framing bits but including FCS bytes).	RW

40.9.3.8 RBYT

RBYT **0x134B009C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														RBYT																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

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31:23	Reserved	Writing has no effect, read as zero.	R
22:0	RBYT	Receive Byte Counter: The Statistic Counter register is incremented by the byte count of all frames received, including those in bad packets, excluding framing bits but including FCS bytes.	RW

40.9.3.9 RPKT

RPKT 0x134B00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RPKT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	RPKT	Receive Packet Counter: Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets).	RW

40.9.3.10 RFCS

RFCS 0x134B00A4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RFCS											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RFCS	Receive FCS Error Counter: Incremented for each frame received that has a integral 64 to 1518 length and contains a Frame Check Sequence error.	RW

40.9.3.11 RMCA

RMCA 0x134B00A8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RMCA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	RMCA	Receive Multicast Packet Counter: Incremented for each Multicast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors.	RW

40.9.3.12 RBCA

RBCA 0x134B00AC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										RBCA																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
21:0	RBCA	Receive Broadcast Packet Counter: Incremented for each Broadcast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors.	RW

40.9.3.13 RXCF

RXCF 0x134B00B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														RXCF																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	RXCF	Receive Control Frame Packet Counter: Incremented for each MAC Control frame received (PAUSE & Unsupported).	RW

40.9.3.14 RXPF

RXPF 0x134B00B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RXPF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RXPF	Receive PAUSE Frame Packet Counter: Incremented each time a valid PAUSE MAC Control frame is received.	RW

40.9.3.15 RXUO

RXUO 0x134B00B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RXUO											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RXUO	Receive Unknown OPcode Counter: Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE.	RW

40.9.3.16 RALN

RALN 0x134B00BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RALN											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RALN	Receive Alignment Error Counter: Incremented for each received frame from 64 to 1518 which contains an invalid FCS and is not an integral number of bytes.	RW

40.9.3.17 RFLR

RFLR 0x134B00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RFLR											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	TR127	Receive Frame Length Error Counter: Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46 - 1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.	RW

40.9.3.18 RCDE

RCDE 0x134B00C4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RCDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RCDE	Receive Code Error Counter: Incremented each time a valid carrier was present and at least one invalid data symbol was detected.	RW

40.9.3.19 RCSE

RCSE 0x134B00C8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RCSE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RCSE	Receive False Carrier Counter: Incremented each time a false carrier is detected during idle, as defined by a 1 on RX_ER and an '0xE' on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames.	RW

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40.9.3.20 RUND

RUND **0x134B00CC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RUND											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RUND	Receive Undersize Packet Counter: Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.	RW

40.9.3.21 ROVR

ROVR **0x134B00D0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				ROVR											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	ROVR	Receive Oversize Packet Counter: Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.	RW

40.9.3.22 RFRG

RFCS **0x134B00D4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RFRG											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RFRG	Receive Fragments Counter: Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS,	RW

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		includes integral and non-integral lengths.	

40.9.3.23 RJBR

RJBR **0x134B00D8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RJBR											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RJBR	Receive Jabber Counter: Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors.	RW

40.9.3.24 RDRP

RDRP **0x134B00DC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				RDRP											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	RDRP	Receive Dropped packets Counter: Incremented for frames received which are streamed to system but are later dropped due to lack of system resources.	RW

40.9.3.25 TBYT

TBYT **0x134B00E0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TBYT																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R

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23:0	TBYT	Transmit Byte Counter: Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.	RW

40.9.3.26 TPKT

TPKT **0x134B00E4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TPKT																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TPKT	Transmit Packet Counter: Incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast, and Multicast packets).	RW

40.9.3.27 TMCA

TMCA **0x134B00E8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TMCA																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17:0	TMCA	Transmit Multicast Packet Counter: Incremented for each Multicast valid frame transmitted (excluding Broadcast frames).	RW

40.9.3.28 TBCA

TBCA **0x134B00EC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														TBCA																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R

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17:0	TBCA	Transmit Broadcast Packet Counter: Incremented for each Broadcast frame transmitted (excluding Multicast frames).	RW

40.9.3.29 TXPF

TXPF **0x134B00F0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TXPF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TXPF	Transmit PAUSE Frame Packet Counter: Incremented each time a valid PAUSE MAC Control frame is transmitted.	RW

40.9.3.30 TDFR

TDFR **0x134B00F4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TDFR											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TDFR	Transmit Deferral Packet Counter: Incremented for each frame, which was deferred on its first transmission attempt. Does not include frames involved in collisions.	RW

40.9.3.31 TEDF

TEDF **0x134B00F8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TEDF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TEDF	Transmit Excessive Deferral Packet Counter: Incremented for frames aborted which were deferred for an excessive period of time (3036	RW

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		byte times).	

40.9.3.32 TSCL

TSCL 0x134B00FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TSCL											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TSCL	Transmit Single Collision Packet Counter: Incremented for each frame transmitted which experienced exactly one collision during transmission.	RW

40.9.3.33 TMCL

TMCL 0x134B0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TMCL											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TMCL	Transmit Multiple Collision Packet Counter: Incremented for each frame transmitted which experienced 2-15 collisions (including any late collisions) during transmission as defined using the RETRY[3:0] field of the TX function control register.	RW

40.9.3.34 TLCL

TLCL 0x134B0104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TLCL											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TLCL	Transmit Late Collision Packet Counter: Incremented for each frame transmitted which experienced a late collision during a transmission	RW

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		attempt. Late collisions are defined using the LCOL[5:0] field of the TX Function control register.	

40.9.3.35 TXCL

TXCL **0x134B0108**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TXCL											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TXCL	Transmit Excessive Collision Packet Counter: Incremented for each frame that experienced 16 collisions during transmission and was aborted.	RW

40.9.3.36 TNCL

TNCL **0x134B010C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TNCL											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Writing has no effect, read as zero.	R
12:0	TNCL	Transmit Total Collision Counter: Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (i.e. transmitting and receiving at the same time). Note, this register does not include collisions that result in an excessive collision condition.	RW

40.9.3.37 TPFH

TPFH **0x134B0110**

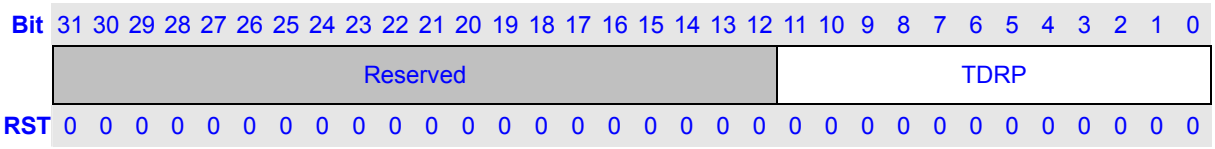
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TPFH											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TPFH	Transmit PAUSE Frames Honored Counter: Incremented each time a valid PAUSE MAC Control frame is transmitted and honored.	RW

40.9.3.38 TDRP

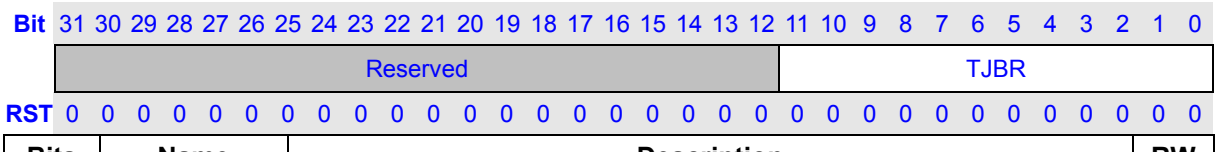
TDRP **0x134B0114**



Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TDRP	Transmit Drop Frame Counter: Incremented each time input PFH is asserted.	RW

40.9.3.39 TJBR

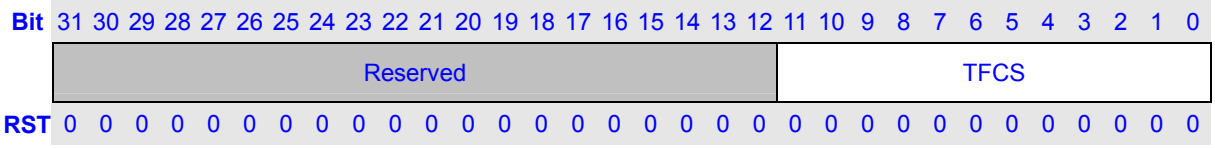
TJBR **0x134B0118**



Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TJBR	Transmit Jabber Frame Counter: Incremented for each oversized transmitted frame with an incorrect FCS value.	RW

40.9.3.40 TFCS

TFCS **0x134B011C**



Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TFCS	Transmit FCS Error Counter: Incremented for every valid sized	RW

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		packet with an incorrect FCS value.	

40.9.3.41 TXCF

TXCF **0x134B0120**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TXCF											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TXCF	Transmit Control Frame Counter: Incremented for every valid size frame with a Type Field signifying a Control frame.	RW

40.9.3.42 TOVR

TOVR **0x134B0124**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TOVR											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TOVR	Transmit Oversize Frame Counter: Incremented for each oversized transmitted frame with an correct FCS value.	RW

40.9.3.43 TUND

TUND **0x134B0128**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TUND											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TUND	Transmit Undersize Frame Counter: Incremented for every frame less then 64 bytes, with a correct FCS value.	RW

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40.9.3.44 TFRG

TFRG 0x134B012C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				TFRG											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	TFRG	Transmit Fragment Counter: Incremented for every frame less then 64 bytes, with an incorrect FCS value.	RW

40.9.3.45 CAR1

CAR1 0x134B0130

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C164	C1127	C1255	C1511	C11K	C1MAX	C1MGV	Reserved								C1RBY	C1RPK	C1RFC	C1RMC	C1RBC	C1RXC	C1RXP	C1RXU	C1RAL	C1RFL	C1RCD	C1RCS	C1RUN	C1ROV	C1RFR	C1RJB	C1RDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	C164	Carry register 1 TR64 Counter Carry bit.	R
30	C1127	Carry register 1 TR127 Counter Carry bit.	R
29	C1255	Carry register 1 TR255 Counter Carry bit.	R
28	C1511	Carry register 1 TR511 Counter Carry bit.	R
27	C11K	Carry register 1 TR1K Counter Carry bit.	R
26	C1MAX	Carry register 1 TRMAX Counter Carry bit.	R
25	C1MGV	Carry register 1 TRMGV Counter Carry bit.	R
24:17	Reserved	Writing has no effect, read as zero.	R
16	C1RBY	Carry register 1 RBYT Counter Carry bit.	R
15	C1RPK	Carry register 1 RPKT Counter Carry bit.	R
14	C1RFC	Carry register 1 RFCS Counter Carry bit.	R
13	C1RMC	Carry register 1 RMCA Counter Carry bit.	R
12	C1RBC	Carry register 1 RBCA Counter Carry bit.	R
11	C1RXC	Carry register 1 RXCF Counter Carry bit.	R
10	C1RXP	Carry register 1 RXPF Counter Carry bit.	R
9	C1RXU	Carry register 1 RXUO Counter Carry bit.	R
8	C1RAL	Carry register 1 RALN Counter Carry bit.	R
7	C1RFL	Carry register 1 RFLR Counter Carry bit.	R

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6	C1RCD	Carry register 1 RCDE Counter Carry bit.	R
5	C1RCS	Carry register 1 RCSE Counter Carry bit.	R
4	C1RUN	Carry register 1 RUND Counter Carry bit.	R
3	C1ROV	Carry register 1 ROVR Counter Carry bit.	R
2	C1RFR	Carry register 1 RFRG Counter Carry bit.	R
1	C1RJB	Carry register 1 RJBR Counter Carry bit.	R
0	C1RDR	Carry register 1 RDRP Counter Carry bit.	R

40.9.3.46 CAR2

CAR2 0x134B0134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												C2TJB	C2TFC	C2TCF	C2TOV	C2TUN	C2TFG	C2TBY	C2TPK	C2TMC	C2TBC	C2TPF	C2TDF	C2TED	C2TSC	C2TMA	C2TLC	C2TXC	C2TNC	C2TPH	C2TDP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19	C2TJB	Carry register 2 TJBR Counter Carry bit.	R
18	C2TFC	Carry register 2 TFCS Counter Carry bit.	R
17	C2TCF	Carry register 2 TXCF Counter Carry bit.	R
16	C2TOV	Carry register 2 TOVR Counter Carry bit.	R
15	C2TUN	Carry register 2 TUND Counter Carry bit.	R
14	C2TFG	Carry register 2 TFRG Counter Carry bit.	R
13	C2TBY	Carry register 2 TBYT Counter Carry bit.	R
12	C2TPK	Carry register 2 TPKT Counter Carry bit.	R
11	C2TMC	Carry register 2 TMCA Counter Carry bit.	R
10	C2TBC	Carry register 2 TBCA Counter Carry bit.	R
9	C2TPF	Carry register 2 TXPF Counter Carry bit.	R
8	C2TDF	Carry register 2 TDFR Counter Carry bit.	R
7	C2TED	Carry register 2 TEDF Counter Carry bit.	R
6	C2TSC	Carry register 2 TSCL Counter Carry bit.	R
5	C2TMA	Carry register 2 TMCL Counter Carry bit.	R
4	C2TLC	Carry register 2 TLCL Counter Carry bit.	R
3	C2TXC	Carry register 2 TXCL Counter Carry bit.	R
2	C2TNC	Carry register 2 TNCL Counter Carry bit.	R
1	C2TPH	Carry register 2 TPFH Counter Carry bit.	R
0	C2TDP	Carry register 2 TDRP Counter Carry bit.	R

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40.9.3.47 CAM1

CAM1 **0x134B0138**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	M164	M1127	M1255	M1511	M11K	M1MAX	M1MGV	Reserved								M1RBY	M1RPK	M1RFC	M1RMC	M1RBC	M1RXC	M1RXP	M1RXU	M1RAL	M1RFL	M1RCD	M1RCS	M1RUN	M1ROV	M1RFR	M1RJB	M1RDR
RST	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	M164	Mask register 1 TR64 Counter Carry bit Mask.	RW
30	M1127	Mask register 1 TR127 Counter Carry bit Mask.	RW
29	M1255	Mask register 1 TR255 Counter Carry bit Mask.	RW
28	M1511	Mask register 1 TR511 Counter Carry bit Mask.	RW
27	M11k	Mask register 1 TR1K Counter Carry bit Mask.	RW
26	M1MAX	Mask register 1 TRMAX Counter Carry bit Mask.	RW
25	M1MGV	Mask register 1 TRMGV Counter Carry bit Mask.	RW
24:17	Reserved	Writing has no effect, read as zero.	R
16	M1RBY	Mask register 1 RBYT Counter Carry bit Mask.	RW
15	M1RPK	Mask register 1 RPKT Counter Carry bit Mask.	RW
14	M1RFC	Mask register 1 RFCS Counter Carry bit Mask.	RW
13	M1RMC	Mask register 1 RMCA Counter Carry bit Mask.	RW
12	M1RBC	Mask register 1 RBCA Counter Carry bit Mask.	RW
11	M1RXC	Mask register 1 RXCF Counter Carry bit Mask.	RW
10	M1RXP	Mask register 1 RXPF Counter Carry bit Mask.	RW
9	M1RXU	Mask register 1 RXUO Counter Carry bit Mask.	RW
8	M1RAL	Mask register 1 RALN Counter Carry bit Mask.	RW
7	M1RFL	Mask register 1 RFLR Counter Carry bit Mask.	RW
6	M1RCD	Mask register 1 RCDE Counter Carry bit Mask.	RW
5	M1RCS	Mask register 1 RCSE Counter Carry bit Mask.	RW
4	M1RUN	Mask register 1 RUND Counter Carry bit Mask.	RW
3	M1ROV	Mask register 1 ROVR Counter Carry bit Mask.	RW
2	M1RFR	Mask register 1 RFRG Counter Carry bit Mask.	RW
1	M1RJB	Mask register 1 RJBR Counter Carry bit Mask.	RW
0	M1RDR	Mask register 1 RDRP Counter Carry bit Mask.	RW

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40.9.3.48 CAM2

CAM2 0x134B013C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												M2TJB	M2TFC	M2TCF	M2TOV	M2TUN	M2TFG	M2TBY	M2TPK	M2TMC	M2TBC	M2TPF	M2TDF	M2TED	M2TSC	M2TMA	M2TLC	M2TXC	M2TNC	M2TPH	M2TDP
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19	M2TJB	Mask register 2 TJBR Counter Carry bit Mask.	RW
18	M2TFC	Mask register 2 TFCS Counter Carry bit Mask.	RW
17	M2TCF	Mask register 2 TXCF Counter Carry bit Mask.	RW
16	M2TOV	Mask register 2 TOVR Counter Carry bit Mask.	RW
15	M2TUN	Mask register 2 TUND Counter Carry bit Mask.	RW
14	M2TFG	Mask register 2 TFRG Counter Carry bit Mask.	RW
13	M2TBY	Mask register 2 TBYT Counter Carry bit Mask.	RW
12	M2TPK	Mask register 2 TPKT Counter Carry bit Mask.	RW
11	M2TMC	Mask register 2 TMCA Counter Carry bit Mask.	RW
10	M2TBC	Mask register 2 TBCA Counter Carry bit Mask.	RW
9	M2TPF	Mask register 2 TXPF Counter Carry bit Mask.	RW
8	M2TDF	Mask register 2 TDFR Counter Carry bit Mask.	RW
7	M2TED	Mask register 2 TEDF Counter Carry bit Mask.	RW
6	M2TSC	Mask register 2 TSCL Counter Carry bit Mask.	RW
5	M2TMA	Mask register 2 TMCL Counter Carry bit Mask.	RW
4	M2TLC	Mask register 2 TLCL Counter Carry bit Mask.	RW
3	M2TXC	Mask register 2 TXCL Counter Carry bit Mask.	RW
2	M2TNC	Mask register 2 TNCL Counter Carry bit Mask.	RW
1	M2TPH	Mask register 2 TPFH Counter Carry bit Mask.	RW
0	M2TDP	Mask register 2 TDRP Counter Carry bit Mask.	RW

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41 EFUSE Slave Interface (EFUSE)

41.1 Overview

Total 256 bits of EFUSE are provided, separated into lower 128bits segment and higher 128bits segment.

Each segment can be programmed separately or together.
Each segment has a protect bit, which has higher priority than program segment selection.

Programming frequency should be with in 133Mhz and 166Mhz.
Programming time is around 3ms for either program in 128bits or 256bits.

Initial value of EFUSE is 0, when programmed to 1, it won't able to program back to 0 anymore.
Do not attempt to program any bit that already programmed to 1, such action will result unpredictable status to whole effuse block.

Programming voltage supply pin VDDQ:

- In program mode, supply VDDQ with 2.5V.
  Important: VDDQ pin should be kept 0v except during programming. Maximum accumulative time for VDDQ pin exposed under 2.5V+/-10% should be less than 1 sec.
- In read mode, leave VDDQ to 0V.

41.2 Register Description

Following table lists all the register definitions. All registers' 32bit addresses are physical addresses.

Table 41-1 EFUSE Register Description

Name	Description	RW	Reset Value	Address	Access Size
EFSCTL	EFUSE Control Register	RW	0x00	0x134100DC	8
EFUSE0	EFUSE Data 0 Register	RW	0x????????	0x134100E0	32
EFUSE1	EFUSE Data 1 Register	RW	0x????????	0x134100E4	32
EFUSE2	EFUSE Data 2 Register	RW	0x????????	0x134100E8	32
EFUSE3	EFUSE Data 3 Register	RW	0x????????	0x134100EC	32
EFUSE4	EFUSE Data 4 Register	RW	0x????????	0x134100F0	32
EFUSE5	EFUSE Data 5 Register	RW	0x????????	0x134100F4	32
EFUSE6	EFUSE Data 6 Register	RW	0x????????	0x134100F8	32
EFUSE7	EFUSE Data 7 Register	RW	0x????????	0x134100FC	32

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41.2.1 EFUSE Control Register (EFSCTL)

EFSCTL 0x134100DC

Bit	7	6	5	4	3	2	1	0
	Reserved						HI_WEN	LO_WEN
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:2	Reserved	Writing has no effect, read as zero.	R
1	HI_WEN	High 128 bit write enable bit. *1 0: Disable; 1: Enabled.	RW
0	LO_WEN	Low 128 bit write enable bit. *1 0: Disable; 1: Enabled.	RW

NOTE:

*1: DATA[31]/PRTCT bits take higher priorities than HI_WEN & LOW_WEN.

41.2.2 EFUSE Data Register (EFUSEn)

EFUSEn (n=0,1,2,4,5,6) 0x134100E0~0x134100FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DATA	EUFSE DATA register.	RW

EFUSE7 [31]	EFUSE7 [30] ~	EFUSE7 [1]	EFUSE7 [0]
EFUSE6 [31]	EFUSE6 [30] ~	EFUSE6 [1]	EFUSE6 [0]
EFUSE5 [31]	EFUSE5 [30] ~	EFUSE5 [1]	EFUSE5 [0]
EFUSE4 [31]	EFUSE4 [30] ~	EFUSE4 [1]	EFUSE4 [0]
EFUSE3 [31]	EFUSE3 [30] ~	EFUSE3 [1]	EFUSE3 [0]
EFUSE2 [31]	EFUSE2 [30] ~	EFUSE2 [1]	EFUSE2 [0]
EFUSE1 [31]	EFUSE1 [30] ~	EFUSE1 [1]	EFUSE1 [0]
EFUSE0 [31]	EFUSE0 [30] ~	EFUSE0 [1]	EFUSE0 [0]

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EFUSEn (n=3,7) **0x134100E0~0x134100FC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[31]/PRTCT	DATA [0-30]																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DATA[31]/PRTCT	EUFSE DATA bit 31 / Protect bit. *1 EFSUE3: When this bit programmed to 1, EFUSE0~3 lower 128 bits become un-programmable forever. EFUSE7: When this bit programmed to 1,EFUSE4~7 higher 128 bits become un-programmable forever.	RW
30:0	DATA [30:0]	EUFSE DATA register.	

EFUSE7 [30]	EFUSE7 [29]	~	EFUSE7 [1] EFUSE7 [0]
EFUSE6 [30]	EFUSE6 [29]	~	EFUSE6 [1] EFUSE6 [0]
EFUSE5 [30]	EFUSE5 [29]	~	EFUSE5 [1] EFUSE5 [0]
EFUSE4 [30]	EFUSE4 [29]	~	EFUSE4 [1] EFUSE4 [0]
EFUSE3 [30]	EFUSE3 [29]	~	EFUSE3 [1] EFUSE3 [0]
EFUSE2 [30]	EFUSE2 [29]	~	EFUSE2 [1] EFUSE2 [0]
EFUSE1 [30]	EFUSE1 [29]	~	EFUSE1 [1] EFUSE1 [0]
EFUSE0 [30]	EFUSE0 [29]	~	EFUSE0 [1] EFUSE0 [0]

NOTE:

*1: DATA[31]/PRTCT bits take higher priorities than HI_WEN & LOW_WEN.

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41.3 Flow

41.3.1 Write EFUSE Flow

1 Write full-256 bit.
   a Config AHB2 freq to 166Mhz.
   b Connect VDDQ pin to 2.5V. *1
   c Write register EFUSE0~EFUSE7.
   d Write register EFSCTL.HI_WEN and EFSCTL.LO_WEN to 1 at same time.
   e Wait till register EFSCTL.HI_WEN and EFSCTL.LO_WEN is set to 0.
   f Disconnect VDDQ pin from 3.3V and finish writing EFUSE.

2 Write low-128 bit.
   a Config AHB2 freq to 166Mhz.
   b Connect VDDQ pin to 2.5V. *1
   c Write register EFUSE0~EFUSE3.
   d Write register EFSCTL.LO_WEN to 1.
   e Wait till register EFSCTL.LO_WEN is set to 0.
   f Disconnect VDDQ pin from 3.3V and finish writing EFUSE.

3 Write high-128 bit.
   a Config AHB2 freq to 166Mhz.
   b Connect VDDQ pin to 2.5V. *1
   c Write register EFUSE3~EFUSE7.
   d Write register EFSCTL.HI_WEN to 1.
   e Wait till register EFSCTL.HI_WEN is set to 0.
   f Disconnect VDDQ pin from 3.3V and finish writing EFUSE.

NOTE:

*1: Do NOT pre-charge VDDQ too early before fuse program started.
The maximum 2.5V supply time to VDDQ must be strictly controlled less than 1sec.
Programming window is below 3ms.
Use on-chip counter and GPIO to coordinate external supply source.

41.3.2 Read EFUSE Flow

Read register EFUSE0~EFUSE7 after chip is reset.

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42 XBurst Boot ROM Specification

The JZ4770 contains an internal 8KB boot ROM. The CPU boots from the boot ROM after reset.

42.1 Boot Select

The boot sequence of the JZ4770 is controlled by boot_sel [2:0]. The configuration is shown as follow:

Table 42-1 Boot Configuration of JZ4770

boot_sel[2:0]	Boot method
111	NAND boot @ CS1
100	SD boot @ MSC0 (use GPIO Port A)
000	eMMC boot @ MSC0 (use GPIO Port A)
101	SPI boot @ SPI0/CE0
011	NOR boot @ CS4 (just for FPGA testing)
110	USB boot @ USB 2.0 device, EXTCLK=12MHz
001	USB boot @ USB 2.0 device, EXTCLK=26MHz
010	USB boot @ USB 2.0 device, EXTCLK=19.2MHz

42.2 Boot Procedure

After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[2:0] to determine the boot method.

2 If it is boot from NAND flash, 4 flags at the beginnig of NAND are read to know the NAND information including bus width(8 or 16 bits), page cycle(2 or 3 cycles) and its page size(512B, 2KB, 4KB or 8KB). Then 8KB code are read out from NAND to cache, if the 8KB reading failed, the next 8KB backup in NAND will be read. Then branch to cache at 12 bytes offset.

3 There 8KB backup reading failed, the 8KB backup at 64th, 128th, 192th , …, and finally 1280th page will be tried in consecutive order.

4 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 8KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/128 is used initially. When reading data, the clock EXTCLK/4 is used.

5 If it is boot from eMMC boot partition1 at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 16KB code from eMMC boot partition1 to cache and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/4 is used.

6 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

NOTE: The JZ4770's cache is 16KB, its address is from 0x80000000 to 0x80004000.

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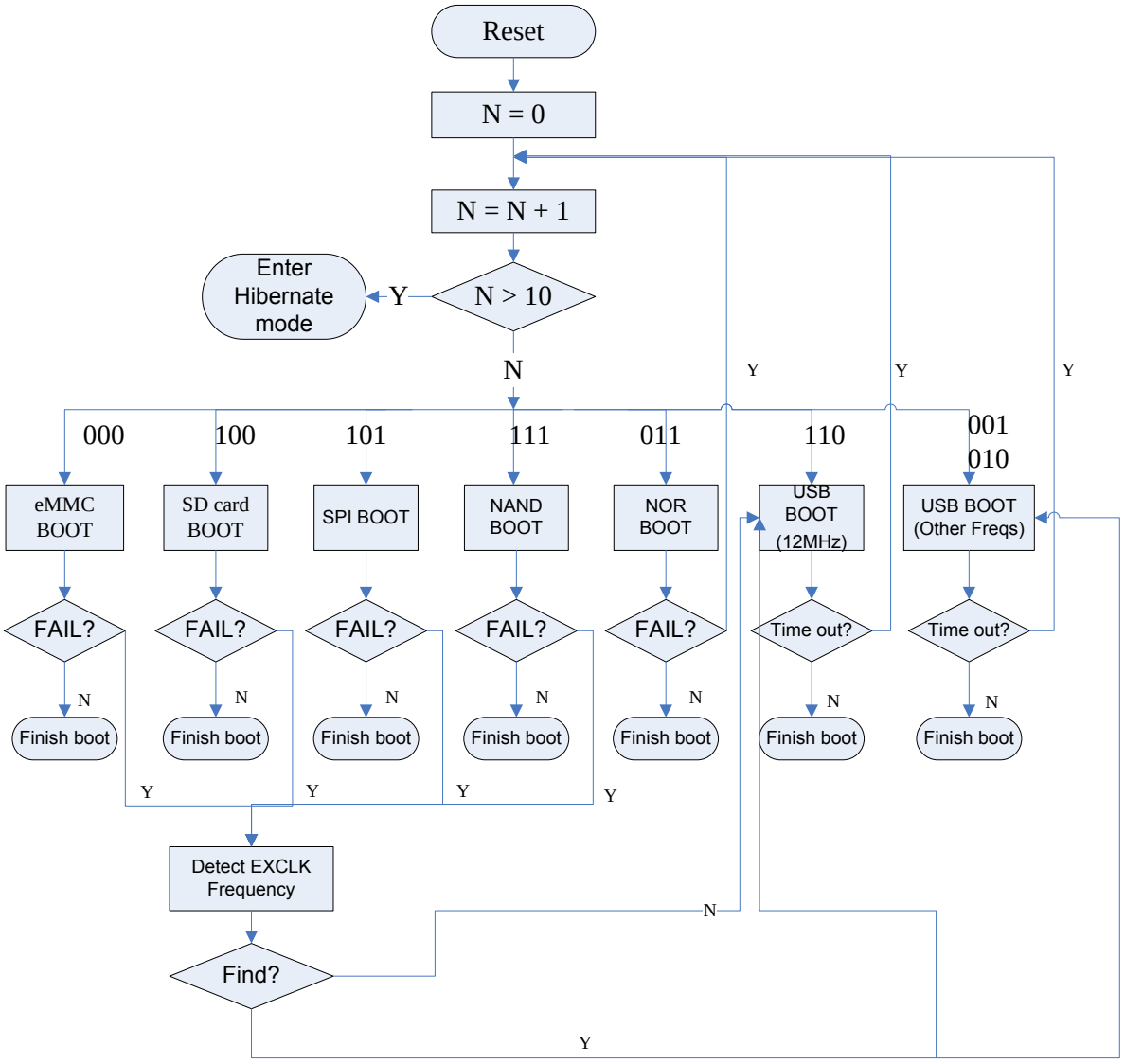


Figure 42-1 Boot sequence diagram of JZ4770

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42.3 NAND Boot Specification

If CPU boots from NAND flash (CS1), the boot ROM will read 4 flags from NAND flash to know the NAND information including bus width(8 or 16 bits), page cycle(2 or 3 cycles) and its page size(512, 2KB, 4KB or 8KB bytes).

The content and definition of the 4 flags are shown as follow:

Table 42-2 The definition of 4 flags in NAND flash

Name	Location (in byte)	length (in byte)	Value	Description
buswidth_flag	0-63	64	0x55 or 0xaa	Bus width. 0x55: 8bit bus width 0xaa: 16bit bus width
rowcycle_flag	64-95	32	0x55 or 0xaa	The number of bytes of row cycles. 0x55: 2-byte row cycles 0xaa: 3-byte row cycles
pagesize_flag1	96-127	32	0x55 or 0xaa	pagesize_flag1 pagesize_flag0 pagesize(byte). 0x55 0x55 512 0x55 0xaa 2048 0xaa 0x55 4096 0xaa 0xaa 8192
pagesize_flag0	128-159	32	0x55 or 0xaa	

The buswidth_flag containing 64 bytes locates at the beginning of NAND, if the bus width of NAND is 8 bit, the buswidth_flag should be filled with 0x55 for all 64 bytes, or else it should be filled with 0xaa. The rowcycle_flag containing 32 bytes locates behind the buswidth_flag, if the number of bytes of row cycles is 2, the flag should be filled with 0x55 for all 32 bytes, or else it should be filled with 0xaa. The pagesize_flag1 and pagesize_flag0 each containing 32 bytes locate behind the rowcycle_flag, which value should be filled is determined by the page size of NAND. Please refer to table 2. Totally, 160 bytes are allocated for the 4 flags.

At first, the first 256 bytes (which is a PN* unit) in NAND containing 4 flags will be read out to a buffer assuming the bus width of NAND is 8 bit. The buswidth_flag will be get from the buffer to detect the page size (whether 512B or not) and bus width of nand. If there is no 0x55 or 0xaa in buswidth_flag, 64th, 128th, 192th, ..., 1280th page will be tried in sequence. If failed at 1280th page, bootrom will jump to usb_boot. If bus width is 16 bit, 256 bytes will be read again to the buffer mentioned above. If buswidth_flag is valid, the rowcycle_flag will be obtained from the buffer to know the number of row cycles. At last, pagesize_flag1 and pagesize_flag0 will be obtained from the buffer to know precise page size.

8KB codes in NAND will be loaded up to dcache and transferred to icache and branch to icache at 160 bytes offset. Hardware PN and 24-bit BCH ECC will be used for every 256 bytes during reading. The

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ECC(39 bytes per 256 bytes data) stores in the data area of a NAND page behind the page storing code data. If no ECC error is detected or ECC error is correctable(number of error bits <= 24), NAND boots successfully. If uncorrectable error occurred, next 8KB backup at 64 pages behind will be tried. 64th, 128th, 192th, ..., 1280th page will be tried in sequence. If failed at 1280th page, bootrom will jump to usb_boot.

The distribution and structure of the boot code in NAND is shown as Figure 42-2.
The procedure of the JZ4770 NAND boot is shown as Figure 42-3.

NOTE: PN is short for pseudorandom noise which is used for supporting TLC (three-level cell) NAND.

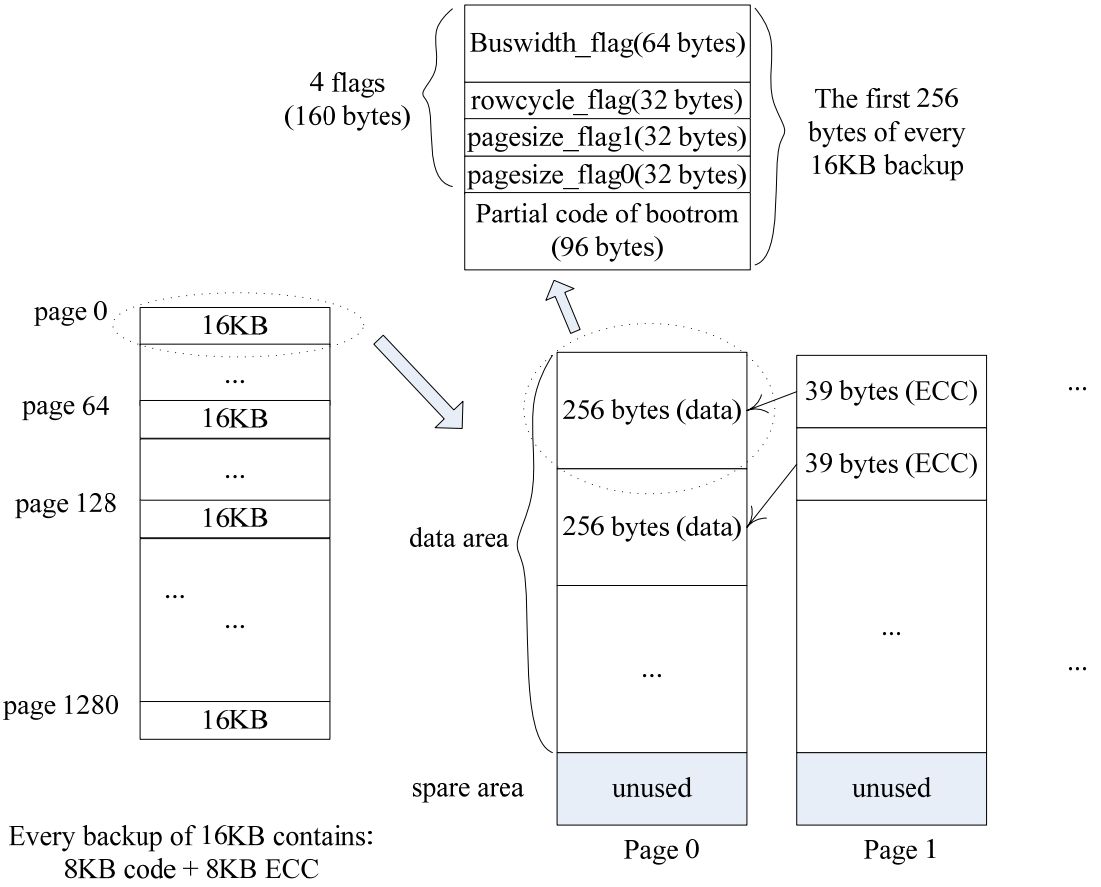


Figure 42-2 the distribution and structure of the boot code in NAND

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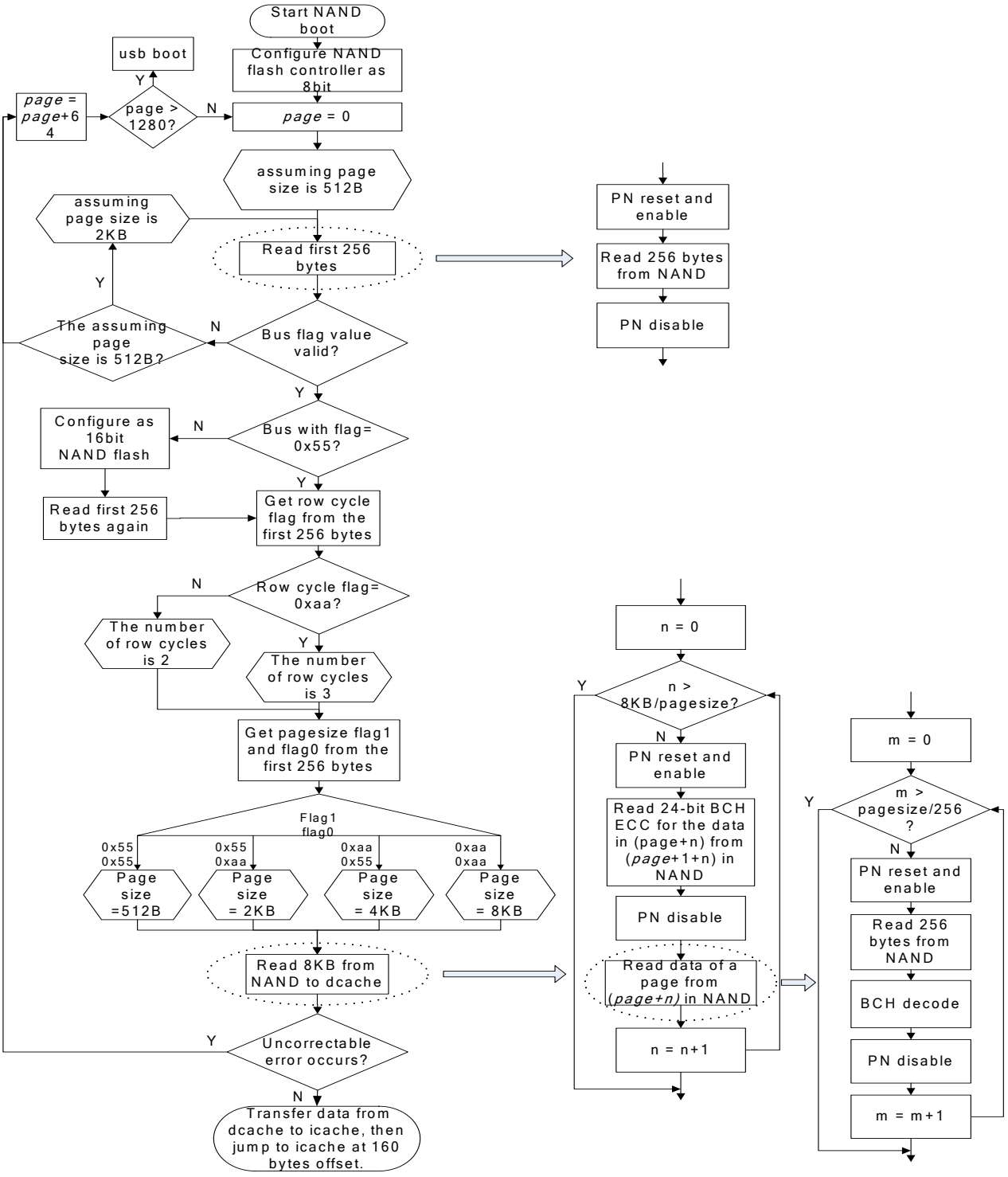


Figure 42-3 JZ4770 NAND Boot Procedure

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42.4 USB Boot Specification

When boot_sel[2:0] is selected as USB boot, the internal boot ROM downloads user program from the USB port to internal SRAM and branches to the internal SRAM to execute the program.

JZ4770 supports the external main crystal whose frequency is 12MHz, 19.2MHz, 26MHz.

The boot program supports both high-speed (480MHz) and full-speed (12MHz) transfer modes. The boot program uses the following two transfer types.

Table 42-3 Transfer Types Used by the Boot Program

Transfer Type	Description
Control Transfer	Used for transmitting standard requests and vendor requests.
Bulk Transfer	Used for responding to vendor requests and transmitting a user program.

The following figure shows an overview of the USB communication flow.

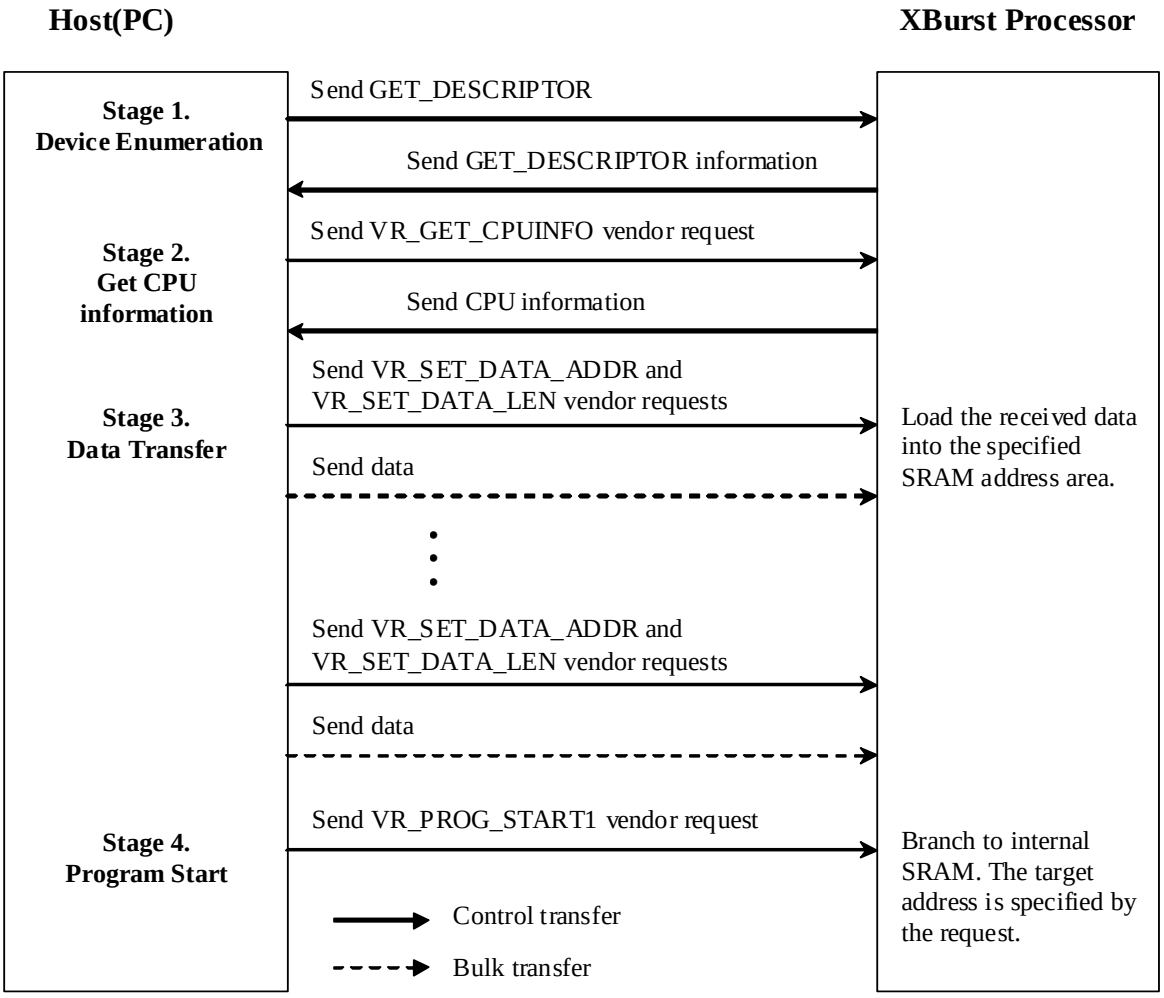


Figure 42-4 USB Communication Flow

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The vendor ID and product ID for the USB boot device are 0xa108 and 0x4770 respectively. The Configuration for USB is for Control Endpoint 0 with Max Packet Size equals 64 bytes, Bulk IN at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed, Bulk OUT at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed.

The USB boot program provides six vendor requests through control endpoint for user to download/upload data to/from device, and to branch to a target address to execute user program. The six vendor requests are VR_GET_CPU_INFO (0x00), VR_SET_DATA_ADDRESS (0x01), VR_SET_DATA_LENGTH (0x02), VR_FLUSH_CACHES (0x03), VR_PROGRAM_START1 (0x04) and VR_PROGRAM_START2 (0x05). User program is transferred through Bulk IN or Bulk OUT endpoint.

When JZ4770 is reset with boot_sel[2:0] equals 110b, 001b or 010b, the internal boot ROM will switch to USB boot mode and wait for USB requests from host. After connecting the USB device port to host, host will recognize the connection of a USB device, and start device enumeration. After finishing the device enumeration, user can send VR_GET_CPU_INFO (0x00) to query the device CPU information. If user wants to download/upload a program to/from device, two vendor requests VR_SET_DATA_ADDRESS (0x01) and VR_SET_DATA_LENGTH (0x02) should be sent first to tell the device the address and length in byte of the subsequent transferring data. Then data can be transferred through bulk-out/bulk-in endpoint. After this first stage program has been transferred to device, user can send vendor request VR_PROGRAM_START1 (0x04) to let the CPU to execute the program. This first stage program must not greater than 16KB and is normally used to init GPIO and SDRAM of the target board. At the end of the first stage program, it can return back to the internal boot ROM by jumping to ra ($31) register. Thus user can download a new program to the SDRAM of the target board like the first stage, and send vendor request VR_FLUSH_CACHES (0x03) and VR_PROGRAM_START2 (0x05) to let the CPU to execute the new program. Next figure is the typical procedure of USB boot.

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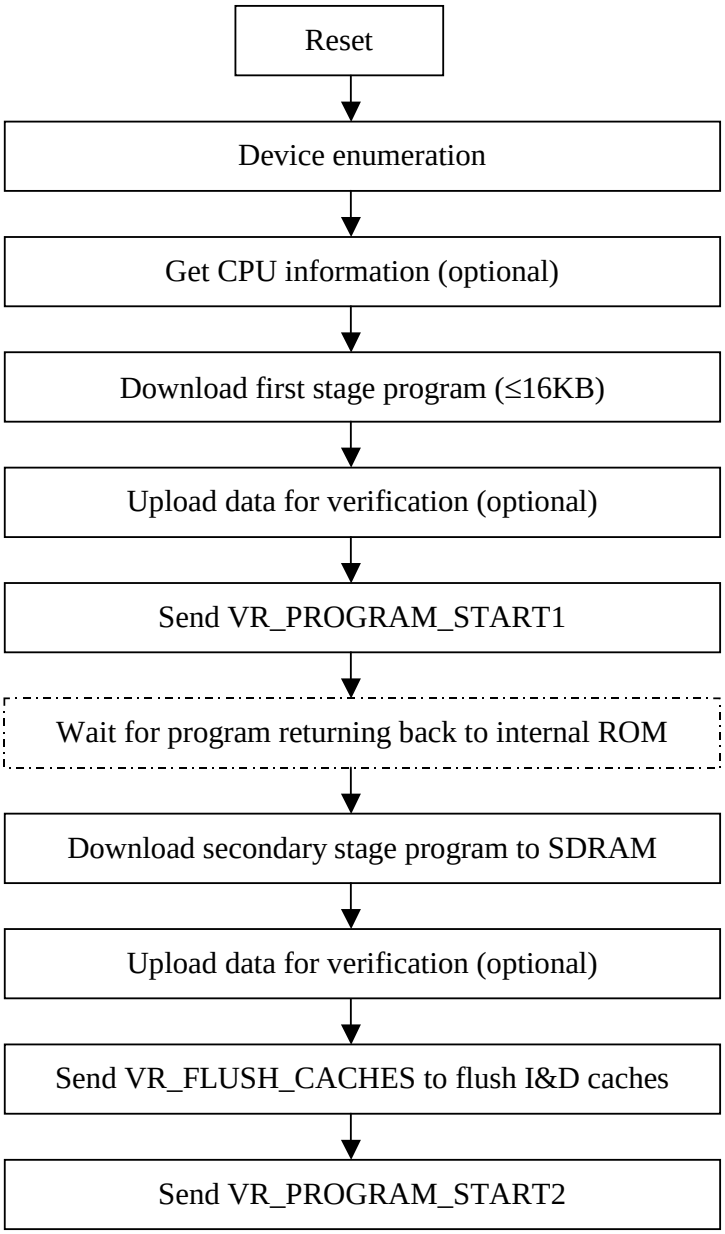


Figure 42-5 Typical Procedure of USB Boot

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Following tables list all the vendor requests that USB boot program supports:

Table 42-4 Vendor Request 0 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	00H	VR_GET_CPU_INFO: get CPU information.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0008H	8 bytes.

Table 42-5 Vendor Request 1 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	01H	VR_SET_DATA_ADDRESS: set address for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data address.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data address.
6	wLength	2	0000H	Not in used.

Table 42-6 Vendor Request 2 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	02H	VR_SET_DATA_LENGTH: set length in byte for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data length.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data length.
6	wLength	2	0000H	Not in used.

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Table 42-7 Vendor Request 3 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	03H	VR_FLUSH_CACHES: flush I-Cache and D-Cache.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0000H	Not in used.

Table 42-8 Vendor Request 4 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	04H	VR_PROGRAM_START1: transfer data from D-Cache to I-Cache and branch to address in I-Cache. **NOTE:** After downloading program from host to device for the first time, you can only use this request to start the program. Since the USB boot program will download data to D-Cache after reset. This request will transfer data from D-Cache to I-Cache and execute the program in I-Cache.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	wLength	2	0000H	Not in used.

Table 42-9 Vendor Request 5 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	05H	VR_PROGRAM_START2: branch to target address directly.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	WIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	WLength	2	0000H	Not in used.

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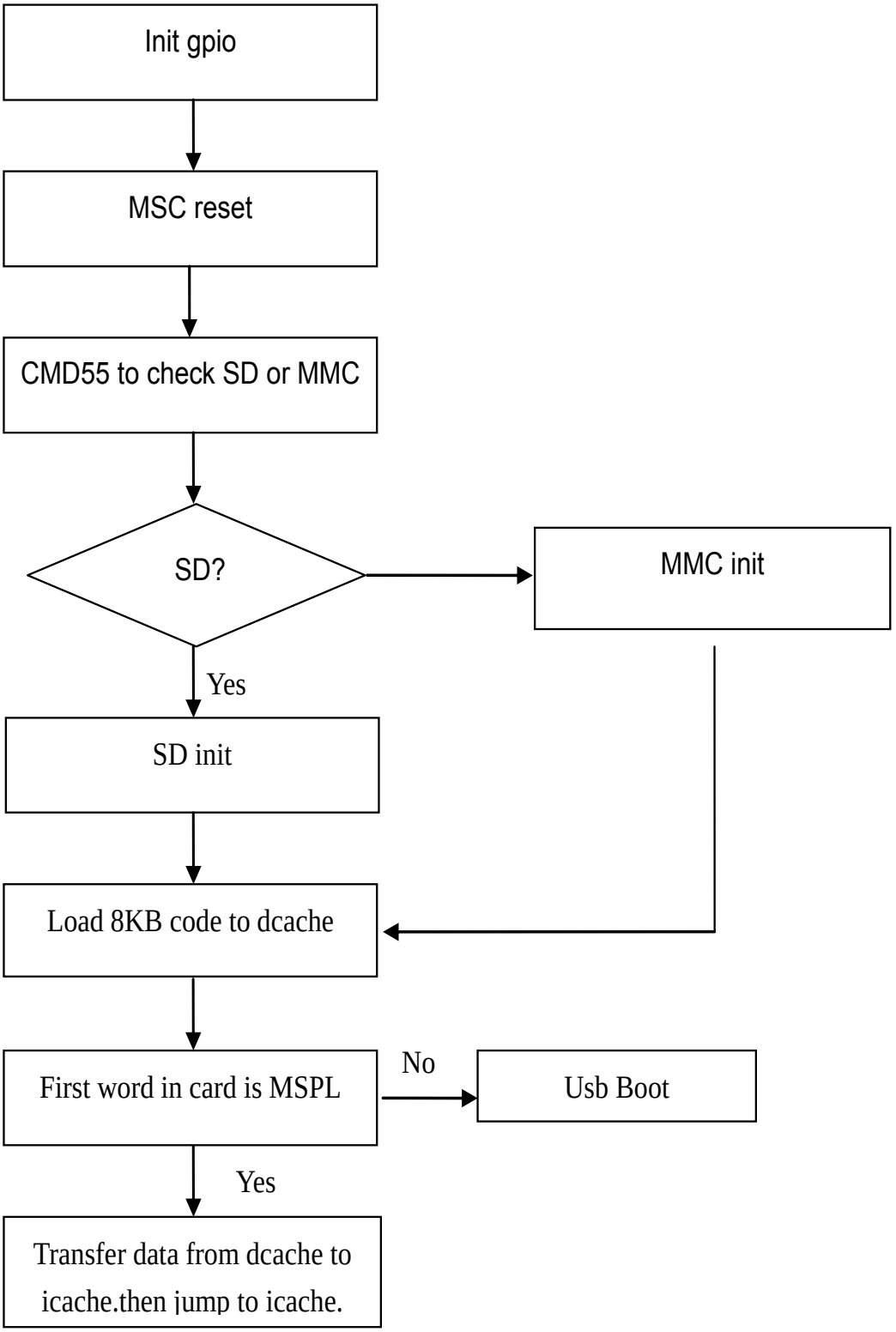
42.5 MMC/SD Boot Specification

All cards can boot from MMC/SD Boot from MSC0, the boot program will load 8KB code starting at sector 0 from MMC/SD card to cache. First the boot program initializes MSC0_D0, MSC0_CLK, MSC0_CMD as function pins. Only one data pin MSC0_D0 is used. Then the boot program sends CMD55 to test if it's SD or MMC card and initializes the card. At last it loads 8KB code from the card to cache and branches to execute the code in cache.

When initializing the card, the clock of EXTCLK/128 is used. And when reading data, the clock of EXTCLK/4 is used.

The procedure of the JZ4770 MMC/SD boot is shown as follow:

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42.6 eMMC Boot Specification

If eMMC is MultiMediaCard System Specification Ver. 4.4 compatible, you can use eMMC boot method. you should write boot code to boot partition1 , then the boot program will load 16KB code from eMMC boot partition1 area to cache. First the boot program initializes MSC0_D0, MSC0_CLK, MSC0_CMD as function pins. Only one data pin MSC0_D0 is used. Then the boot program sends CMD0 to set eMMC in boot mode. At last it loads 16KB code from the card to cache and branches to execute the code in cache. and the clock of EXTCLK/4 is used.

The procedure of the JZ4770 eMMC boot is shown as follow:

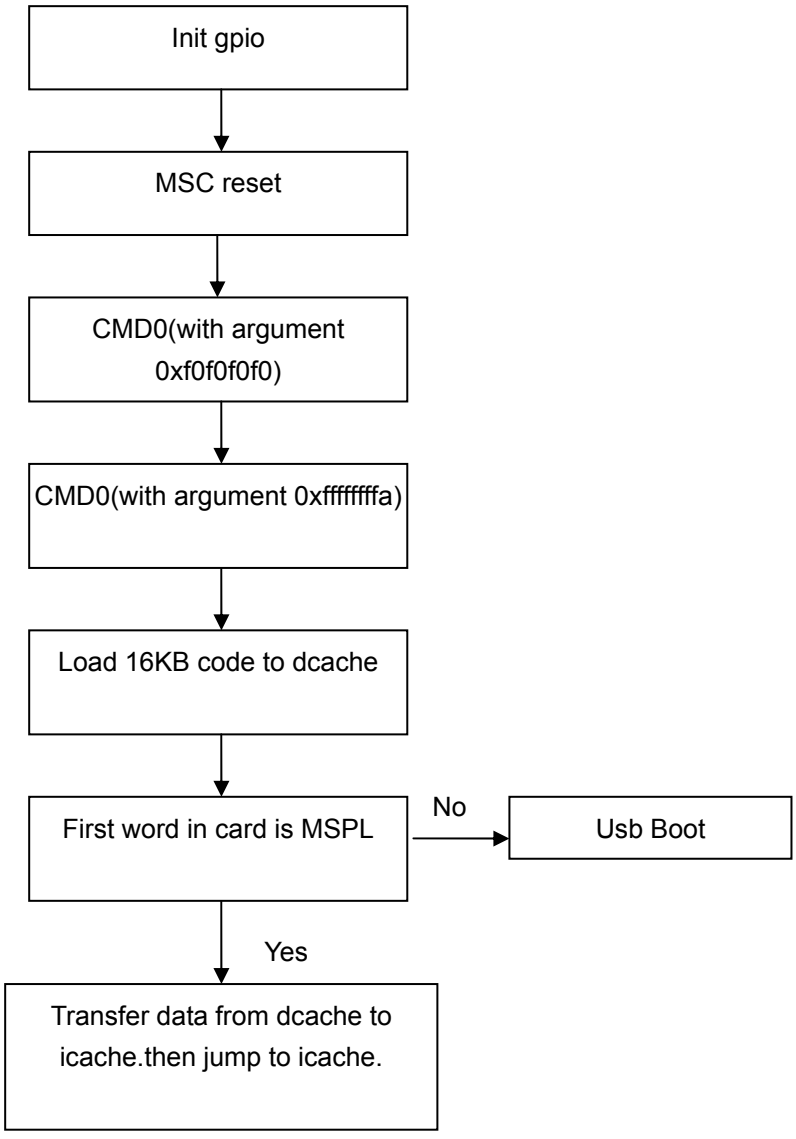


Figure 42-6 JZ4770 eMMC Boot Procedure

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43 Memory Map and Registers

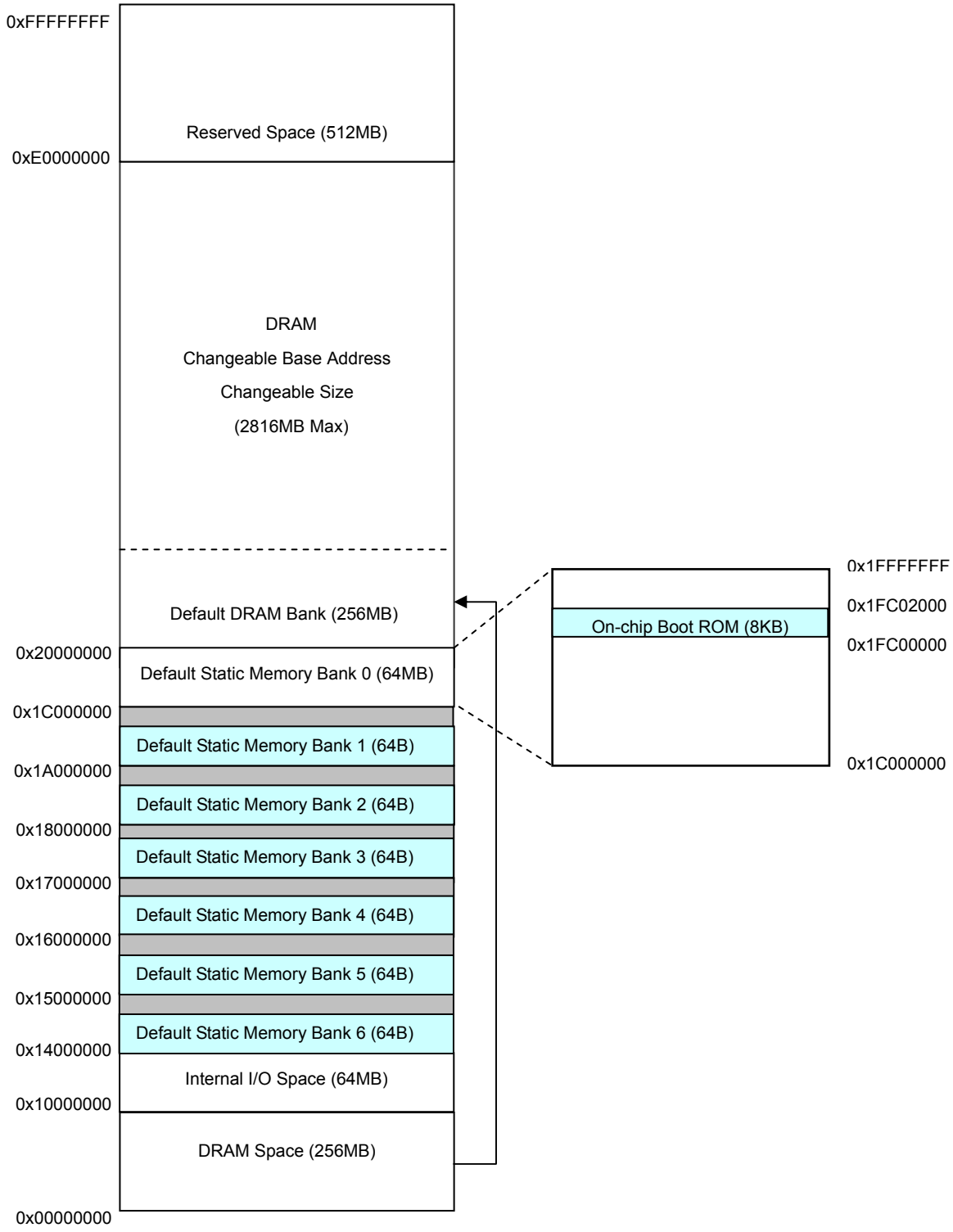
43.1 Physical Address Space Allocation

This chapter describes the physical address map, memory-mapped regions for every block in the JZ4770 processor. Both logical space and physical space of the JZ4770 are 32 bits wide. The 4Gbyte physical space is divided into several partitions for external memory, PCMCIA and internal I/O devices. Table 43-1 shows the basic physical memory map:

Table 43-1 JZ4770 Processor Physical Memory Map

Start Address	End Address	Size (MB)	Function
0x00000000	0x0FFFFFFF	256	DRAM Memory
0x10000000	0x10FFFFFF	16	I/O Devices on APB Bus
0x11000000	0x12FFFFFF	32	Reserved
0x13000000	0x13FFFFFF	16	I/O Devices on AHB Bus
0x14000000	0x1400003F	64B	Static Memory, CS6#
0x14000040	0x14FFFFFF		Reserved
0x15000000	0x1500003F	64B	Static Memory, CS5#
0x15000040	0x15FFFFFF		Reserved
0x16000000	0x1600003F	64B	Static Memory, CS4#
0x16000040	0x16FFFFFF		Reserved
0x17000000	0x1700003F	64B	Static Memory, CS3#
0x17000040	0x17FFFFFF		Reserved
0x18000000	0x1800003F	64B	Static Memory, CS2#
0x18000040	0x19FFFFFF		Reserved
0x1A000000	0x1A00003F	64B	Static Memory, CS1#
0x1A000040	0x1BFFFFFF		Reserved
0x1C000000	0x1FBFFFFF	60	Reserved
0x1FC00000	0x1FC01FFF	0.008	On-chip Boot ROM (8kB)
0x1FC02000	0x1FFFFFFF	3.992	Reserved
0x20000000	0xDFFFFFFF	3072	DRAM Memory
0xE0000000	0xFFFFFFFF	512	Reserved

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NOTES:

1 Data width of static memory banks can be configured to 8, 16 or 32 bits by software.

2 The 8KB address space from H'1FC00000 to H'1FC01FFF in bank 0 is mapped to on-chip boot ROM. The other memory spaces in bank 0 are not used.

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3 To support large DRAM space, DDRC re-maps the physical address H'00000000-H07FFFFFF to H'20000000-H'27FFFFFF. Software must configure the DRAM base address by the re-mapped address.

The JZ4770 processor AHB bus devices are mapped at the addresses based at 0x13000000, and each device is allocated for 64KB space. Table 43-2 lists the complete addresses:

Table 43-2 AHB0 Bus Devices Physical Memory Map

Module	Start Address	End Address	Size (KB)	Description
HARB	0x13000000	0x1300FFFF	64	AHB Bus Arbiter
DDRC	0x13020000	0x1302FFFF	64	External DDR Controller
LCDC TVE	0x13050000	0x1305FFFF	64	LCD Controller TV Encoder
CIM	0x13060000	0x1306FFFF	64	Camera Interface Module
AOSD Compress	0x13070000	0x1307FFFF	64	Alpha-OSD Controller Compress Controller
IPU	0x13080000	0x1308FFFF	64	Image Process Unit

Table 43-3 AHB1 Bus Devices Physical Memory Map

Module	Start Address	End Address	Size (KB)	Description
DMAGP0	0x13210000	0x1321FFFF	64	2D-DMA Controller 0
DMAGP1	0x13220000	0x1322FFFF	64	2D-DMA Controller 1
DMAGP2	0x13230000	0x1323FFFF	64	2D-DMA Controller 2
MCE	0x13250000	0x1325FFFF	64	Motion Compensation/Estimation
DEBLK1	0x13270000	0x1327FFFF	64	De-Block 1
DEBLK2	0x132D0000	0x132DFFFF	64	De-Block 2
VMAU	0x13280000	0x1328FFFF	64	Video Matrix Arithmetic Unit
SDE	0x13290000	0x1329FFFF	64	Stream DEC/ENC
AUX	0x132A0000	0x132AFFFF	64	Auxiliary cpu core
TCSM0	0x132B0000	0x132BFFFF	64	Tightly coupled sram 0
TCSM1	0x132C0000	0x132CFFFF	64	Tightly coupled sram 1
SRAM	0x132F0000	0x132FFFFF	64	General purpose sram

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Table 43-4 AHB2 Bus Devices Physical Memory Map

Module	Start Address	End Address	Size (KB)	Description
HARB	0x13400000	0x1340FFFF	64	AHB Bus Arbiter
NEMC	0x13410000	0x1341FFFF	64	External Normal Memory / Boot ROM / OTP Controller
DMAC	0x13420000	0x1342FFFF	64	DMA Controller
UHC	0x13430000	0x1343FFFF	64	USB 1.1 Host Controller
OTG	0x13440000	0x1344FFFF	64	OTG 2.0 Controller
BDMAC	0x13450000	0x1345FFFF	64	BCH/NAND DMA Controller
GPS	0x13480000	0x1348FFFF	64	GPS Baseband
ETHC	0x134B0000	0x134BFFFF	64	ETH Controller
BCH	0x134D0000	0x134DFFFF	64	BCH Controller
TSSI	0x134E0000	0x134EFFFF	64	TS Slave Interface

The JZ4770 processor APB bus devices are based at 0x10000000, and each device is allocated for 4KB space. Table 43-5 lists the complete addresses:

Table 43-5 APB Bus Devices Physical Memory Map

Module	Start Address	End Address	Size (KB)	Description
CPM	0x10000000	0x10000FFF	4	Clocks and Power Manager
INTC	0x10001000	0x10001FFF	4	Interrupt Controller
TCU OST WDT	0x10002000	0x10002FFF	4	Timer/Counter Unit Operating System Timer Watchdog Timer
RTC	0x10003000	0x10003FFF	4	Real-Time Clock
GPIO	0x10010000	0x10010FFF	4	General-Purpose I/O
AIC CODEC	0x10020000	0x10020FFF	4	AC97/I2S/SPDIF Controller Embedded CODEC
MSC0	0x10021000	0x10021FFF	4	MMC/SD 0 Controller
MSC1	0x10022000	0x10022FFF	4	MMC/SD 1 Controller
MSC2	0x10023000	0x10022FFF	4	MMC/SD 2 Controller

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UART0	0x10030000	0x10030FFF	4	UART 0
UART1	0x10031000	0x10031FFF	4	UART 1
UART2	0x10032000	0x10032FFF	4	UART 2
UART3	0x10033000	0x10033FFF	4	UART 3
UART4	0x10035000	0x10035FFF	4	UART 4
SCC	0x10040000	0x10040FFF	4	Smart Card Controller
SSI0	0x10043000	0x10043FFF	4	Synchronous Serial Interface 0
SSI1	0x10044000	0x10044FFF	4	Synchronous Serial Interface 1
I2C0	0x10050000	0x10050FFF	4	I2C 0 Bus Interface
I2C1	0x10051000	0x10051FFF	4	I2C 1 Bus Interface
I2C2	0x10055000	0x10055FFF	4	I2C 2 Bus Interface
KBC	0x10060000	0x10060FFF	4	KBC Bus Interface
SADC	0x10070000	0x10070FFF	4	SAR A/D Controller
PCM0	0x10071000	0x10071FFF	4	PCM 0 Interface
OWI	0x10072000	0x10072FFF	4	One-Wire Bus Interface
PCM1	0x10074000	0x10074FFF	4	PCM 1 Interface

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