Am93412/93422

256 x 4-Bit TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- High-speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs or with open-collector outputs
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

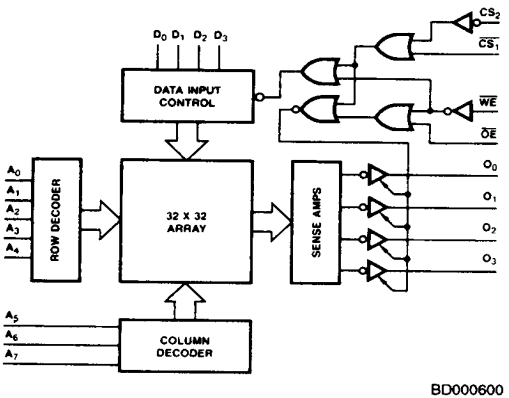
The Am93412/22 is comprised of 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active-LOW chip select one ($\overline{CS_1}$) and active HIGH chip select two (CS_2) as well as open collector OR tieable outputs (Am93412) or three-state outputs (Am93422).

An active-LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write line ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) LOW and the chip select two (CS_2) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

BLOCK DIAGRAM



BD000600

MODE SELECT TABLE

Input					Output	
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	Mode
L	X	X	X	X	*Hi-Z	Not Select
X	H	X	X	X	*Hi-Z	Not Select
H	L	H	H	X	*Hi-Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*Hi-Z	Write "0"
H	L	L	X	H	*Hi-Z	Write "1"
H	L	L	H	L	*Hi-Z	Write "0" Output Disable
H	L	L	H	H	*Hi-Z	Write "1" Output Disable

H = HIGH L = LOW X = Don't Care

*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93422A/422 and as output high level for the Am93412A/412.

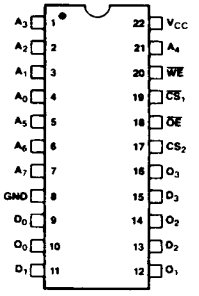
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	Am93412A	Am93412	Am93412A	Am93412
Three-State Part Number	Am93422A	Am93422	Am93422A	Am93422
Access Time	35 ns	45 ns		60 ns
Temperature Range	C	C	M	M

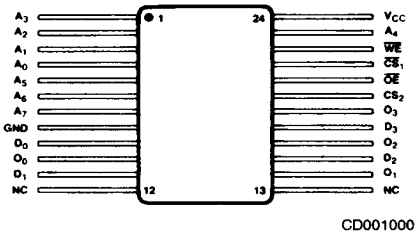
IMOX is a trademark of Advanced Micro Devices, Inc.

Publication # 03080 Rev. C Amendment /0
Issue Date: May 1986

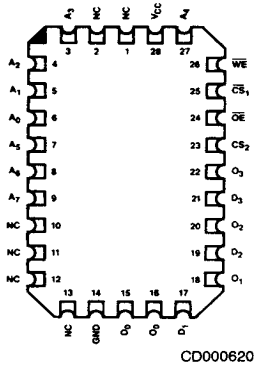
CONNECTION DIAGRAMS
Top View



CD000610



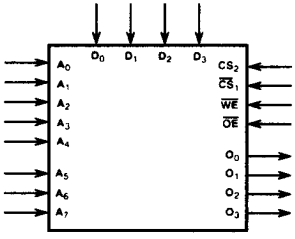
CD001000



CD000620

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



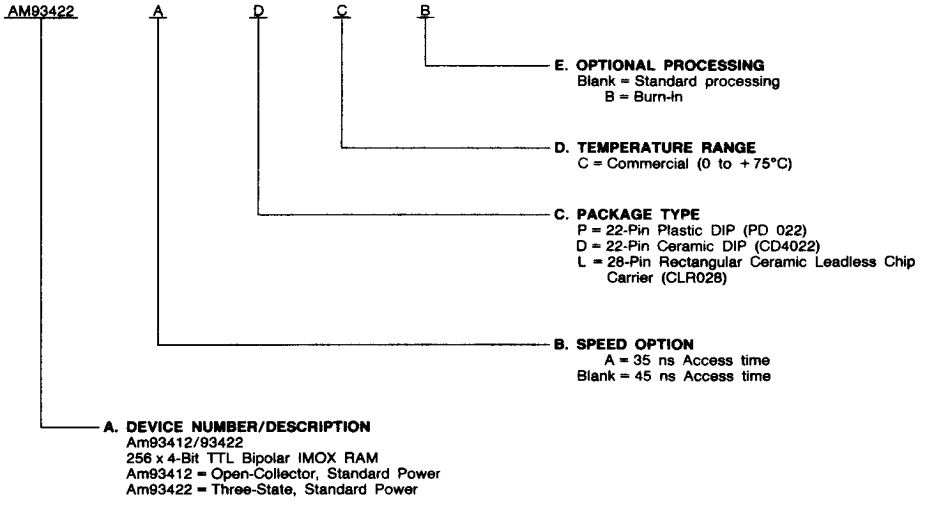
LS000221

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM93422	PC, PCB, DC, DCB, LC, LCB
AM93422A	
AM93412	
AM93412A	

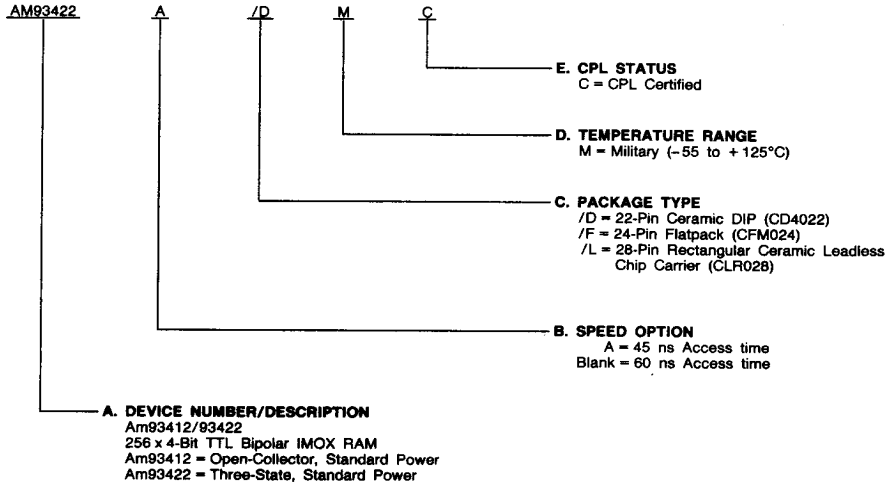
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for CPL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM93422	/DMC, /FMC, /LMC
AM93422A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 6)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

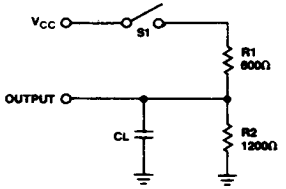
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V			−100	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)		−10		−90	mA
I_{CC}	Power Supply Current	ALL inputs = GND, V_{CC} = Max.	Commercial			155	mA
			Military			170	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4 V	Am93422A/422		0	50	μA
		V_{OUT} = 0.5 V, V_{CC} = Max.	Am93422A/422	−50	0		
		V_{OUT} = 4.5 V	Am93412A/412		0	100	
C_{IN}	Input Pin Capacitance	See Note 5			4		pF
C_{OUT}	Output Pin Capacitance	See Note 5			7		pF

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Applies only to devices with three-state outputs (Am93422 family).
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0 MHz at initial characterization.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_j.
   $\theta_{jA} \cong 60°C/W$ (with moving air) for Ceramic DIP.
   $\theta_{jC} \cong 36°C/W$ for Flatpack and Leadless Chip Carrier.

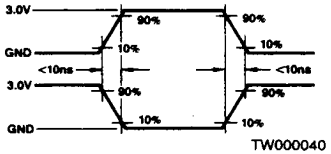
*See the last page of this spec for Group A Subgroup testing information.

SWITCHING TEST CIRCUIT



TC000200

SWITCHING TEST WAVEFORMS



TW000040

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

*See notes after Switching Characteristics.

3

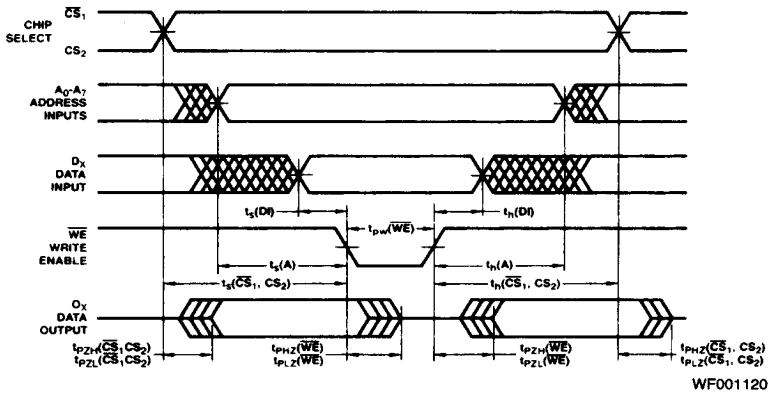
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93412A/93422A C Devices Min.	Am93412A/93422A C Devices Max.	Am93412A/93422A M Devices Min.	Am93412A/93422A M Devices Max.	Am93412/93422 C Devices Min.	Am93412/93422 C Devices Max.	Am93412/93422 M Devices Min.	Am93412/93422 M Devices Max.	Units
1	t_{PLH}(A)(Note 2)	Delay from Address to Output (Address Access Time)		35		45		45		60	ns
2	t_{PHL}(A)(Note 2)										
3	$t_{PZH}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Active Output and Correct Data		25		35		30		45	ns
4	$t_{PZL}(\overline{CS_1}, CS_2)$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		25		40		40		50	ns
6	$t_{PZL}(\overline{WE})$										
7	$t_{PZH}(\overline{OE})$	Delay from Output Enable to Active Output and Correct Data		25		35		30		45	ns
8	$t_{PZL}(\overline{OE})$										
9	t_s(A)	Setup Time Address (Prior to Initiation of Write)	5		5		10		10		ns
10	t_h(A)	Hold Time Address (After Termination of Write)	5		5		5		5		ns
11	t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
12	t_h(DI)	Hold Time Data Input (After Termination of Write)	5		5		5		5		ns
13	$t_s(\overline{CS_1}, CS_2)$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
14	$t_h(\overline{CS_1}, CS_2)$	Hold Time Chip Select (After Termination of Write)	5		5		5		5		ns
15	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	20		35		30		40		ns
16	$t_{PHZ}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Inactive Output (Hi-Z)		30		35		30		45	ns
17	$t_{PLZ}(\overline{CS_1}, CS_2)$										
18	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		30		40		35		45	ns
19	$t_{PLZ}(\overline{WE})$										
20	$t_{PHZ}(\overline{OE})$	Delay from Output Enable to Inactive Output (Hi-Z)		30		35		30		45	ns
21	$t_{PLZ}(\overline{OE})$										

Notes:
1. For AC and Functional Testing, $V_{IH} = 3.0$ V and $V_{IL} = 0.0$ V.
2. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. For open-collector devices, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, CS_2,$\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$, $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.
4. For three-state output devices, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}\ CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

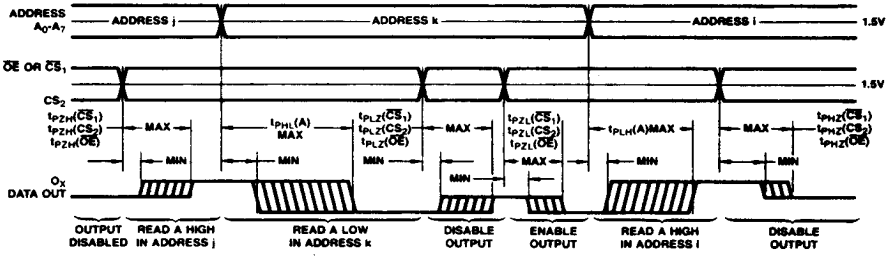
*See the last page of this spec for Group A Subgroup testing information.

SWITCHING WAVEFORMS



WF001120

Write Mode (With $\overline{OE}$ = LOW)



WF001130

Read Mode

Switching delays form address input, output enable input and the chip select inputs to the data output. For the Am93422A/422 disabled output is OFF, represented by a single center line. For the Am93412A/412, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11	12	t_h(DI)	9, 10, 11
2	t_{PHL}(A)	9, 10, 11	13	$t_s(\overline{CS_1}, CS_2)$	9, 10, 11
3	$t_{PZH}(\overline{CS_1}, CS_2)$	9, 10, 11	14	$t_h(\overline{CS_1}, CS_2)$	9, 10, 11
4	$t_{PZL}(\overline{CS_1}, CS_2)$	9, 10, 11	15	$t_{PW}(\overline{WE})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	16	$t_{PHZ}(\overline{CS_1}, CS_2)$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	17	$t_{PLZ}(\overline{CS_1}, CS_2)$	9, 10, 11
7	$t_{PZH}(\overline{OE})$	9, 10, 11	18	$t_{PHZ}(\overline{WE})$	9, 10, 11
8	$t_{PZL}(\overline{OE})$	9, 10, 11	19	$t_{PLZ}(\overline{WE})$	9, 10, 11
9	t_S(A)	9, 10, 11	20	$t_{PHZ}(\overline{OE})$	9, 10, 11
10	t_h(A)	9, 10, 11	21	$t_{PLZ}(\overline{OE})$	9, 10, 11
11	t_s(DI)	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.