Final COM'L: A/B/-20/AL MIL: A T-46-19-13

PAL20X10A Series
AmPAL20L10B/-20/AL

XOR Registered 24-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- XOR gates on registered outputs
- Efficient implementation of counters
- Popular 24-pin architectures: 20L10, 20X10, 20X8, 20X4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20X10A Series offers Exclusive-OR gates preceding each flip-flop. The XOR gate combines two sum terms, each composed of two product terms. This extra level of logic is very efficient for counter applications.

The combinatorial member of the family, the PAL20L10, offers three product terms per output with no XOR gate. A fourth product term provides the enable term. While the registered devices are offered in only one performance option, the 20L10 is offered in four performance grades. Note that three of these options follow the "old" AMD part numbering system while the fourth follows the "old" MMI part numbering system, as do the registered devices.

The family utilizes Advanced Micro Devices' advanced bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE	t_{PD} (ns)	I_{CC} (mA)
AmPAL20L10B AmPAL20L10-20 AmPAL20L10AL PAL20L10A	12	8 comb. 2 comb.	3 3	I/O –	prog. prog.	15 20 25 30	210 165 105 165
PAL20X10A	10	10 reg.	4, XOR	reg.	pin	30 (ts)	180
PAL20X8A	10	8 reg. 2 comb.	4, XOR 3	reg. I/O	pin prog.	30	180
PAL20X4A	10	4 reg. 6 comb.	4, XOR 3	reg. I/O	pin prog.	30	180

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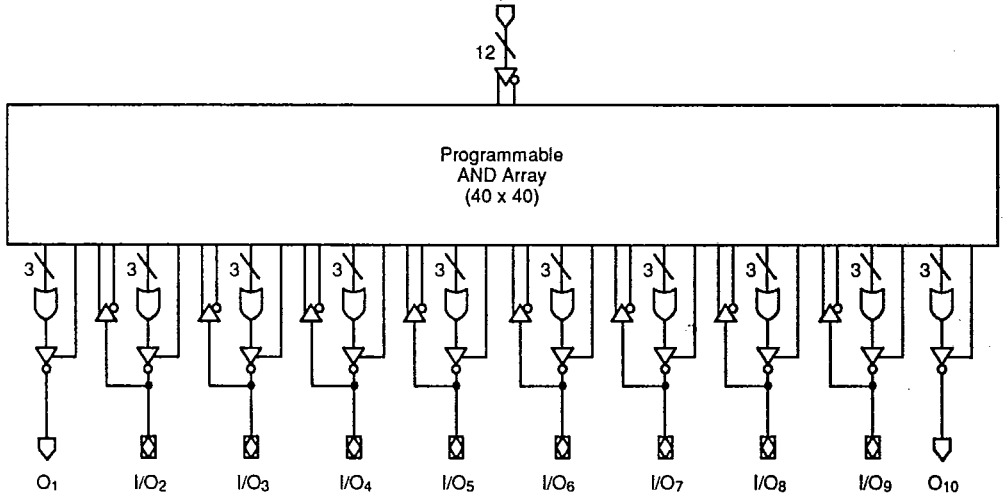
BLOCK DIAGRAMS

T-46-19-13

PAL20L10



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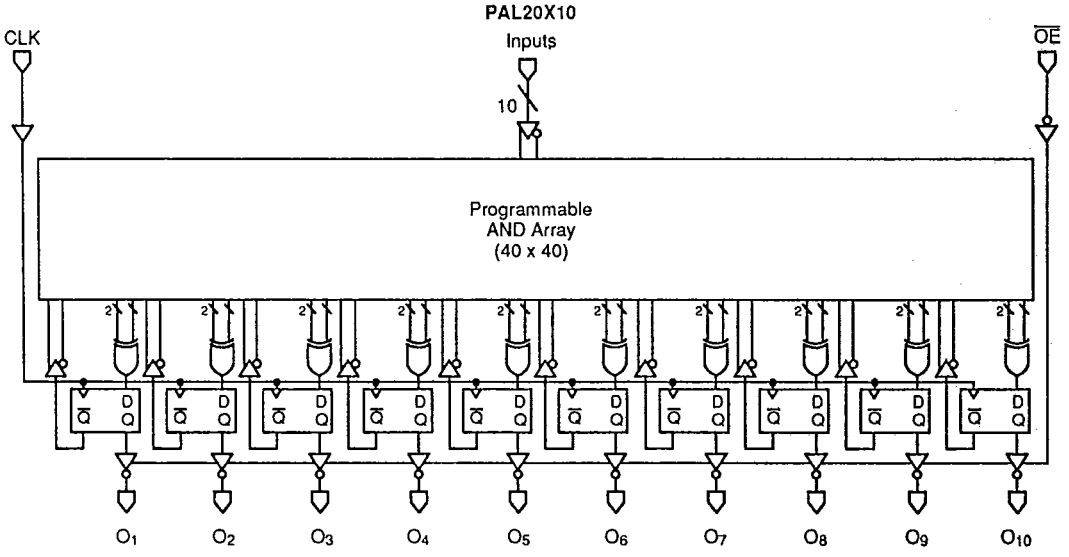
PAL20X10



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BLOCK DIAGRAMS

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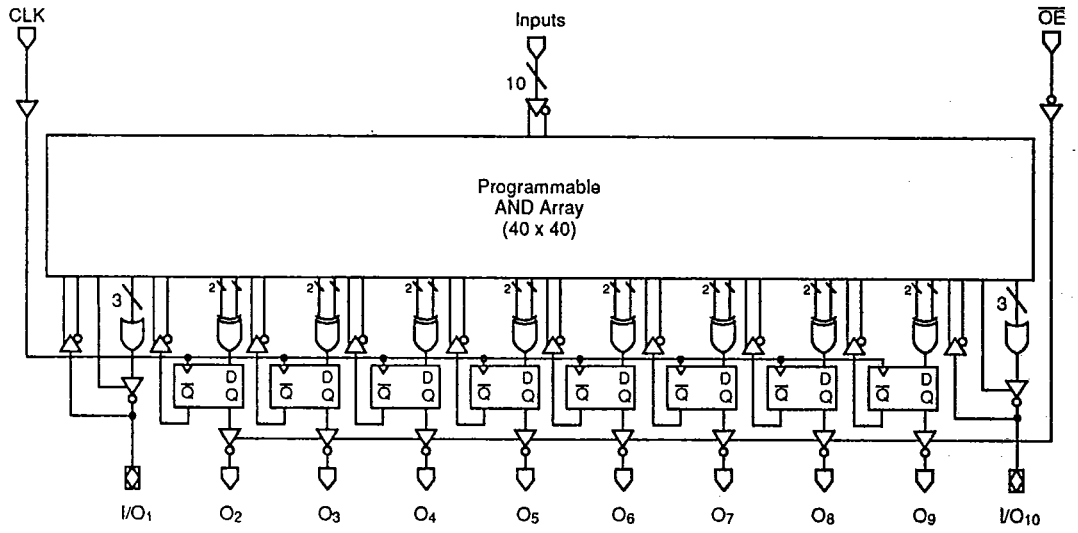
PAL20X8



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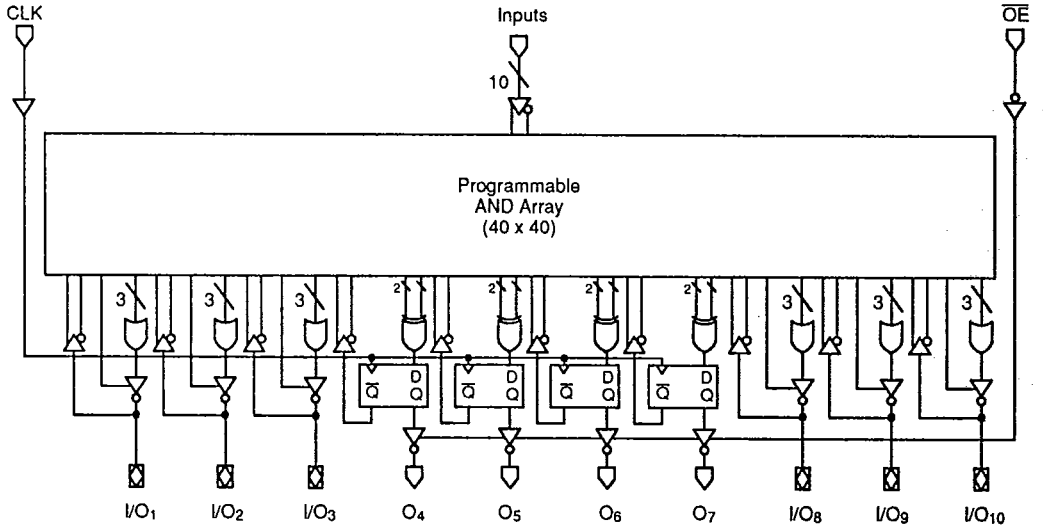
PAL20X4



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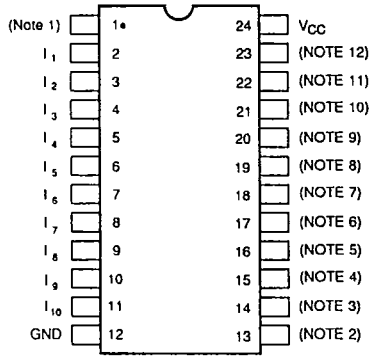
CONNECTION DIAGRAMS
Top View

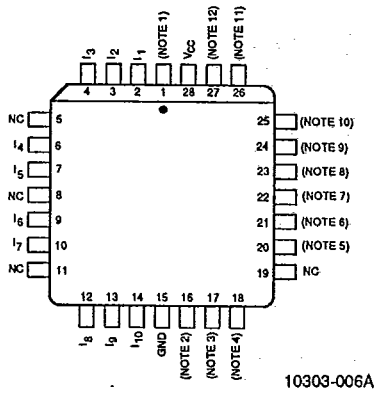
T-46-19-13

SKINNYDIP/FLATPACK



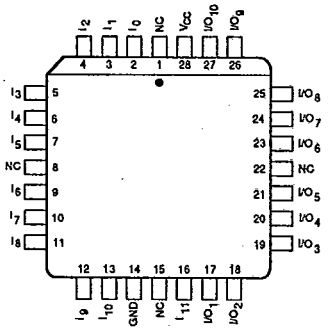
10303-005A

PLCC (except AmPAL20L10)



10303-006A

PLCC
AmPAL20L10 only



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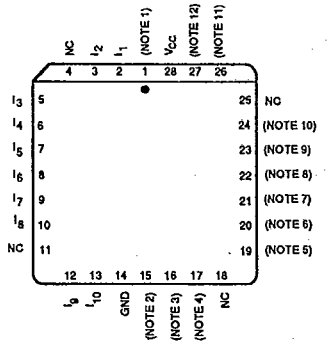
LCC



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Note	20L10	20X10	20X8	20X4
1	I_0	CLK	CLK	CLK
2	I_{11}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	I/O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	O_7
10	I/O_8	O_8	O_8	I/O_8
11	I/O_9	O_9	O_9	I/O_9
12	O_{10}	O_{10}	I/O_{10}	I/O_{10}

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
O	Output
$\overline{OE}$	Output Enable
Vcc	Supply Voltage

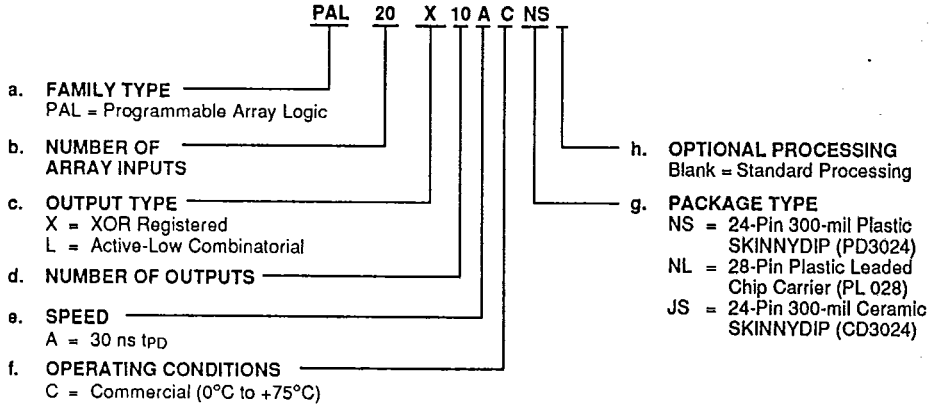
Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Commercial Products (MMI Marking Only)

T-46-19-13

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Operating Conditions
g. Package Type
h. Optional Processing



Valid Combinations	
PAL20L10A	CNS, CNL, CJS
PAL20X10A	
PAL20X8A	
PAL20X4A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

ORDERING INFORMATION
Commercial Products (AMD Marking Only)

T-46-19-13

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Power**
g. **Package Type**
h. **Operating Conditions**
i. **Optional Processing**

AmPAL 20 L 10 A L P C

a. **FAMILY TYPE**
AmPAL = Programmable Array Logic

b. **NUMBER OF ARRAY INPUTS**

c. **OUTPUT TYPE**
L = Active-Low Combinatorial

d. **NUMBER OF OUTPUTS**

e. **SPEED**
-20 = 20 ns t_{PD}
B = 15 ns t_{PD}
A = 25 ns t_{PD}

f. **POWER**
Blank = Full Power (165–210 mA I_{CC})
L = Low Power (105 mA I_{CC})

g. **PACKAGE TYPE**
P = 24-Pin 300-mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
D = 24-Pin 300-mil Ceramic SKINNYDIP (CD3024)

h. **OPERATING CONDITIONS**
C = Commercial (0°C to +75°C)

i. **OPTIONAL PROCESSING**
Blank = Standard Processing

Valid Combinations		
AmPAL20L10	B, -20, AL	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

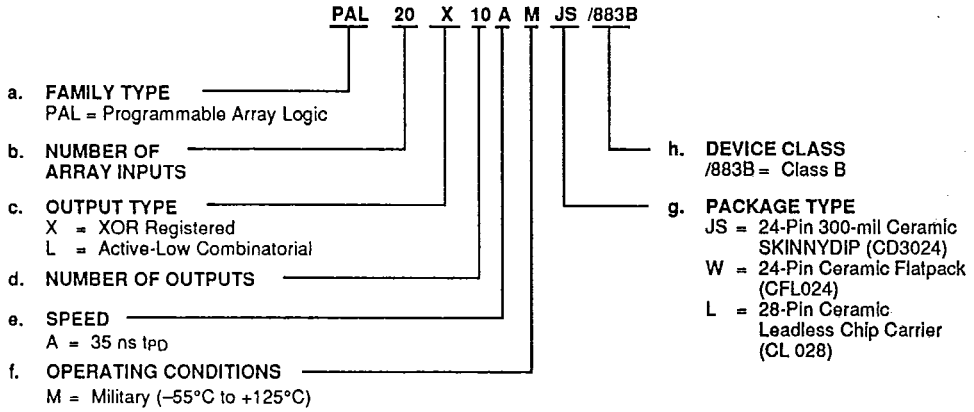
Note: Marked with AMD logo.

ORDERING INFORMATION
APL Products

T-46-19-13

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Operating Conditions**
g. **Package Type**
h. **Device Class**



Valid Combinations	
PAL20L10A	MJS/883B, MW/883B, ML/883B
PAL20X10A	
PAL20X8A	
PAL20X4A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

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FUNCTIONAL DESCRIPTION

Four different devices are available in the 20X10 Series, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have ten dedicated input lines, and each combinatorial output is an I/O pin. The 20L10 has twelve dedicated input lines, and only eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20X10A Series will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL20X10A Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20X10 Series design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact. For the AmPAL20L10, the array will read as if every fuse is programmed.

Pinouts

All members of the PAL20X10 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. The AmPAL20L10 and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with no-connects on pins 1, 8, 15, and 22. The older PAL20X10A Series devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19.

A different LCC pinout is offered for military products.The older PAL20X10A Series devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25.

Series	Com'l PLCC No-connects	Mil LCC No-connects
AmPAL20L10 B/-20/AL	1, 8, 15, 22 (JEDEC)	N/A
PAL20X10A Series (inc. PAL20L10A)	5, 8, 11, 19	4, 11, 18, 25

Quality and Testability

The PAL20X10 Series offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL20X10A Series is fabricated with AMD's advanced junction-isolated bipolar process. The array connections are formed with proven TiW fuses for reliable operation.

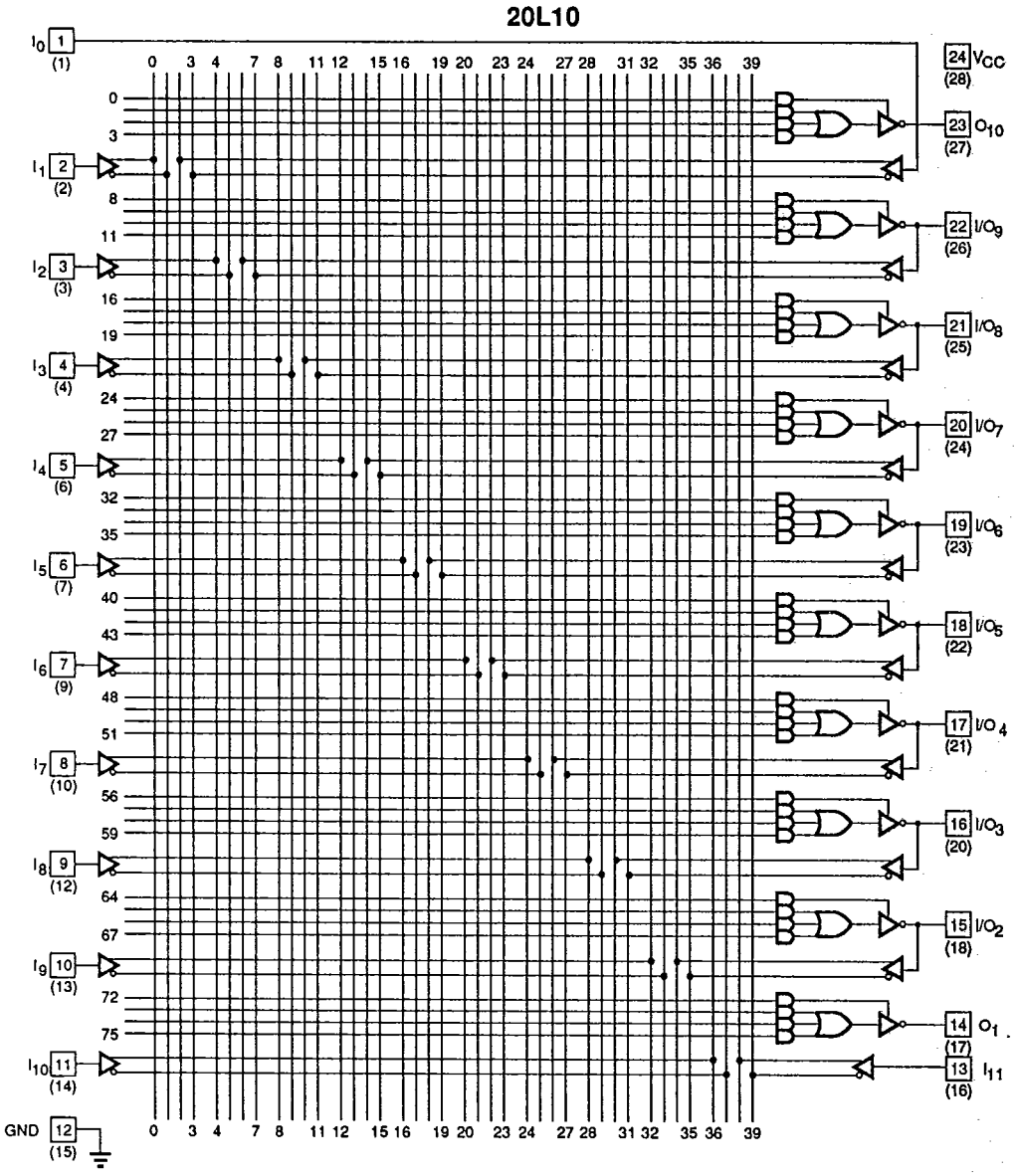
The AmPAL20L10 is fabricated with the IMOX™ oxide-isolated bipolar process using proven PtSi fuses.

T-46-19-13

LOGIC DIAGRAM

SKINNYDIP (PLCC, PAL20L10A only) Pinouts

See Connection Diagrams for LCC and AmPAL20L10 PLCC Pinouts



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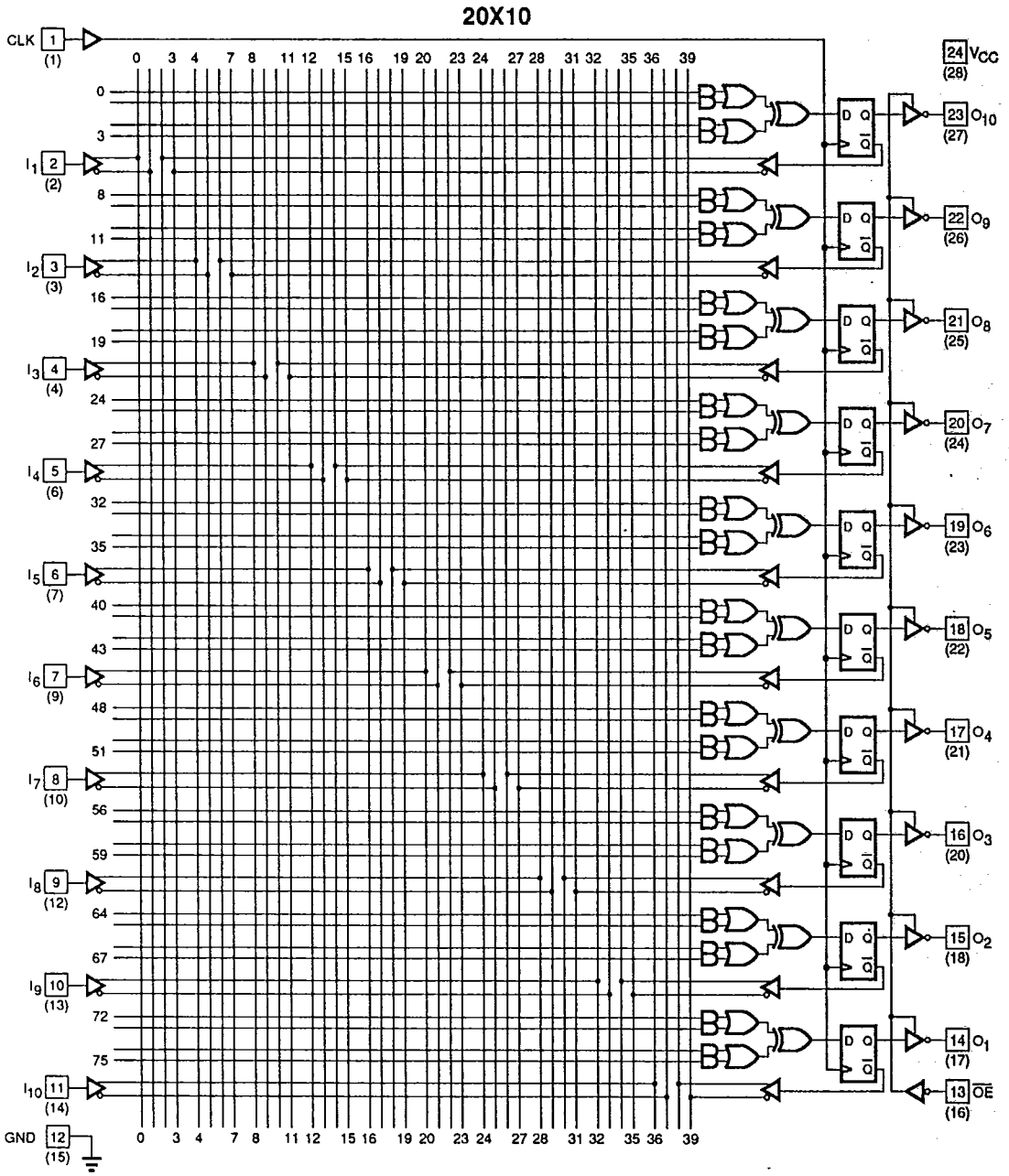
LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts
See Connection Diagrams for LCC Pinout

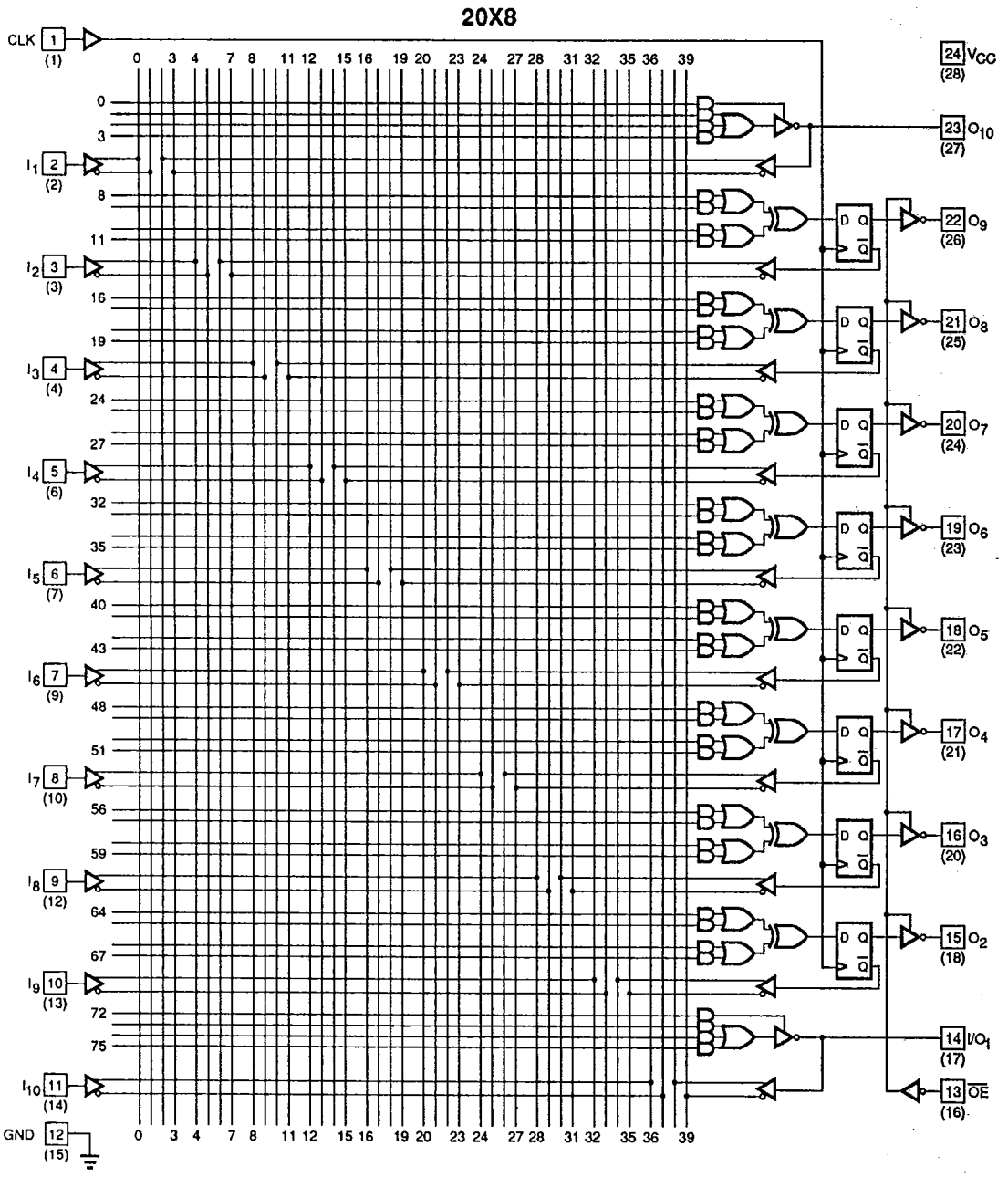
T-46-19-13



10303-010A

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts
See Connection Diagrams for LCC Pinout

T-46-19-13



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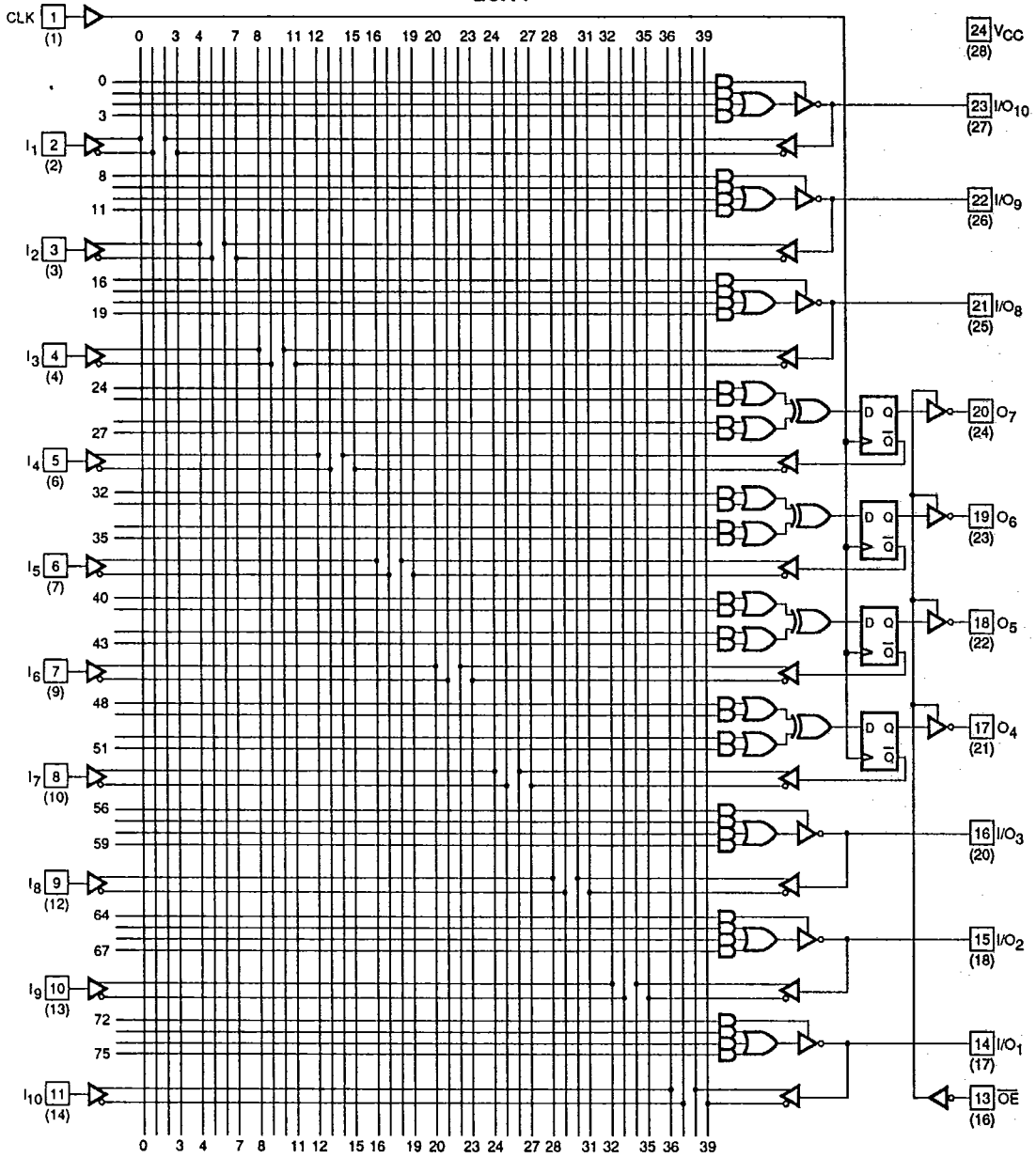
LOGIC DIAGRAM

SKINNYDIP (PLCC) Pinouts

See Connection Diagrams for LCC Pinout

T-46-19-13



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.			−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	20X10A, 20X8A, 20X4A		180	mA
			20L10A		165	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L10A, 20X8A, 20X4A		30	ns
t_S	Setup Time from Input or Feedback to Clock			20X10A, 20X8A, 20X4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		22.2		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L10A, 20X8A, 20X4A		30	ns
t_{ER}	Input to Output Disable Using Product Term Control					30	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to 5.5 V
DC Output or I/O Pin Voltage	−0.5 V to 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA $V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.			−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)			−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)		−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	20X10A, 20X8A, 20X4A		180	mA
			20L10A		165	

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L10A, 20X8A, 20X4A		35	ns
t_S	Setup Time from Input or Feedback to Clock			20X10A, 20X8A, 20X4A	40		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			35		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		15.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		18.2		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L10A, 20X8A, 20X4A		35	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					35	ns

2

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

T-46-19-13

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	20L10B		210	mA
			20L10-20		165	
			20L10AL		105	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

T-46-19-13

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

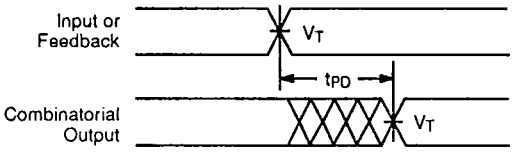
Parameter Symbol	Parameter Description	20L10B		20L10-20		20L10AL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		20		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		20		25	ns

Notes:

2. See Switching Test Circuit for test conditions.

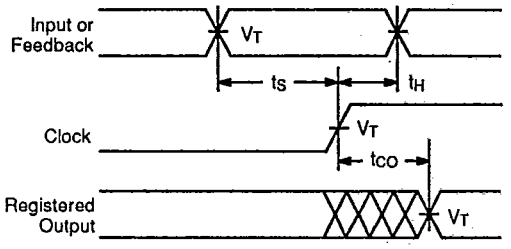
SWITCHING WAVEFORMS

T-46-19-13



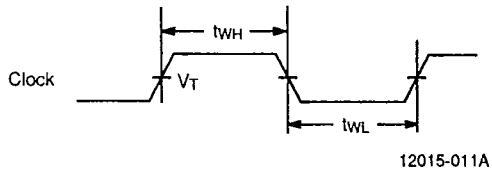
12015-010A

Combinatorial Output



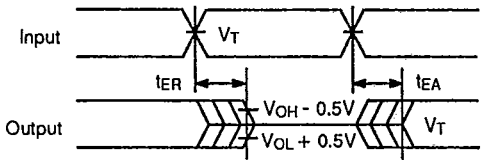
12015-012A

Registered Output



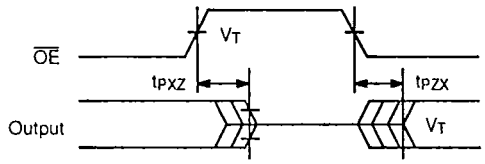
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



12015-014A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

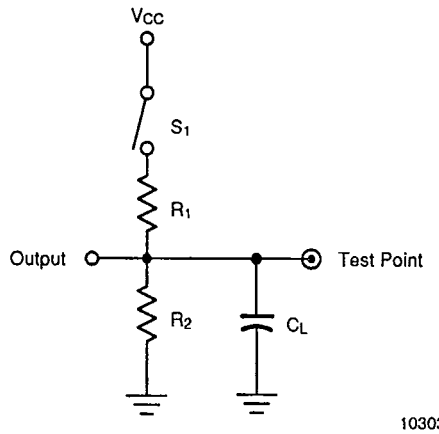
T-46-19-13

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT



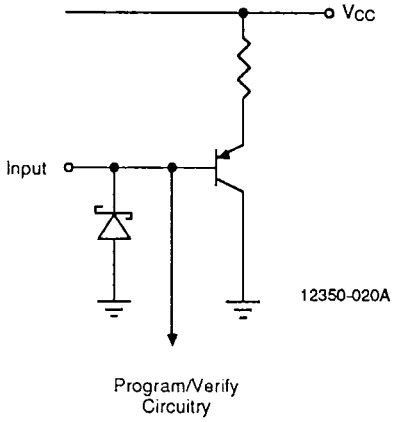
10303-013A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

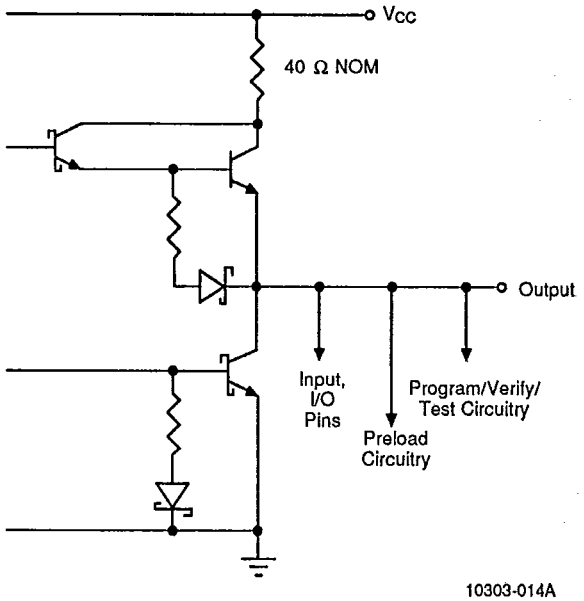
INPUT/OUTPUT EQUIVALENT SCHEMATICS

T-46-19-13

Typical Input



Typical Output



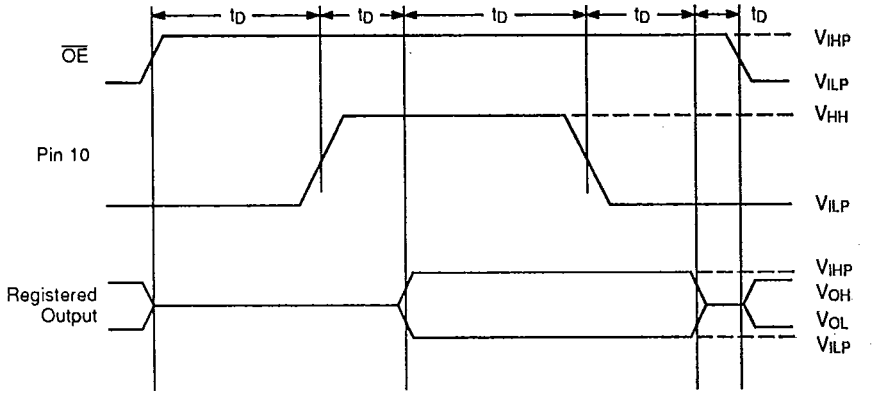
OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Raise pin 10 to V_{HH} to enter preload mode.
4. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
5. Lower pin 10 to V_{ILP}.
6. Remove V_{ILP}/V_{IHP} from all registered output pins.
7. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

T-46-19-13

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19	20	21	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload		4.5		V
t_D	Delay time	100	200	1000	ns



10303-015A

Output Register Preload Waveform

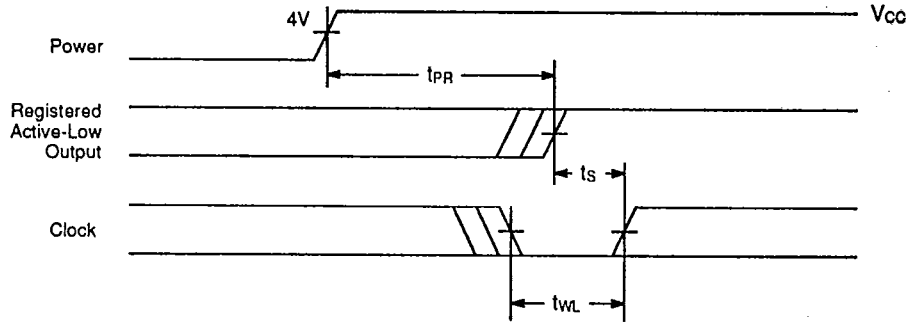
POWER-UP RESET

T-46-19-13

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform